

## **Digital Logic**

## **Pocket Data Book**

2003 SLL

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#### Little Logic

Series	Supply Voltage Vcc (V)	Operating Free-air Temperature Ta ( $^{\circ}$ C)
SN74AUC1G/2G/3G	0.8~2.7	-40~85
SN74LVC1G/2G/3G	1.65~5.5	-40~85
SN74AHC1G	2.0~5.5	-40~85
SN74AHC1GxxH	2.0~5.5	-40~85
SN74AHC2GxxH	2.0~5.5	-40~85
SN74AHCT1G	4.5~5.5	-40~85

#### GATE/OCTAL/Widebus<sup>TM</sup>/Widebus+

Series	Supply Voltage Vcc (V)	Operating Free-air Temperature Ta (°C)
SN74ABT	4.5~5.5	-40~85
SN74BCT SN74F SN74ALS SN74AS	4.5~5.5	0~70
SN74LS SN74S SN74xx(STD)	4.75~5.25	0~70
SN74AC SN74AC11 SN74AHC	2.0~5.5	-40~85
SN74HC	2.0~6.0	-40~85
SN74LV	2.0~5.5	-40~85
SN74LVC	2.0~3.6	-40~85
SN74LVT	2.7~3.6	-40~85
SN74ALVC	1.65~3.6	-40~85
SN74ALVT	2.3~3.6	-40~85
SN74AVC	1.4~3.6	-40~85

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Production processing does not necessarily include testing of all parameters. See www.ti.com/sc/logic for the most current data sheets.

#### Little Logic

#### GATE/OCTAL/Widebus<sup>TM</sup>/Widebus+

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	TTL JTT	
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16823	18-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH DUAL OUTPUTS	604
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16833	DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS	610
16834	16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS	612
16835	3.3-V ABT 18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS	613
16841	20-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS	614
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16861	20-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS	618
16863	18-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS	619
16901	18-BIT UNIVERSAL BUS TRANSCEIVER WITH PARITY GENERATORS/CHECKERS	620
16903	3.3-V 12-BIT UNIVERSAL BUS DRIVER WITH PARITY CHECKER AND DUAL 3-STATE OUTPUTS	622
16952	16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS	624
25244	25Ω OCTAL BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS	626
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29821	10-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS	629
29825	8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS	630
29827	10-BIT BUFFERS AND BUS DRIVERS WITH 3-STATE OUTPUTS	631
29828	10-BIT BUFFERS AND BUS DRIVERS WITH 3-STATE OUTPUTS	632
29841	10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS	633

		634
29843	WITH 3-STATE OUTPUTS	034
29854	8-BIT TO 9-BIT PARITY BUS TRANSCEIVER	636
29863	9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS	638
29864	9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS	639
32240	32-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS	640
32244	36-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS	642
32245	36-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS	644
32316	16-BIT TRI-PORT UNIVERSAL BUS EXCHANGERS	646
32318	18-BIT TRI-PORT UNIVERSAL BUS EXCHANGERS	648
32373	32-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS	650
32374	32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS	652
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162240	3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS	659
162241	3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS	660
162244	16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS	661
162245	16-BIT TRANSCEIVER WITH 3-STATE OUTPUTS	662
162260	12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS	664
162268	12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS	666
162280	16-BIT TO 32-BIT REGISTERED BUS EXCHANGER WITH BYTE MASKS AND 3-STATE OUTPUTS	668
162282	18-BIT TO 36-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS	670
162334	16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS	672
162344	1-BIT TO 4-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS	674
162373	3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS	676
162374	3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS	677
162460	4-TO-1 MULTIPLEXED/DEMULTIPLEXED REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS	678
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162541	3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS	686
162601	18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS	688
162721	3.3-V 20-BIT FLIP-FLOP WITH 3-STATE OUTPUTS	690
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6000	TTL CMOS SN74 BiCMOS	Page
Device	Function	
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162827	20-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS	694
162830	1-BIT TO 2-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS	695
162831	1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS	696
162832	1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS	697
162834	18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS	698
162835	18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS	699
162836	20-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS	700
162841	20-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS	701
164245	16-BIT TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS	702
322374	3.3-V ABT 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS	703

#### TTL CMOS SN74 BICMOS

## **FUNCTION**

1G / 2G / 3G

### FUNCTION

1G / 2G / 3G

#### LITTLE LOGIC GATE (AND/NAND/OR/NOR/EX-OR)

									5.15	-		T	echnolo	gy			-	-		
	1777					CI	MOS		BiC	MOS					Adva	nced (	MOS			
Description	No. of Input	Curcuit	Input	Output	Туре	HC	НСТ	BCT	ABT	LVI	ALVT	AC	ACT	АНС	AHCT	2	LVC	ALVC	AVC	AUC
POSITIVE-AND	2	1	8		1G08	+				- 100	1/		88	0	0		0			0
POSITIVE-AND	-	2			2G08					100			260				0	насти	N-DEV	
	l D	1 1			1G00	+				1101			200	0	0		0			To
POSITIVE-NAND	2	2			2G00												0			
	101	1 1			1G32	-				Ittig	(t)		20	0	0		0	DIST	ranyu	10
POSITIVE- OR	2	2	to O veito	Red-cond	2G32	latus	98922	n nee	notelo	uri ee	18	iin.	legist 0	o tegal	ec e	Itue	0	paton	VIIOTE	
		Bernitson	NI Ols	berests	il voolone	(set)	Descri	ale fa	Denni.	nort.		Stapi	and were	louds.	el ni e	defley	100	: Pro		
POSITIVE- NOR	2	2		-	1G02 2G02	_	-	-	-					0	0		0			0
					-		-		-		_		-							
EXCLUSIVE-OR	2	1			1G86									0	0		0			
and the second s		2			2G86												0			

Explanatory notes [Input] SCH : Schmitt-Trigger Inputs [Output] BUF : Buffered Output OC : Open-Collector Output 3S : 3-State Output

[Output] BUF: Buffreed Output OC: Open-Collector Output 35: 3-state Output
Status (): Product available in technology indicated \*: New product planned in technology indicated X: Discontinued

												T	chnolo	gy						
						CI	MOS	ppub	BIC	MOS	DOM:	700	2411	-	Adva	anced (	MOS	aprive	\$1517	
Description	No. of Input	Curcuit	Input	Output	Туре	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	ΓΛ	TAC	ALVC	AVC	AUC
		graph ( )	1100,550	OHMESIC	1G04		100000	HC 10	0000	1000			CIL SCOR	0	0	C. Steiner	0	2001.5		(
		- 1		UBF	1GU04									0			0			-
		1 1		oc	1G06												0			
			SCH		1G14									0	0		0			
					2G04												0			
		2		UBF	2GU04							100	incedes	thult	enofo	sled.	0	1260	2.1 2	
INVERTING		-	Y110000	oc	2G06				-								0			
Mer En Time	1.1m2	sonerhA.	SCH		2G14				1								0			
		1 4			2G04							-					0	10	Nin	Г
	9	100	35	1 8 1	3G04		1 3		1 9	100	10.0	- 11	0.00		7325	100	0	high	Öldug	1
		3		UBF	3GU04															
	1	3		OC	3G06	-											0			
	100	-	SCH		2G14					- 117						-	0			
			SCH		3G14						-					7	0			
		1		. minte	F Junior 20	32	24.774	2 1111	Certain in	Harry S	19.00	Acuthin	-	Married D	1199	1000	24943	Tree	1	
		ALTERNATION AND ADDRESS OF	The same	oc	1G07	No.	Den	and the	- N	170		Conne	an dillo	S. Million	0.00		0	217		
		1	SCH		1G17												0			-
					1G66												0			1
				OC	2G07								-1				0			

NON-INVERTING

Explanatory notes [Input] SCH: Schmitt-Trigger Inputs [Output] Oct Open-Collector Output 35:3-State Output Status O: Product available in technology indicated ': New product planned in technology in the technol

OC

SCH

2G34 2G66

3007

3G17 2G34 3G34

#### LITTLE LOGIC BUFFER/DRIVER

										T	echnolo	gy						
100	MET Bearings			CN	MOS		BIC	MOS					Adva	nced C	MOS			,
Description	Curcuit	Output	Туре	HC	нст	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	, A	LVC	ALVC	AVC	AUC
		38	1G125									0	0		0			
	10	38	1G126					Joseph Company				0	0		0	1 20	N BVID	1
NON-INVERTING		38	2G125					1:00					- 3		0			1
	2	38	2G126												0			1
	D 1	38	2G241					13000							-0	2330		1

Explanatory notes Output 3S:3-State Output R3S: Series Resistor and 3-State output OC: Open-Collector Output Status O: Product available in technology indicated \*: New product planned in technology indicated X: Discontinued

#### LITTLE LOGIC D-TYPE FLIP-FLOP

INVERTING

											23110	T	echnolo	gy	1-7 (427)	1111	onli	aning	Wictims	-10
				tograf	return-o	CN	MOS	2	BIC	MOS	-			10.10	Adva	nced C	MOS			
Trigger	Curcuit	PRE CLR	Output	Q·/Q	Туре	HC	нот	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	2	LVC	ALVC	AVC	AUC
			28	Q	1G79												0			
POS	1		28	/Q	1G80												0			
		В	25	В	2G74												0			

Explanatory notes [Trigger] POS : POSITIVE EDGE, NEG : NEGATIVE EDGE [PRE · CLR] B : Preset and Clear . C : Clear only

[O/Q] B: Q-/Q-Output Q: Q-Output /Q: /Q-Output Status : Product available in technology indicated : New product planned in technology indicated : Discontinued

#### LITTLE LOGIC Data Selectors/Multiplexers

								100 in	1	T	echnolo	gy	177					
				CN	/OS		BiC	MOS	_			100	Adva	nced C	MOS	-	Will real	
No. of Input/Output	Output	Curcuit	Туре	HC	HCT	ВСТ	ABT	LVT	ALVT	AG	ACT	AHC	AHCT	rv	LVC	ALVC	AVC	AHC
2/1	28	1	2G157		+										0			-

Explanatory notes [Output] 2S: Totem Pole Output 3S: 3-State Output OC: Open-Collector Output Status : Product available in technology indicated \*: New product planned in technology indicated : Discontinued LITTLE LOGIC ANALOG SWITCH

	- 1							T	echnolo	gy						
		CN	MOS		BiC	MOS					Adv	anced C	MOS			
Description	Туре	HC	НСТ	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	ΓΛ	LVC	ALVC	AVC	AUC
SINGLE ANALOG SWITCH	1G66												0			0
One of Two Noninverting Demultiplexer with 3-State Deselected Output	1G18												0			
SINGLE 2-CHANNELANALOG MULTIPLEXERS/DEMULTIPLEXERS	2G53												0			
DUAL ANALOG SWITCH	2G66												0			*

Status O: Product available in technology indicated \*: New product planned in technology indicated X: Discontinued

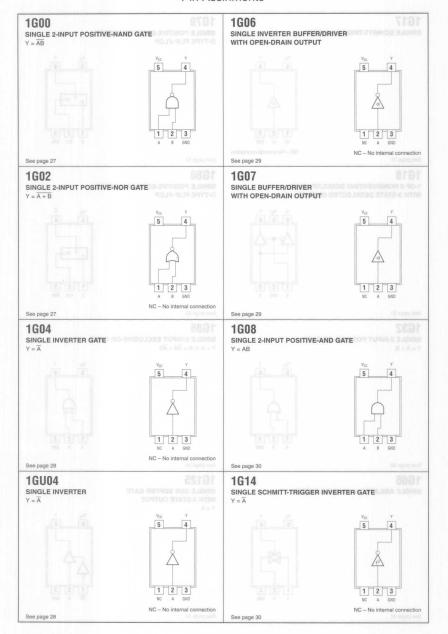
\* How products to technology indicated \* How product plumed in technology indicated X: Discuminated

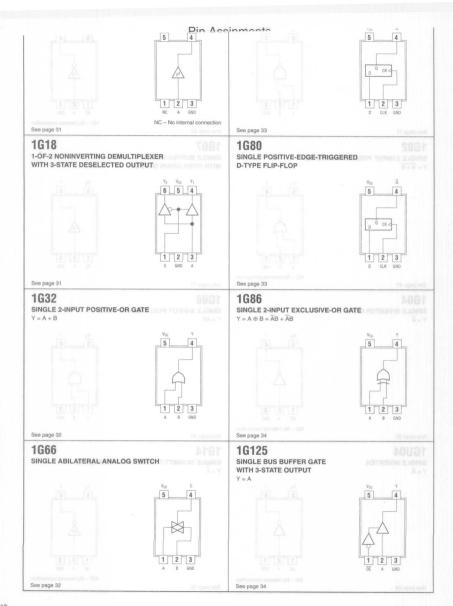
## **PIN ASSIGNMENTS**

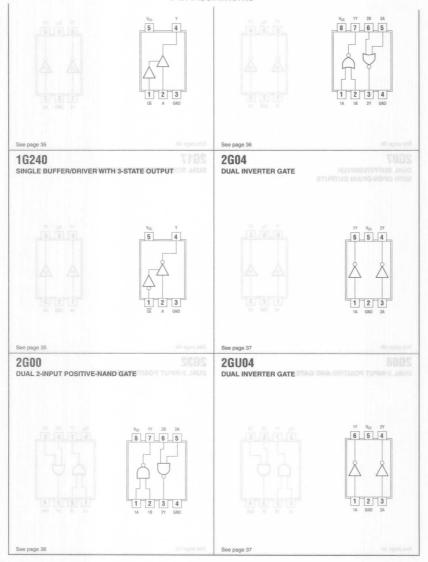
1G/2G/3G

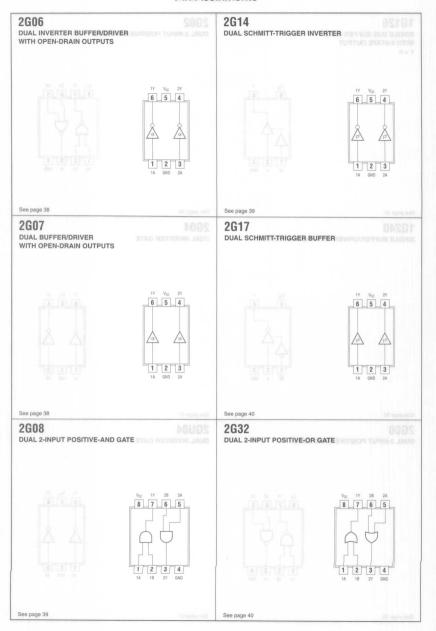
## PIN ASSIGNMENTS

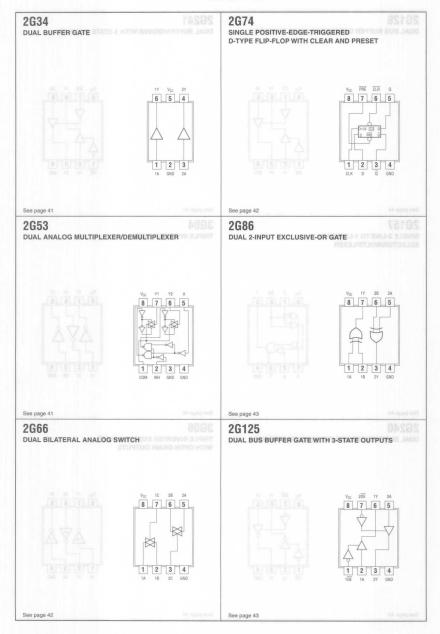
1G/2G/3G

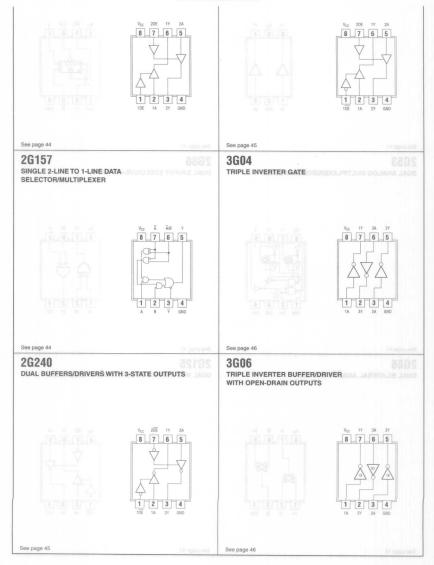


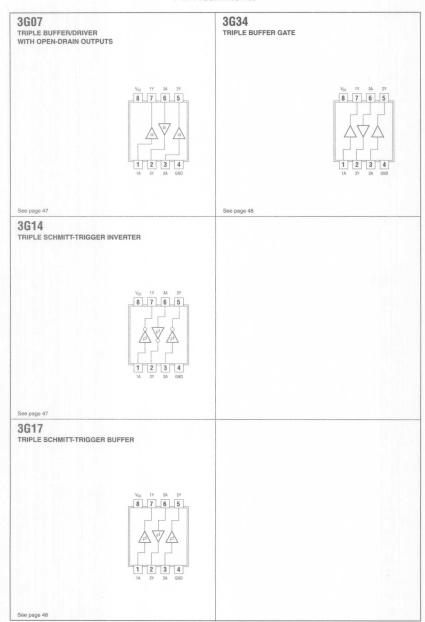


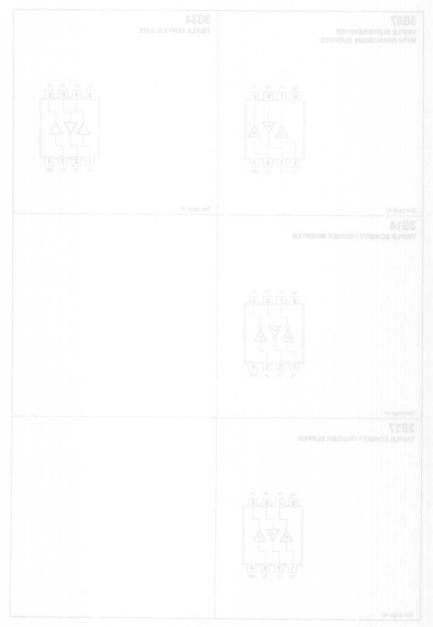












# FUNCTION AND ELECTRICAL CHARACTERISTICS

1G / 2G / 3G

## FUNCTION AND ELECTRICAL CHARACTERISTICS

G / 2G / 3G

#### SINGLE 2-INPUT POSITIVE-NAND GATE

A 1 4 Y

 $\bullet$  Y =  $\overline{AB}$ 

#### **FUNCTION TABLE**

RECOMMEND	ED OPERATING	CONI	DITIONS							
PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
lcc	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	mA
Іон	MAX	-8	-8	-32	-24	-8	-4	-9	-8	mA
In	MAY	9	8	32	24	. 8	- 4	q	8	mΔ

Α.	PUT	OUTPUT
H	н	Man dane
L	X	H
X	L	H

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
tPLH	A or B	V	MAX	8.5	9	- 4	4.7	5.5	8	2	2.2
tphL .	AUID	13	B. IVIAA	8.5	9	4	4.7	5.5	8	2	2.2

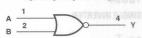
UNIT:ns

#### 1G02

#### SINGLE 2-INPUT POSITIVE-NOR GATE

 $\bullet$  Y =  $\overline{A + B}$ 

#### Logic Diagram (positive logic)



RECOMMENDED OPERATING CONDITIONS

TIEGOTVITALIADI	D OI LIBETING	, 00141	71110140						,	
PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	mA
Іон	MAX	-8	-8	-32	-24	-8	-4	-9	-8	mA
lor	MAX	8	8	32	24	8	4	9	8	mA

#### **FUNCTION TABLE**

	INF	TU	OUTPUT
Γ	Α	В	Y
I	Н	X	made as
Т	X	H	L
1	L	L	H

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
tPLH	A or B	v	MAX	8.5	8.5	- 4	4.5	5.5	8	2.1	2.4
<b>TPHL</b>	AUID	,	WIAX	8.5	8.5	4	4.5	5.5	8	2.1	2.4

SINGLE INVERTER GATE

● Y = A

Logic Diagram



BECOMMENDED OPERATING CONDITIONS

FUNCTION	TABLE
FUNCTION	IABL

RECOMMENDI	ED OPERATING	CON	DITIONS							
PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
lcc	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	mA
Іон	MAX	-8	-8	-32	-24	-8	-4	-9	-8	mA
lou	MAX	8	8	32	24	8	4	9	8	mA

INPUT A	OUTPUT
H	L H

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V		AUC 2.5V	
tPLH	۸	v	MAX	8.5	8.5	3.7	4.2	5.2	7.5	1.9	2.2
TPHL	Α	2.2	IVIMA	8.5	8.5	3.7	4.2	5.2	7.5	1.9	2.2

UNIT:ns

1GU04 of evilland energial origin.

SINGLE INVERTER

Logic Diagram



- $\bullet$  Y =  $\overline{A}$
- Unbuffered Output
- ullet Supply Voltage Renge : 2V  $\sim$  5.5V

**FUNCTION TABLE** 

	894010	INPUT A	OUTPUT
	TOR	H L	L H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AHC	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	mA
Іон	MAX	-8	-32	-24	-8	-4	-9	-8	mA
lou	MAX	8	32	24	8	4	9	8	mA

SWITCHING CHARACTERISTICS

SWITCHING CH	ANACIENIS	165								
PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
tPLH .	۸	v	MAX	8	3	3.7	4	5	2.1	2.4
TPHL	A	1.5	IVIAA	8	3	3.7	4	5	2.1	2.4

### SINGLE INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUT

**Logic Diagram** 



ECOMMENDED OPERATING CONDITIONS

**FUNCTION TABLE** 

	ED UPERATING	-		LVC	LVC	AUC	AHC	Parks I			INPUT A	OUTPUT
PARAMETER	MAX or MIN	LVC 5V	3.3V	2.5V	1.8V	2.5V	1.8V	UNIT		TOR	H	L H
Icc	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA		10.0	10.0	XAM.
Vo	MAX	5.5	5.5	5.5	5.5	2.7	2.7	V				
lor	MAX	32	24	8	4	9	8	mA				

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	ОИТРИТ	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
tPLH .	۸	VIS	MAX	3	4	4	5.6	1.8	2.5
tpui	A	4.0	IVIAA	3	4	4	5.6	1.8	2.5

UNIT:ns

1G07

SINGLE BUFFER/DRIVER
WITH OPEN-DRAIN OUTPUT

Logic Diagram



#### **FUNCTION TABLE**

RECOMMENDI	ED OPERATING	CONE	DITIONS								2000	INPUT	OUTPUT
PARAMETER	7	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT	EVC CBV		1366	H L	H
Icc	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA	mo				
Іон	MAX	5.5	5.5	5.5	5.5	2.7	2.7	V	3-				
lou	MAX	32	24	8	4	9	8	mA	1				

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	оитрит	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
tPLH .	۸	vis	MAX	3.5	4.2	5.5	8.3	1.8	2.5
tPHL .	A	2.5	IVIAA	3.5	4.2	5.5	8.3	1.8	2.5

#### SINGLE 2-INPUT POSITIVE-AND GATE

Y = AB



RECOMMENDED OPERATING CONDITIONS

TILOUIVITALIADI	ED OF ENDATING	, 00141	31110140							
PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	mA
Іон	MAX	-8	-8	-32	-24	-8	-4	-9	-8	mA
lou	MAX	8	8	32	24	8	4	9	8	mA

**FUNCTION TABLE** 

INF	PUT	OUTPUT
A	В	Y
Н	Н	H
L	X	L
X	L	L

SWITCHING CHARACTERISTICS

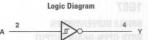
PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
tPLH .	A or B	V	MAX	9	9	4	4.5	5.5	8	2	2.4
tPHL .	AUID	,	IVIAA	9	9	4	4.5	5.5	8	2	2.4

UNIT:ns

#### 1G14 manuald aims

#### SINGLE SCHMITT-TRIGGER INVERTER GATE

 $\bullet$  Y =  $\overline{A}$ 



TURNO TURN

RECOMMEND	ED OPERATING	CUNI	JIIIONS							
PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	mA
Іон	MAX	-8	-8	-32	-24	-8	-4	-9	-8	mA
lou	MAX	8	8	32	24	8	4	9	8	mA

**FUNCTION TABLE** 

INPUT	OUTPUT
Н	L
The same	H

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
tPLH .	^	V	MAX	12	9	5	5.5	6.5	11	2.5	2.5
tPHL .	A	1	IVIAA	12	9	5	5.5	6.5	11	2.5	2.5

#### SINGLE SCHMITT-TRIGGER BUFFER

#### **Logic Diagram**



RECOMMENDED OPERATING CONDITIONS

FIIN	CTIO	NTA	RI	F

	D OPERATING	717000		LVC	LVC	AUC	AUC	100.00		arrise)	INPUT A	OUTPUT
PARAMETER	MAX or MIN	LVC 5V	3.3V	2.5V	1.8V	2.5V	1.8V	UNIT		1316	H	Y H L
lcc -	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA		10.0	10.0	XAM
Іон	MAX	-32	-24	-8	-4	-9	-8	mA				
lou	MAX	32	24	8	4	9	8	mA				

SWITCHING CHARACTERISTICS

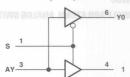
PARAMETER	INPUT	ОИТРИТ	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
tPLH .	۸	v	MAX	- 5	5.5	6.5	11	2.5	2.4
tpui	A	1.0		5	5.5	6.5	11	2.5	2.4

UNIT:ns

#### 1G18

## 1-OF-2 NONINVERTING DEMULTIPLEXER WITH 3-STATE DESELECTED OUTPUT





RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
lcc	MAX	0.01	0.01	0.01	0.01	mA
Іон	MAX	-32	-24	-8	-4	mA
lor.	MAX	32	24	8	4	mA

**FUNCTION TABLE** 

INF	PUTS	OUT	PUT	
S	A	Y0	Y1	
L	L	L	Z	
L	H	H	Z	
H	L	Z	L	
H	H	Z	H	

SWITCHING CHARACTERISTICS

SWITCHING CH	ANACIENIS	1100					
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
tPLH	A	Y	MAX	3.2	4.2	5	9.3
tPHL	A		WAA	3.2	4.2	5	9.3
tPZL	S	V	MAX	3.4	4.6	5.6	10.2
tPZH	3	'	IVIAA	3.4	4.6	5.6	10.2
tPLZ	S	Υ	MAX	3.3	4.9	5.3	12.7
tpu7	3		IVIAA	3.3	4.9	5.3	12.7

### SINGLE 2-INPUT POSITIVE-OR GATE

 $\bullet$  Y = A + B



Δ 1		ICLE SCI	
B 2	>_	4	Υ

RECOMMENDED OPERATING CONDITIONS

NECOMMEND	U UFENATING	CON	SHIDINS							
PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
lcc	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	mA
Іон	MAX	-8	-8	-32	-24	-8	-4	-9	-8	mA
lou	MAX	8	8	32	24	8	4	9	8	mA

**FUNCTION TABLE** 

INF	TU	OUTPUT
A	В	Υ
Н	X	H
X	H	H
L	L	L

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
tPLH .	A or B	v	MAX	8.5	9	4	4.5	5.5	8	2.1	2.4
tPHL .	AUID	1	IVIAA	8.5	9	4	4.5	5.5	8	2.1	2.4

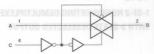
UNIT:ns

1G66

### SINGLE ABILATERAL ANALOG SWITCH



Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC	AUC 1.8V	UNIT
Icc	MAX	0.01	0.01	mA

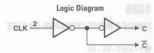
**FUNCTION TABLE** 

CONTROL INPUT (C)	SWITCHI
L.	OFF
H	ON

### SWITCHING CHARACTERISTICS

011110111110 011	THI TO I EITHO	100								
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	
tPLH.	A or B	B or A	MAX	0.6	0.8	1.2	2	0.1	0.2	
tPHL .	AUID	BUIA	IVIAA	0.6	0.8	1.2	2	0.1	0.2	
tPZH	С	B or A	MAX	4.2	5	6.5	12	1	1.1	
tPZL	U	BUIA	IVIAA	4.2	5	6.5	12	1	1.1	
tPHZ	С	B or A	MAX	5	6.5	6.9	10	2.2	2.9	
tPLZ	C .	BUIA	IVIAA	5	6.5	6.9	10	2.2	2.9	

# SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP



### **FUNCTION TABLE**

### RECOMMENDED OPERATING CONDITIONS

TILOOMINICIAD!	LD OI LIDATING	, 00146	,,,,,,,,,,,			_
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	mA
Іон	MAX	-32	-24	-8	-4	mA
lor	MAX	32	24	8	4	mA

		INP	UT	OUTPUT
		CLK	D	Q
		TOHA TOHA	Н	A to XHM
		1	L	L
		no Line	X	Q <sub>0</sub>

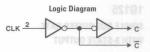
### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	ОИТРИТ	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
fmax			MIN	160	160	160	160
tw	CLK high or le	ow	MIN	2.5	2.5	2.5	2.5
tsu	Before CLK 1	, Data high	MIN	1.2	1.3	1.4	2.2
tsu	Before CLK 1	, Data low	IVIIIV	1.2	1.3	1.4	2.6
th	Data after CL	K ↑	MIN	0.5	1.0	0.4	0.3
tPLH	CLK	0	MAX	4.5	5.2	7	9.9
tPHL .	ULK	u	IVIAA	4.5	5.2	7	9.9

UNIT fmax: MHz other: ns

### 1G80

SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP



RECOMMENDED OPERATING CONDITIONS

HEGOIVIIVIEIVDI	D OI LIMITIAL	CON	711101113			
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	mA
Іон	MAX	-32	-24	-8	-4	mA
lou	MAX	32	24	8	4	mA

### **FUNCTION TABLE**

CLK	D	Q
104	Н	L
1	L	H
L	X	Qn

### SWITCHING CHARACTERISTICS

SVVII GHIIVO G	HANAGIENIO	1103						
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	31
fmax		2.5	MIN	160	160	160	160	8
tw	CLK high or I	wo	MIN	2.5	2.5	2.5	2.5	a
tsu	Before CLK	, Data high	MIN	1.1	1.3	1.5	2.3	1
tsu	Before CLK	, Data low	IVIIIV	1.1	1.3	1.5	2.5	1
th	Data after CL	K ↑	MIN	0.4	0.9	0.2	0	0
tPLH .	CLK	ō	MAX	4.5	5.2	7	9.9	G
<b>TPHL</b>	CLK	u	IVIAA	4.5	5.2	7	9.9	

UNIT fmax: MHz other: ns



### RECOMMENDED OPERATING CONDITIONS

THE O'CHINIST TO								
PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
Іон	MAX	-8	-8	-32	-24	-8	-4	mA
for	MAX	8	8	32	24	8	4	mA

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

### **FUNCTION TABLE**

	INF	TU	OUTPUT
-1	Α	В	Y
_	L	L	L A
- 1	L	Н	H
- 1	H	L	H
- 1	H	H	animal contra

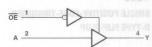
### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC	
					1131	5V	3.3V	0277	1.8V	
tPLH .	A or B	Y	MAX	10	9	4	5	5.5	9.9	
tPHL	AUID		MAX	10	9	4	5	5.5	9.9	
UNIT:ns										

1G125
SINGLE BUS BUFFER GATE
WITH 3-STATE OUTPUT

Y = A

Logic Diagram



### RECOMMENDED OPERATING CONDITIONS

RECUMINENDI	ED UPERATING	CUNI	JIIIUNS							
PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	mA
Іон	MAX	-8	-8	-32	-24	-8	-4	-9	-8	mA
lor	MAX	8	8	32	24	8	4	9	-8	mA

### **FUNCTION TABLE**

INP	UT	OUTPUT
OE	A	Y
L	H	Н
L	L	L
Н	X	Z

### SWITCHING CHARACTERISTICS

SWITCHING CH	ANACIENIS	1163	,						,		
PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
tPLH .	A	v	MAX	8.5	8.5	4	4.5	5.5	8	1.7	2.5
tPHL:	A	Y	IVIAA	8.5	8.5	4	4.5	5.5	8	1.7	2.5
tPZH	ŌE	v	MAX	8	8	5	5.3	6.5	9.4	1.9	2.6
tPZL	UE	1	IVIAA	8	8	5	5.3	6.5	9.4	1.9	2.6
tPHZ	ŌE	v	MAX	10	10	4.2	5	5	9.2	1.7	3.1
tPLZ	UL		IVIAA	10	10	4.2	5	5	9.2	1.7	3.1

### Logic Diagram

### RECOMMENDED OPERATING CONDITIONS

MAX

8 32 24

### LVC 5V LVC 3.3V LVC 2.5V LVC AUC 2.5V AUC 1.8V PARAMETER MAX or MIN AHC AHCT 1.8V 0.01 mA MAX 0.01 0.01 0.01 0.01 0.01 0.01 0.01 -9 -8 MAX -8 -32 -24 -4 mA

### **FUNCTION TABLE**

-	INP	UT	OUTPUT
	OE	A	Υ
	H	Н	Н
	H	L	L
	L	X	Z

### SWITCHING CHARACTERISTICS

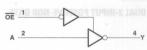
PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
tPLH	A	v	MAX	8.5	8.5	4	4.5	5.5	8	1.7	2.5
tPHL	A	Y	IVIAA	8.5	8.5	4	4.5	5.5	8	1.7	2.5
tPZH	05	V	MAX	8	8	5	5.3	6.6	9.4	1.9	2.5
tPZL	0E	4	IVIAX	8	8	5	5.3	6.6	9.4	1.9	2.5
tPHZ	0E	v	MAX	10	10	4.2	5.5	5.5	9.8	1.7	3.1
tPLZ	UE	4	IVIAX	10	10	4.2	5.5	5.5	9.8	1.7	3.1

UNIT:ns

### 1G240

# SINGLE BUFFER/DRIVER WITH 3-STATE OUTPUT

### **Logic Diagram**



RECOMMEND	ED OPERATING	CONE	DITIONS					
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
Іон	MAX	-32	-24	-8	-4	-9	-8	mA
lou	MAX	32	24	8	4	9	8	mA

### **FUNCTION TABLE**

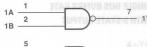
INP	UT	OUTPUT
OE	A	Y
L	H	L
L	L	H
H	X	Z

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
tPLH	۸	v	MAX	4	4.5	5.5	8	1.7	2.5
tPHL	A		WAA	4	4.5	5.5	8	1.7	2.5
tPZH	ŌĒ	v	MAX	5.2	5.4	6.5	9.4	1.9	2.6
tPZL	OL.	,	IVIAA	5.2	5.4	6.5	9.4	1.9	2.6
tPHZ	ŌĒ	v	MAX	4.1	5.2	4.9	9.4	1.7	3.1
tPLZ	UE	7	WAX	4.1	5.2	4.9	9.4	1.7	3.1

### **DUAL 2-INPUT POSITIVE-NAND GATE**

### Logic Diagram





### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
lcc	MAX	0.01	0.01	0.01	0.01	mA
Іон	MAX	-32	-24	-8	-4	mA
lou	MAX	32	24	8	4	mA

FUNCTION TABLE (each gate)

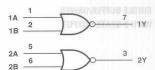
INF	TU	OUTPUT
A	В	Y
H	Н	-L
L	X	H
X	L	H

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
tPLH	A or P	v as	MAX	3.3	4.3	4.8	8.6
tPHL	A or B	2.5	IVIAA	3.3	4.3	4.8	8.6

UNIT:ns

Logic Diagram



### 2G02

### **DUAL 2-INPUT POSITIVE-NOR GATE**

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	mA
Іон	MAX	-32	-24	-8	-4	mA
lou	MAX	32	24	8	4	mA

### **FUNCTION TABLE**

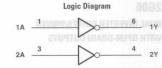
		(each	gate)
Γ	INF	TUT	OUTPUT
1	Α	В	Υ
ı	H	X	XAPL
	X	H	Sal.
	L	L	H

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	ОИТРИТ	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
tPLH	A or D	v	MAX	4.4	4.9	5.4	8.9
<b>TPHL</b>	A or B	,	IVIAA	4.4	4.9	5.4	8.9

**DUAL INVERTER GATE** 





**FUNCTION TABLE** 

(each inverter)

RECOMMEND	ED OPERATING	CONE	ITIONS			_
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	mA
Іон	MAX	-32	-24	-8	-4	mA
In	MAY	32	24	8	Δ	mΔ

PARAMETER	MAX or MIN	LVC 5V	3.3V	LVC 2.5V	LVC 1.8V	UNIT
lcc	MAX	0.01	0.01	0.01	0.01	mA
Іон	MAX	-32	-24	-8	-4	mA
lou	MAX	32	24	8	4	mA

	-	Н	L
	2.5	8.5	XAM

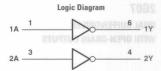
SVVII CHING CH	ANACIENISI	163				_	-	
PARAMETER	INPUT	ОИТРИТ	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	
tPLH .	Δ.	v	MAX	3.2	4.1	4.4	8	
PHL	A	1	IVIAA	3.2	4.1	4.4	8	

UNIT:ns

2GU04

**DUAL INVERTER GATE** 





RECOMMENDED OPERATING CONDITIONS

RECOMMEND	LD OF LINATING	COIVE	71110143			,
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	mA
1он	MAX	-32	-24	-8	-4	mA
lou	MAX	32	24	8	4	mA

FUNCTION TABLE (each inverter) INPUT OUTPUT

CWITCHING CHARACTERISTICS

SVVITCIIIIVG CH	MIMOTERIO	100					
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
tPLH .	۸	v	MAX	3	3.7	4	5.5
tPHL .	A		IVIAA	3	3.7	4	5.5

2606

LaniarDiamon

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
lcc	MAX	0.01	0.01	0.01	0.01	mA
Vo	MAX	5.5	5.5	5.5	5.5	٧
lou	MAX	32	24	8	4	mA

**FUNCTION TABLE** (each inverter)

INPUT	OUTPUT
H	L
200 EV.	H to
AFE AC	

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
tPLH	۸	v	MAX	2.9	3.4	3.9	7.2
tPHL .	А	1	IVIAA	2.9	3.4	3.9	7.2

UNIT:ns

2G07 margett signal

**DUAL BUFFER/DRIVER** 

WITH OPEN-DRAIN OUTPUTS

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

TILOUIVINILIADI	D OI LINATING	OOTEL	71110140			
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	mA
Vo	MAX	5.5	5.5	5.5	5.5	٧
10L	MAX	32	24	8	4	mA

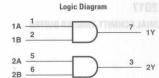
**FUNCTION TABLE** 

		each bui	ner/delver)
	SMB	INPUT A	OUTPUT
	DVI	H	H L ya

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	ОИТРИТ	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
tPLH	Δ.	v	MAX	2.9	3.7	4.4	8.6
tPHL .	A	1	IVIAA	2.9	3.7	4.4	8.6

### **DUAL 2-INPUT POSITIVE-AND GATE**



### RECOMMENDED OPERATING CONDITIONS

HECOMMINICIAN	LD OF LINATING	COIAL	71110143				
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT	
Icc	MAX	0.01	0.01	0.01	0.01	mA	
Іон	MAX	-32	-24	-8	-4	mA	
lor	MAX	32	24	8	4	mA	

<b>FUNCTION TABLE</b>
(each gate)

	(each gate)						
INF	TUT	OUTPUT					
A	В	Y					
H	Н	Н					
L	X	XAY					
X	SEL	XAL					

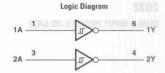
### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC	LVC 3.3V	LVC 2.5V	LVC 1.8V	39.1		
100.00				3.8	0.01	5.1	9	7.5		
TPHL TPHL	A or B	Y	MAX	3.8	4.7	5.1	9	23		

UNIT:ns

### 2G14

### **DUAL SCHMITT-TRIGGER INVERTER**

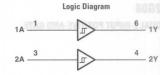


RECOMMEND	ED OPERATING	LUINI	THUNS			
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	mA
Іон	MAX	-32	-24	-8	-4	mA
lou	MAX	32	24	8	4	mA

	(each inverter)					
	INPUT A	OUTPUT				
	100 Han	L				
	M. SE	ZHIA				

SWITCHING CH	ARACTERIS	IUS			281	70/4	SVI	í
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	
tPLH .	۸	v	MAX	4.3	5.4	5.7	9.5	
tPHL .	M	,	IVIAA	4.3	5.4	5.7	9.5	ı

### **DUAL SCHMITT-TRIGGER BUFFER**





TILO OTHER PER	D OI LINTING	00111	71110110			
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	mA
Іон	MAX	-32	-24	-8	-4	mA
lou	MAX	32	24	8	4	mA

FUNCTION TABLE

INPUT	OUTPUT
Н	Н
to Lan	L

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
tPLH .	۸		MAX	4.3	5.4	5.7	9.3
tPHL .	M	1	WIAA	4.3	5.4	5.7	9.3

UNIT:ns

2G32

### **DUAL 2-INPUT POSITIVE-OR GATE**





RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	mA
Іон	MAX	-32	-24	-8	-4	mA
lou	MAX	32	24	8	4	mA

FUNCTION TABLE

INF	TU	OUTPUT
A	В	Y
Н	X	Н
X	H	H
L	L	L

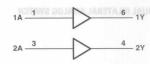
### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
tPLH	A or B	v	MAX	3.2	3.8	4.4	8
tPHL .	AUID		IVIAA	3.2	3.8	4.4	8



### **DUAL BUFFER GATE**





### FUNCTION TABLE

**FUNCTION TABLE** 

RECOMMEND	ED OPERATING	CONE	ITIONS			
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
lcc	MAX	0.01	0.01	0.01	0.01	mA
Іон	MAX	-32	-24	-8	-4	mA
la.	MANY	22	24	0		m A

(eac	h gate)
INPUT A	OUTPUT
Н	Н
1	L

### SWITCHING CHARACTERISTICS

				_	_	_	-
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
tPLH .	۸	Y	MAX	3.2	4.1	4.4	8.6
tPHL .	A		IVIAA	3.2	4.1	4.4	8.6

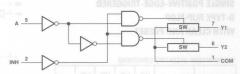
UNIT:ns

# 2G53

### DUAL ANALOG

### MULTIPLEXER/DEMULTIPLEXER

# Logic Diagram



### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	UNIT
Icc	MAX	0.01	mA

### **FUNCTION TABLE**

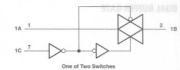
CONTRO	L INPUT	ON
INH	A	CHANNE
L	L	Y1
L	H	Y2
H	X	None

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
tPLH	COM or Y	Y or COM	MAX	0.6	0.8	1.2	2
tPHL .	CONTOLL		IVIAA	0.6	0.8	1.2	2
tPZH		COM or Y	MAX	4.5	5.4	6.1	9
tPZL	INH			4.5	5.4	6.1	9
tPHZ				8	8.1	8.3	10.9
tPLZ				8	8.1	8.3	10.9
tpzH			MAX	5.4	5.8	7.2	10.3
tPZL	А	COM or Y		5.4	5.8	7.2	10.3
tPHZ	A	CONTOL	IVIAA	5	7.2	7.9	9.4
TPLZ				5	7.2	7.9	9.4

### **DUAL BILATERAL ANALOG SWITCH**







PARAMETER	MAX or MIN	LVC	UNIT
Icc	MAX	0.01	mA

# FUNCTION TABLE (each section)

CONTROL INPUT (C)	SWITCHI
L	OFF
H	ON

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
tPLH .	A or B	B or A	MAX	0.6	0.8	1.2	2
tPHL .	AUID	BOLA	IVIAA	0.6	0.8	1.2	2
tPZH	С	A or B	MAX	3.9	4.4	5.6	10
tPZL	· ·	AUID	IVIAX	3.9	4.4	5.6	10
tPHZ	С	A or B	MAX	6.3	7.2	6.9	10.5
tPLZ	C	AUID	WAA	6.3	7.2	6.9	10.5

UNIT:ns

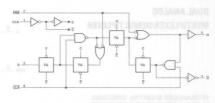
### 2G74

### SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
lcc	MAX	0.01	0.01	0.01	0.01	mA
Іон	MAX	-32	-16	-8	-4	mA
lou	MAX	32	16	8	4	mA

### Logic Diagram



### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
fmax			MIN	200	175	175	80
tw	CLK			2	2.7	2.7	6.2
LVV	PRE or CLR low			2	2.7	2.7	6.2
tsu	Data		MIN	1.1	1.3	1.7	2.9
tsu	PRE or CLR ina	PRE or CLR inactive		1	1.2	1.4	1.9
th			MIN	0.5	1.2	0.3	0
tplH .	CLK	CLK Q		4.1	5.9	7.1	13.4
tPHL.	CLK	u	MAX	4.1	5.9	7.1	13.4
tplH	CLK	ā	MAX	4.4	6.2	7.7	14.4
tPHL	CLK	u	IVIAA	4.4	6.2	7.7	14.4
tplh	PRE or CLR	Q or $\overline{Q}$	MAX	4.1	5.9	7	12.9
tPHL .	THE OF GER	u or u	IVIAA	4.1	5.9	7	12.9

### **FUNCTION TABLE**

	INPUT			OUT	PUT
PRE	CLR	CLK	D	Q	Q
L	Н	X	X	Н	L
H	L	X	X	L	H
L	L	X	X	H†	H
H	H	200	H	H	L
H	H		L	L	H
H	H	L	X	Qn	Q

† This configuration is nonstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

### 2686

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	mA
Іон	MAX	-32	-24	-8	-4	mA
lou	MAX	32	24	8	4	mA

### **Logic Diagram**

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

# FUNCTION TABLE

Γ	INF	TU	OUTPUT
Ī	A	В	Y
Γ	L	L	L
ı	L	H	Н
П	H	L	H
П	H	H	brown Loope

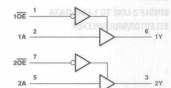
### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	mA
Іон	MAX	-32	-24	-8	-4	mA
lor	MAX	32	24	8	4	mA

# 2G125

# DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS

### Logic Diagram



### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	mA
Іон	MAX	-32	-24	-8	-4	mA
for.	MAX	32	24	8	4	mA

### **FUNCTION TABLE**

INP	UT	OUTPUT
OE	A	Y
L	Н	H
L	L	L
H	X	Z

### SWITCHING CHARACTERISTICS

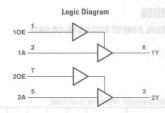
SWITCHING CH	ARACTERIS	1105					
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
tplH .	A	v	MAX	3.7	4.3	4.8	9.1
tPHL .	A	,	IVIAA	3.7	4.3	4.8	9.1
tPZH	ŌĒ	v	MAX	3.8	4.7	5.6	9.9
tPZL	UL	'	IVIAA	3.8	4.7	5.6	9.9
tPHZ	ŌĒ	V	MAX	3.4	4.6	5.8	11.6
tPLZ	UE	,	IVIAA	3.4	4.6	5.8	11.6

### 2G126 immunit sign.l

### **DUAL BUS BUFFER GATE** WITH 3-STATE OUTPUTS



RECUIVINIENDE	D OF ENATING	CONE	THON			_
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	mA
Іон	MAX	-32	-24	-8	-4	mA
lor	MAX	32	24	8	4	mA



**FUNCTION TABLE** 

	1	each L	uner
Г	INP	UT	OUTPUT
I	OE	Α	Y
1	Н	Н	Н
1	H	L	L
-1	1.	X	7

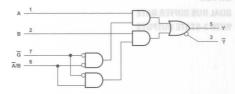
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
tPLH	Λ	v	MAX	3.2	4	4.9	9.8
tphl .	A	1	IVIAA	3.2	.2 4	4.9	9.8
tPZH	0E	v	MAX	3.1	4.1	5	10
tPZL	UE	1	IVIAA	3.1	4.1	5	10
tPHZ	OE OE		MAX	3.3			12.6
tPLZ	UE	1	IVIAA	3.3	4.4	5.7	12.6

UNIT:ns

2G157

# SINGLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER



Logic Diagram

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	11/0	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	mA
Іон	MAX	-32	-24	-8	-4	mA
lou	MAX	32	24	8	4	mA

	INP	OUT	PUT		
G	A/B	Α	В	Y	Y
Н	X	X	X	L.	L
L	L	L	X	L	H
L	L	H	X	Н	L
L	H	X	L	L	H
1	H	X	H	H	1

SWITCHING CHARACTERISTICS

SWITCHING CH	HARACTERIST	rics										
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	NA DAT				
tPLH	A or B	Y or \overline{Y}	MAX	4	6	8	14	3.7				
tPHL .	A UI D	1 01 1	WIAA	4	6	8	14	0.0				
tPLH	Ā/B	Y or \( \overline{Y} \)	MAX	4	6	9	16	1.8				
<b>TPHL</b>	A/D	1 01 1	IVIAA	4	6	9	16	B.E				
tPLH .	G	Y or \overline{Y}	MAX	4	6	8	14	0.0				
tphl.	0	1 01 1	IVIAA	4	6	8	14	3.4				

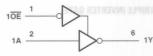
# **DUAL BUFFERS/DRIVERS**

# WITH 3-STATE OUTPUTS



HEGOIVIIVIEIVO	LD OI LIMITIAL	00141	71110140		,	
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	mA
Іон	MAX	-32	-24	-8	-4	mA
Inc	MAX	32	24	8	4	mA

### Logic Diagram



**FUNCTION TABLE** (each buffer)

INP	UT	OUTPUT
OE	Α	Y
L	Н	L
L	L	H
H	X	Z

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
tplH	A	Y	MAX	4	4.6	5.5.	11.3
tPHL	A	,	IVIAA	4	4.6	5.5	11.3
tPZH	ŌĒ	V	MAX	5	5.4	6.6	11.7
tPZL	UE	1	IVIAA	5	5.4	6.6	11.7
tPLZ	ŌĒ	V	MAX	4.2	5.5	5.7	12.8
tPHZ	UE	1	IVIAA	4.2	5.5	5.7	12.8

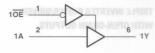
### 2G241

### **DUAL BUFFER/DRIVER** WITH 3-STATE OUTPUTS

BECOMMENDED OPERATING CONDITIONS

TILO O INTIVILIADI	LO OI LINATING	OOITE	71110140			
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	mA
Іон	MAX	-32	-24	-8	-4	mA
lor	MAX	32	24	8	4	mA

### Logic Diagram





### **FUNCTION TABLE**

INP	UT	OUTPUT
10E	1A	1Y
L	H	H
L	L	L
H	X	Z

INP	UT	OUTPUT
20E	2A	2Y
Н	Н	Н
H	O L	L
L	X	Z

### SWITCHING CHARACTERISTICS

SWITCHING CH	AIIACILIIIOI	100			_		_	
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	
tPLH .	А	Y	MAX	3.7	4.3	4.8	8.8	
tphl.	^	1	IVIAA	3.7	4.3	4.8	8.8	
tPZL	ŌĒ	OF.	Y	MAX	3.8	4.7	5.6	9.9
tPZH			WAX	3.8	4.7	5.6	9.9	
tPLZ	ŌĒ	Y	MAX	3.4	4.4	5.8	11.6	
tPHZ	UE			3.4	4.4	5.8	11.6	
tPZL	0E	Y	MAX	3.3	4.1	4.7	8.8	
tPZH	UE	1	IVIAA	3.3	4.1	4.7	8.8	
tPLZ	0E	Y	MAX	3.3	4.2	5.2	12.5	
tPHZ	UE	1	IVIAA	3.3	4.2	5.2	12.5	



RECOMMENDED OPERATING CONDITIONS

RECUMINIENT	EU UPERATIN	G CUN	DITIUN	3	_	_
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	mA
Іон	MAX	-32	-24	-8	-4	mA
lou	MAX	32	24	8	4	mA



FUNCTION TABLE (each inverter)

INPUT A	ОИТРИТ
H	L
L	H

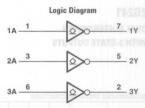
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	ОИТРИТ	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
tPLH .	۸	v	MAX	3.2	4.1	4.4	7.9
tPHL .	М	1	IVIAX	3.2	4.1	4.4	7.9

UNIT:ns

### 3G06

TRIPLE INVERTER BUFFER/DRIVER
WITH OPEN-DRAIN OUTPUTS



### RECOMMENDED OPERATING CONDITIONS

				-		-
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	mA
Vo	MAX	5.5	5.5	5.5	5.5	٧
In	MAX	32	24	8	4	mΔ

### FUNCTION TABLE

(each	inverter)
INPUT A	OUTPUT
H	L

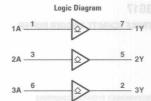
SWITCHING CHARACTERISTICS

SWITCHING CI	HARACTERIS	51165			US I	22.6	
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
tPLH .	Α	v	MAX	2.9	3.4	3.9	7.2
TPHL .		,	MAX	2.9	3.4	3.9	7.2

### 3G07 mangaid signal

## TRIPLE BUFFER/DRIVER

### WITH OPEN-DRAIN OUTPUTS



### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	mA
Vo	MAX	5.5	5.5	5.5	5.5	٧
lo <sub>L</sub>	MAX	32	24	8	4	mA

### **FUNCTION TABLE** (each buffer/driver)

INPUT A	OUTPUT
H	H
L	L

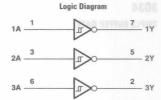
### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	ОИТРИТ	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
tPLH .	Λ	v	MAX	2.9	3.7	4.3	7.8
tPHL A	1	MAX	2.9	3.7	4.3	7.8	

UNIT:ns

### 3G14

### TRIPLE SCHMITT-TRIGGER INVERTER





RECOMMEND	ED OPERATING	COND	ITIONS			
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
łcc	MAX	0.01	0.01	0.01	0.01	mA
Іон	MAX	-32	-24	-8	-4	mA
lou	MAX	32	24	8	4	mA

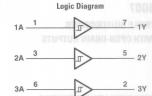
### **FUNCTION TABLE**

INPUT	OUTPUT
Н	L
L	H

SWITCHING CHARACTERISTICS

SWITCHING C	HANACIENIS	1163								
PARAMETER	A Y	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V				
tPLH	Δ.	v	MAY	4.3	5.4	5.7	9.2			
tPHL .	A	1	IVIAA	4.3	5.4	5.7	9.2			
ФИН A Y MAX 4.3 5.4 5.7 9.2										

### TRIPLE SCHMITT-TRIGGER BUFFER



### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
lcc	MAX	0.01	0.01	0.01	0.01	mA
Іон	MAX	-32	-24	-8	-4	mA
lor	MAX	32	24	8	4	mA

### **FUNCTION TABLE**

INPUT A	OUTPUT
H	H
L	L

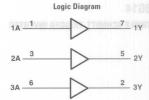
### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
tPLH .	Λ	v	MAX	TBD	TBD	TBD	TBD
tPHL .	М	1	IVIAA	TBD	TBD	TBD	TBD

UNIT:ns

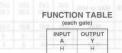
### 3G34

TRIPLE BUFFER GATE



# RECOMMENDED OPERATING CONDITIONS

TILOUTETTE	CO OI CHAINING	00140	1110110			
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
Icc	MAX	0.01	0.01	0.01	0.01	mA
Іон	MAX	-32	-24	-8	-4	mA
lou	MAX	32	24	8	4	mA



### SWITCHING CHARACTERISTICS

			_		-		_
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
tPLH .	Λ	v	MAX	3.2	4.1	4.4	7.9
tPHL .	A	1	IVIAA	3.2	4.1	4.4	7.9

# **FUNCTION**



### GATE (AND/NAND/OR/NOR)

	FIGURE NAME				251/216			Bip	olar			CN	IOS		BiC	MOS	ology		Adv	ance	d CN	ios		_
Description	No. of Input	Curcuit	Input	Output	Device	TTL	2	co.	ALS	AS	u.	P.	НСТ	BCT	ABT	LVI	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC
18018		17300	100		08	X	0	0	0	0	0	0/0	0/0	X		1	-	0/0/0	0/0/0	0	0	OA	OA	0
				oc	09		0	0	0		X	X/-		×			121				1		111	-10
		4		oc	15		X	X	X		150		170											
	2			BUF	1008				$\times A$	OA						100								
POS-AND			SCH		7001							0/-					- 01							
		6	1 42	BUF	808				X	OB	1.70	×/-				-					-		-	-
			-	BUF	1808		0	V	X	X	0	010	10	-		-	- 05	X/O/-	X/O/-	-		OA		
	3	3	-	BUF	1011	-	0	×	OA X	0	0	010	-/0	-	100	-	-	AIOI-	A/O/-	-	-	OA		
	4	2		BOF	21		0		OA.	0	0	0/0	X/O		100			×/-/-	X/-/-		0	OA	0.011	
												-0.0												
TO TACTO	101	2			8003				X						0									
		ALC VE		oc	00		0	0	OA	0	0	0/0	0/0	2		-	-	0/0/0	0/0/0	0	0	OA	OA	0
				OC	01	X	X	- V	X OB			X/-	-/0		-	-	-			-		-		-
	0.0	T TOO	SCH	00	24		X	Α.	OB			CIC	-//		-	-		HOS			-			
			JUH	oc	26	×	6				-				1	-	-	1,010	100				5000	
			-	BUF	37	×	ŏ	0	OA		×		100		100	-	100	S I DUIS	-	-		-	27711	
	2	4		OC	38		ŏ	ŏ	OB		0				100		150	-						
	-		SCH			X	0	X			Ť	0/0	-/0					X/-/-	X/-/-	0	0	OA		
		-		BUF	1000				XA	OA					011									
	11111			OC	1003				$\times A$				1 14					T MOS	0.0					
			SCH	oc	7003							X/-												
				OC BUF	39 804				~	200					100	-								
		6		BUF	1804					OB		×/-		-		-					-			
POS-NAND	-			BUF	1804		0	0	OA		0	0/0	-/0			-	- 51	VIOIO	XIOIO			OA	OA	0
	3	3	-	oc		×		0	X	10	0	Cro	40		-	$\vdash$	170	NON	AICIO			UA	UA	-
			-	BUF	1010		<u> </u>		X						+								1000	
			SCH	1		X	×		-									X/-/-	-/X/-					
			SCH		18		X		-		9				100		10							
					20		0	X	OA	0	0	010	-10		The second			X/X/O	X/X/O			OA		
	4	2		OC		X	×	X	×											-				-
	1			BUF	40	X	X		X		X										1			
				BUF	140			0													10			
		3	SCH	BUF	1020				X								-			-		-		
	8	1	SUH		30		X	×	OA	0	0	X/O	-/0	-	+			VIIV	0/-/×	-	-		-	-
	12	1		38	134		1	×	UA	1	-	710	-70	-		+	-	7/-/ 7	CITA	-			-	-
	13	- 1		-	133			X	0			×/-					1							
																								_
				BUF	32 1032		0	0	0		0	0/0	010					01010	0/0/0	0	.0	OA	OA	0
	2	4	SCH	BUF	7032				X	OA		0/-				-					-		-	-
POS- OR	2	-	SCH	BUF	832			-	OA	ОВ	-	×/-		-		-	-			-	-	-	-	-
		6	100	BUF	1832			-		X		^/-		-	100	-	-		1 0		27	-		-
	3	3	100		4075					1		X/O	-10		100									
				BUF		0	0	0		0	0	0/0	0/0		10		-	X/-/O	X/-/0	0	0	OA	OA	
				OC	28	X	X		X OA					-	-	-	-		-			-	-	-
			-	00	36		10		UA	-	×	×/-		-	-		-		-		-	-	-	-
		4		BUF	128						1	VI.		1	1	1								-
	2			BUF	1002				XA				_	1	-		1	owind -	100 0	-			1	
			SCH		7002	2.4	18			0	120	01-	500	100		100	leg e	05/6:3	HE DAY	100				
POS- NOR				BUF	1036					XA											06			
		6		BUF	805			100	OA			X/-	755		1000	1		and and	-	9 10	177			- 64
				BUF	1805				X			ensile.	2 1000	10	bed.	0.0		in July 1	bit bit	1177	000	9.1	6	
	3	3			27	X	0		OA	0	0	0/0	-/0		1	-	-	X/-/X	XI-IX	-	-	OA		
	4	2	-	-	25	X	-	-		-		-	-	-	-	-	-				1	-		-
	-	2	-	-	4002		-		-		-	X/O	-	-	+	-	-	CYTOME	DO 1.15	1	118	10	-	-
	5	2		-	260		-	0	-	-	0	100	-	-	+	-	-	a Torono	10 7 225	-	110	10	10	-

Explanatory notes [Input] SCH : Schmitt-Trigger Inputs

[Output] BUF: Buffered Output OC: Open-Collector Output 3S: 3-State Output

Status : Product available in technology indicated : New product planned in technology indicated

imes : Discontinued  $\ \blacksquare$  : Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT : SN74HCxx / CD74HCTxx

BCT : SN74BCTxx / SN64BCTxx

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACxx / CD74ACxx

				1016	HE PART			44.1					ios			echn	ology				d CM	00			_
Description	No. of Input	Curcuit	Input	Output	Device	TTL	9	Bip	ALS	AS	LL	CN	HCT	BCT	ABT	TA L	ALVT	AC	ACT	AHC	-	LV CO	LVC	ALVC	AND
	Imput	1 1	. P	1 1	EF	2		U)				1.5		B	A	5	AL							AL	1
EX-OR	2	4	100	oc	86 136	×	OA	0	O	OA		0/0	-/0	0.1	-		100	0/0/0	X/0/0	0	0	OA	OA	_	-
EX-OR	-	-		00	386	^	X		^	^		×/-	130		1		-		1 1			Н			t
								I									100	2				$\perp$			Ξ
			-	OC	266 810		0	-	×	×	-	0/-	-		100		90	X/-/-	×/-/-	-		+	1944	-	t
EX-NOR	2	4		ОС	811				X	×		X					-	70-1-	757-7-						t
1/1		-1570	1 9 7		7266				1			X/O									-	_			I
EX-OR/NOR	2	4	100		135		1	×													2				I
					04	0	0	0	ОВ	10	10	10/0	0/0					0/0/0	0/0/0	10	101	OA	OA	0	Т
		LOWIN		OC	05		Ŏ	0	OA	Ĭ	Ĭ	0/-			100			-/-/0	-1-10	0		OA			İ
			SCH	oc	06 14		0					0.0	010				-	27010	24010			OA	OA	_	Ŧ
			SUR	oc	16		0		-			0/0	0/0					X/0/0	X/O/O	10	0	OA	OA	0	t
INVERTING	1	6	SCH		19		OA										-								İ
	-		-	BUF	1004			-	0	OA	1		1/4	18	-		- 15		4		-	-			+
	I O I	3.000	700	- 00	4049				0			-10			501			1.00							+
					U04						IA.	0/0			90			9		0		OA	OA		1
-	-	8	SCH		619	_	×	-	-	-	+	100	_	_		_	-	1 1000		4		4		_	_
		4			425						T														Т
	-			oc	426							10.0							1 0				~		I
		0.00	+	OC	17	0	0		-		-				-					-		OA	OA		ł
NON- INVERTING	1				34				X			101	111					×/-/-	×/-/-		-				t
	+11-	6		OC BUF	35 1034				OA				1		-					-		4			Ŧ
				OC	1034				0	OF	1		100					1		-		Н			+
		Cox			4050				-			-/0													1
	1 1	6			63		I×			1	-	101			-		-	F		-		-			_
	2	6			31		0																		$\pm$
	4	2				×		-			-	201						×/-/-	×/-/-						Ŧ
	-	-			60	×	0	×			×	×/-						X/-/-	X/-/-		-				+
					53	X																			1
	8	1	-		55 4078		×				-	×/-		-			-			-					+
OTHER	10	1			54	X	×																		Ť
OTHER	11	1	-	oc	64 65			X			×		-				-	X/-/-	×/-/-	$\blacksquare$					T
			-	BUF	800			×	-		+	100	-	+	+		-	×/-/-	×/-/-	+		-	BO	-	+
	12	3		BUF	802							100						X/-/-	×/-/-						1
					7006 7008					-	-	X/- X/-	-		-	-	+		-	-	-				+
	12	6			7074							X/-			1										Ť
					7075							X/-	10												I
-	-	-	1		7076			-	-	1	+	×/-							-	+		-		-	_
planatory n	otes [I	nput] S	CH : Sc	hmitt-Tr	rigger Inp	uts																			
	[0	Output]	BUF : E	Buffered	Output	OC	: 0	pen	-Co	llec	tor (	Output	38:	3-5	tate	Outp	out								
tatus O	Produc	t available	e in tec	hnology	indicated	1	*:	Nev	v pro	odu	ct p	lanned	in tec	hnol	ogy	indic	atec								
×	Discon	tinued	■: N	ot recon	mended	for	new	de	sign	s															
но	: SN74F	HCxx / CI	074HC	CX.					18																
		4HCxx / C																							
HC	T : SN74																								

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACxx / CD74ACxx

### BUFFER/DRIVER(NON-INVERTING)

	100	C) bear	VIII.			В	ipolar			CN	IOS		BICM	Technol IOS		100		Adv	ance	d CMC	S		
Description	No. of Output	Output	Device	Ĕ	53	8	ALS	AS	ш	HC	НСТ	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	2	LVC	ALVC	AVC
		1 2	R		-		4	-	-	-					1	4	<	4	4				A
	4	38	125		OA				0	0/0	0/0	OA/OA	0	HO				0	0	OA	OA	0	
	-	38	126		OA				0		-/0	XA/OA	0	HO		100	1	0	0	OA	OA	0	
	6	38	365		OA			-		010	-/0						1000	-					
	0	38	367	X	OA					010	-10				1		1100	0	10	OA			
		38	241		0	.0	OC	OA	0	0/0	X/O	0/-	OA	HO		X/O/-	X/0/0				-		
		38	244	100	0	0	OC/ OC1	OA	0	0/0	0/0	0/0	OA	OB/ TO/ HOA/ ZO	180	0/0/0	0/0/0	0	0	OA	OA/ HOA/ ZOA	О/НО	
	W7 1	38	455	-			-	-		1		X/a			-	1 10	1000	-		-	_	-	+
	190-2011	38	465		0		×				-	A1-	-		+	-	1000			-			+
		38	467		×	100	×	-							-								-
		38	541		ô		0/01		0	0/0	0/0	OA/-	ОВ	HO	1	-/-/0	-/-/0	0	0	OA	OA		+
		38	656	-	10		0/01		0	0/0	010	UA/-	OB	HU	-	XI-I-	X/-/-	V	0	UA.	OA		+
		35	747				×							1	-	V/-/-	V/-/-						+
	8	00	757				. ^	-				010				-	1000		2	-		200	+
		OC						0				0/0			1		(20.0)		100				+
		38	760				0	0				0/-			-		7.00						-
		3S 3S	1241				-										10.60						-
							OA										100						+
	140	R3S	2241			100						0/-	0										
		R3S	2244						X	-		0/-	OA								OA		
		R3S	2541				0					Lucia I						2					
		35	25241									X/-					1100		- 51		24		
		3S	25244									0/0					Long		- 50				П
NON-	R 784	oc	25757				1			-		X/-									400	0	Т
INVERTING	W W	oc	25760				17:31			100		×/-					19940	1					
	17 140	38	827							1 47			0			X/-/-	X/-/-	-	3		=OA		$^{\dagger}$
	10	R3S	2827									OC/-	0				Torse	100					+
	1	38	29827				0					OB/-					1100	100					_
	11	R3S	5400										OA								756		+
	100	3S	5402										OA				71			_	7.5		+
	12	R3S	16903										UH.		+	_				-		нО	-
	-	38	16241					_					OA	HO	+		×			-	H×A	HO.	+
		38	16244					F					OA/ H	1	но	0	0	0	0		OA/ HOA/ ZOA	OA/ HO	(
	16	35	16541										OA	HO			0	0	0		HOA	×	
		R3S	162241											HO			1000	1					
		R3S	162244										0	OA/HO	но		cos	251	80		OA/ HOA	нО	Г
		R3S	162541											HO			Ped	1				×	
		38	16825										0				0	1				HO	1
		R3S	162825										0				1000				100		1
	18	38	16835											но			1000		- 60	H		HO HO	(
		R3S	162835														5882	N. C.	63			0/	Г
		38	16827														-					HO	
	20		16827	400	-	200	0	-	1	200	1.00	Character and	0		HO	Distance.	0	2,0	2000	503	and the	HO	1.5
		38		-					-				OA		HO							HO	
	32	3\$	32244			.0		111		1000	1000	1000		O/HO	HO	HOUR YOU				100	O/HO	HO	1

Explanatory notes [Output] 3S: 3-State Output R3S: Series Resistor and 3-State Output OC: Open-Collector Output Status O: Product available in technology indicated \*: New product planned in technology indicated

X: Discontinued : Not recommended for new designs

HC : SN74HCxx / CD74HCxx
HCT : SN74HCxx / CD74HCTxx
ECT : SN74HCxx / CD74HCTxx

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACxx / CD74ACxx ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

7 10		38	240	10	0	OA1	OA	0	0/0	0/0	0/-	OA	OA/HO		0/0/0	0/0/0	0	0	OA	OA/ ZOA	
Design		38	456						100		X/-		100	353.0	10.0	10.00		-			
		38	466	×		X		111						10	100						
		38	468	X		X		-													
		38	540	0		0/01		×	0/0	0/0	OA/-	0	HO		-1-10	-1-10	0	0	OA	OA	
		38	655	-	-					0.0		-			X/-/-	X/-/-	-	-	-		
	8	38	746			×									7/1-1-	VI-1-					
		OC	756		-	X	0				0/-					1175					
		OC	763	-	-	^	X				OV.										
		38	1240	-	-	×	^		_		_					-					
NVERTING		R3S	2240	-	-	×					0/-	OA		-	-	191		-	-	-	
		R3S	2540	-	-	×	-		-		O/-	UM	-	-		-	-		-		
		3S	25240	-	-	X	-				×/-			-		1110			-		
		OC	25756	-	-		-	-			×/-	-		-	-	-	-	-	-	-	
		38	828		-		-		-		^/-	-		-	X/-/-	×/-/-		- 11	-	OA	
	10	R3S	2828	-	-						×/-		-		2/-/-	A/-/-	-	-		UA	
	10	3S	29828	-	-	-			-					-							
	11		5401	-	-	-					XB/-	-		-							
		R3S			-							0				100					
	12	R3S	5403	-								0							-		-
		38	16240									OA	O/HO	HO	×	0	0	0		HOA/ ZOA	HO
	16	38	16540		13.6				8			OA				×	0	0		HOA	×
		R3S	162240							1000	954.11		O/HO			17.535		110		122	
		R3S	162540													1779					×
	20	38	16828						1.00							×		1.5		11	×
	32	38	32240						1				0			11100		1		600	
1.901					_			_								1000					
AND	8	38	230			×	×														
NON- INVERTING	NCS.	ос	762			1	×	2								1					
- B	W. 786 I	38 1	16830		_											1 110				-	H*
	1-2	-																			HO/
	NO.	R3S	162830			711		1.0								885	197	3			HSO
		38	16344													1111					HO
ADDRESS		38	16831																		HO
DHIVERS	1-4	38	16832										-			- Van					HO
	1-4	R3S	162344																		HO
		R3S	162831					-								1000					O/HO
		R3S	162832																		HO

Explanatory notes [Output] 3S: 3-State Output R3S: Series Resistor and 3-State Output OC: Open-Collector Output Status : Product available in technology indicated :: New product planned in technology indicated

X: Discontinued III: Not recommended for new designs

HC:SN74HCxx / CD74HCxx
HCT:SN74HCxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT1xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACXx / CD74ACXx ACT : 74ACT1xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACXx / CD74ACXx

Description No. Outpi				-		10.1	olar		1001	- 01	MOS	-	DIO	Techno	ology	1		6.4		d CM	00		_
Description	No. of	Output	Device	-								-			H	1	. F				1000000	l v	0
Description	Output	Output	5 5	I	3	S	ALS	AS	Œ.	HG	HCT	BCT	ABT	F.	ALVT	AC	ACT	AHC	AHC	3	LVC	ALVC	AVC
		38	226	-		×		-				-						1000					
		100				-														0.0			
		38	440		X			1													18/34		
	-	OC	441		X						-							1					
	4	3S 3S	442 443		0				-						-					-			
		3S 3S	443		X	+-			-			-			-			-			9		
		OC	448		X		-			-	-	-	-	-				-		-	4000	-	Н
	145.0	38	449		×							-											
	WOH	38	243		0		OA	×	X	-10	-/0							1000		255			
	VA CHS	38	1243		Ĭ		UN			, ,	1												
		38	245		0		OA/ OA1		0	0/0	010	010	OB/ HO	OB/ H		0/0/0	0/0/0	0	0	OA	OA/ HOA/	О/НО	
	10	38	470			1	-						-	0		×/-/-	X/-/-	1000			ZOA		
	- F./H	38	472													X/-/-	X/-/-						
	-	38	474			10										X/-/-	X/-/-						
	A THE	38	543						0			0/-	OA	HO		X/-/-	0/-/-			100	OA		
	100	oc	615				×													10			
	OB	ос	621		×		OA/ OA1	×	×									100					
		38	623		0		OA	X	X	0/-	0/-	0/-	0			X/-/O	0/-/0						
		3SOC	639		X		OA	×										-		100			
		ос	641		0		OA/ OA1	0		-										100	EXIL		
		38	645		0/		OA/ OA1	0	-	0/-	0/-									111	Code		
		38	646		0		OA			0/0	0/0	0/-	O/ OA	но		X/-/O	X/-/O	200		10	OA	1010	ic
		oc	647		×		×						UA							50		-	-
		38	652		0		OA			0/0	0/0	0/-	O/ OA	HO		X/-/O	01-10	1			OA		
111		3SOC	654		X		0													23	1		
NON-		38	657						0			×/-	OA			X/-/-	X/-/-						
HATHING	8	38	659							X/-	×/-										1		
		38	665							X/-	X/-												
	-	3S 3S	852 856			-	10	×								X/-/-	X/-/-	1		88			
		38	877			-		X	-				-			X/-/-	×/-/-	0.00		40	1		
		3S	899	-	-	-	-	×	-	-		×/-	-			X/-/-	X/-/-	-		-	1 9		
	CON.	3S	1245			-	OA			-	-	X/-	-		-	-	-	-	-	35		-	
		38	1645		-	+-	OA	-	-	-	-	-	-		-			-		-	il and	-	-
		38	2245			+	CA		-	1	-	0/-	O/RO	HO				1000		100	ROA		
		38	2623				×					-	Circo	110	100			-			-		
		38	2645					X							1						11		
		38	2952							J V		×/-	OA	HO				10010		-	OA		
		38	25245									01-	OH							COR			
		38	25543									X/-					1-10-11	107	1	no.			
		38	25621									X/-						100			00.401		
		3S 3S	25623			-		-	-			X/-						100					
		3S	25641 25646			-			-			×/-	-		-			-	-	100	0.	-	-
		38	25647		-	+	-	-	-	1	-	X/-	-	-	-			-	-				
		38	25652		-	-	-	-	+		-	X/-	-		-			-		100	-	-	-
	W V	38	25654					-				×/-	-			-		-		-	-		
	263	38	3245									1		×				-			COA		
		38	4245							1										89	OA/ COA		
	-	3SOC	833										0			X/-/-	X/-/-						
	8+1P	3SOC	853										0		-	X/-/-	X/-/-	No.	0			-	
	07.15	3SOC 3SOC	29833 29853				×					X/-											
	-	3800	29853 863		-	-	X	-	1	15757		X/-	0			×/-/-	×/-/-	-	185	1	OA		-
	9	38	29863			-	0	-	-	-	-	OB/-	0	-		VI-I-	VI-I-	1			CA		
	9X4	38	16409			bed	SIL/	100	101	cond o	Danie	1150	Dong V	134.77	130	Rodon y	dents	10.4	Habit	0.0	Product	HO/	211

Explanatory notes [No. of Output] +P: With Parity Bit

[Output] 3S: 3-State Output R3S: Series Resistor and 3-State Output

OC : Open-Collector Output 3SOC : 3-State Output / Open-Collector Output

Status : Product available in technology indicated : New product planned in technology indicated

X: Discontinued : Not recommended for new designs

HC: SN74HCxx / CD74HCxx HCT: SN74HCxx / CD74HCTxx

BCT : SN74BCTxx / SN64BCTxx

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACxx / CD74ACxx

	(NON-INVERTIN	

		2007	Garage Co.	-		Bip	olar			CN	MOS		BiCI	Techn	orogy		_	Ad	vance	d CM	os		
Depositeli	No. of	Outnut	Device			Uip		1.			1	-	1		TE	T. I	-				1 100 100	0	1
Description	Output	Output		I	53	03	ALS	AS	L	H <sub>C</sub>	HCT	BCT	ABT	LVI	ALVT	AC	ACT	AHC	AHC	LV	LVC	ALVC	AVC
		38	16268																			X	
		38	16269													1 2				25		HO/ HROA	(
	12/24	38	16270														2	1		365		HO	
	12224	38	16271																	36		HO	
		38	16272															100		2.5		X	
		38	162268					-										1		90		HO	
	16/32	3S 3S	162269 162280			-		-	-									-	-	-	-	HGO	-
	10/32	33	102200	-	-		-	-										-		-00	OA/	HGO	-
		38	16245										OA/ HO	OB/ HOA	но	0	0		0	25 0x 31	HOA/ HROA/ ZOA	HO/ HRO	0
	W.	38	16334												100						LON	O/HO	1
	45.CH	38	16470					11					0		10		×			100			
	8.5	38	16543				-			-			0	но		×	0	4		1	0/	но	$\Box$
	100													- HO						100	HOA	nO.	
	16	3S 3S	16623 16646										0	-		×	.0						
	875				-	-							0	HO		×	0	1			HOA	HO.	1
	-	3S 3S	16652										0	HO		0	0				HOA	×	
		-	16952	-	-	-		-			-		0	HO			0	-			HOA	HO	
		R3S	162245	5									O/HO	OA/ HO	HO		1			00	RO.		
		R3S	164245			100					1	1	1	100	12			100		1600	-	0	H
		R3S	162334												1.74					-		O/HO	1
	16X3	38	32316										HO										
	18X3	38	32318									T A	HO		1 19			1900		83			
		38	16657										0				0						
NON-	16+2P	38	16833		16.1	1			1.55				0				X	O US		22			
INVERTING		38	16853									22	0				×						
		38	16472													X							
	40.1	38	16474			100											×			.03			
		38	16500										OB	HO						OAB		HO	
		38	16501								1		0	HO						50		HO	11
		38	16525															1				HO	
		38	16600	)									0					1				HO	
		38	16601	1		1-13							0		HO			den		130	1 -	HO/ HRO	
	18	38	16834															10		100		0	1
	10	38	16863										0				0					HO	
		38	16901															The			HO	HO	
		R3S	162500					1.5					0					0					
	1	R3S	162501								100		0	100									
	100	R3S	162525																			HO.	
		R3S	162600	)																			
	AC)	R3S	162601						U	1.8			0					100		100		HO/ HRX	
		R3S	162834															1		100		0	
	18/36	38	16282																			HO	
	10/30	R3S	162282	2																1 5		HGO	
	1	35	16836																	20		H.	
	20	38	16861					1									0			100			
		R3S	162836																			O/HO	
	32	38	32543										HO.					-		100			
	-	38	32952	+		+		+	-			-	×					-		100	O/ H		-
	36	38	32245						1				HO	HO				1		100	OA	HO	
	30	38	32500										×					100		20			
	1 2 0	38	32501	П									HO.									HO	

Explanatory notes [No. of Output] +P: With Parity Bit

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AC : 74AC11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACxx / CD74ACxx

ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACTxx / CD74ACTxx

и тольном и солинотия

: SMCRBOTX ( PREVENTE )

- SMCRBOTX ( Prededict swellable in reduced-online advanced CRAS | 17000 Servica) ( StratoCx ( CDT WCKs)

- SMCRRSSON Shoulder swellable in reduced-online advanced CRAS : 17000 Servica) ( DH-GROTX / CD-GAOTX

- SMCRRSSON Shoulder swellable in reduced-online advanced CRAS : 17000 Servica) ( DH-GROTX / CD-GAOTX

- SMCRRSSON Shoulder swellable in reduced-online desired crass services of CRAS CRASS ( CRASS C

			200			Die	olar		-	CN	108	-	PICI	MOS	nology		-	Ad	vance	d CM	108	_	_
Description	No. of	Output	Device	E	-			10	72		1	-	10.		TE	- 12	-				_	5	AVC
	Output	5		F	3	00	ALS	AS	II.	HC	HCT	BCT	ABT	7	ALVT	AC	ACT	AHC	AHC	3	LVC	ALVC	1
		38	242		×		X	×	×	X/-	X/-					107							
		3\$	446		×											0.191							
	4	3\$	1242				X				T.V.	78081			-	0.1122	1 11						
		R3S	2242				X				100	10.11	200	2.3	200	1001	8						100
		38	544				-		×			X/-				X/-/-	X/-/-						1
		38	471			_			-			1.0			1	X/-/-	X/-/-						+
		38	473			-		-							_	X/-/-	X/-/-	-	_			+	+
		38	475	-		-	_	-	-			200			100	X/-/-	X/-/-	-				_	+
		OC	614			-	×	-	-			100			-	VI-1-	Alter	-				-	+
		3\$	620	-	×	-	OA	×	×	X/-	X/-	X/-	0		1	X/-/-	X/-/-	-	-			_	+
		OC	622		×	-	X		Î	VI-	~/-	VI-	-	27 127	-	VI-I-	VI-1-	-	-		_	+	+
				-		-		^	1			-	-		-			-	-	-	-	-	-
		3SOC	638		×	1	OA/ OA1	OA						1000		1874				- 6			
				-	-01	-			-	-				-	-			-	-	-	_	_	+
		38	640	-	0/	1	OB/ OB1	0		010	X/O	01-	-0			×/-/-	×/-/-	1		-	-	1	1
					01		OA/	-		-					1			-	-			-	-
		oc	642		0/		OA/	×				×/-											
		38	648		0	-	OA	0	-	X/-	×/-	×/-			+	×/-/-	X/-/-	+	-	-	IO Jay	19.19.10	100
		OC	649		X	-	X	1	-	~J*	11.	1.		-	-	VI-1-	01-1-	-	-	-	100		-
		38	651		X	-	OA	V		×/-	×/-	×/-	0		-	×/-/-	X/-/O	-	-	-	_	-	-
	8	3SOC	653		×	-		X	-	\/-	A/-	VI-	-0		-	VI-1-	N-10	-	-	-	-		-
		38	658		_ ^	-	0	-	-	207	221	-			-			-	-	-	-	-	+
		3S	664		15	-		-		XJ-	X/-			F 1	-		- 0	-	-	15.0		-	
						-	-	-		X/-	X/-	-			-	-		-	-	-			-
	8+1P 9 10 16	38	1640		1	-	×		-							111	- 2		-	-			-
		38	2620				X	-								1111							
		38	2640					X				X/-				2 184F	0			-			
INVERTING		38	2953		1100							X/-	81		0.1	1816	100		13				
		35	25620		200						100	X/-				(1011	0						
		38	25622		- 100							X/-	5			1000	1 51						
	A.S	38	25640		11111						75.7	X/-				6.1612	1 0			- 9			
		38	25642		70.7			11		1.1	35.71	0/-	23.7	N. T.		1016	9.						
		38	25648		990						20.21	X/-				1372	1 57						
		35	25649		11.5							X/-				1012	12						
		38	25651		200					115	351	X/-				1160	100						
		35	25653		10.00					427	797	X/-				1775	0.0						
	III DA	3SOC	834		363											X/-/-	X/-/-		10				
	0.40	3SOC	854											Jan 1		X/-/-	X/-/-						
	8+1P	3SOC	29834				×					X/-					100						
		3SOC	29854				0					0/-	18			1710	100						
		3\$	864		447								120			X/-/-	X/-/-						
	9	38	29864		75.00		×					OB/-				1100	10						
		35	862		4-0											×/-/-	X/-/-						
	10	38	29862				×					XB/-		100		100			100				
		35	16471									-	1130			100	-						
		38	16544										100	AXI.		1870	×						
		38	16620										150			×	X						
		38	16640							-2.31			0	6.		×	X						+
	16	35	16648							100			-	121	_		×				_	_	10
	100	38	16651		4445											1000	0						-
		38	16862														-						+
		38	16953							122			110			THE SALE	×					1	-
		38	16475					-							1	10000	×	-		-		+	+
	18	38	16524		353.7	-		-								1111	^		1	-		HO	-
	.0	38	16864			-		-	-						1	100	×	-	-	-		HO	+
		00	10004	-	1000	-	-	-	_						-	111111	_ ^	_	_	_	_	-	_
		38	643		×	-	×	I×	-	X/-	×/-				-	×/-/-	1 4//	-		-	_		-
		OC OC	644			-				XI-	X/-		10			X/-/-	X/-/-						
NON-		00	758		×	-	×	X		1					-	12000	100						
INVERTING	8	OC	758 759				X	X								1000	- 0						
								1 8															

		35	643	X	X	X	X/-	X/-	1.0		X/-/-	X/-/-	11.0			
NON-		OC	644	X	X	X	THE S			×1.1	1,000	101				
INVERTING	8	OC	758		×	X					10000					
/INVERTING		OC	759			X					1000000	- 53.				
		3S	7340				X/-									

Explanatory notes [No. of Output] +P: With Parity Bit

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HCT : SN74HCxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACxx / CD74ACxx

### J/K FLIP-FLOP

							mond	nib.	11						Tecl	nnolo	ogy						
		200		0	10		10	Bip	olar	1000		CN	los	BICM	os			land.	Adva	nced	CMOS		
		В	28	В	107	0	OA					X/O	-/0	1×13			1.54	17115		100			
NEG	2	В	28	В	112		OA	OA	OA		0	0/0	-/0	100 10			X/-/O	X/-/O		00		OA	
		В	28	В	113		X	X	X		×	X/-			1.50								
		В	28	В	114		X	×	×		×	×/-		100	1.12	101							
	4	B	28	0	276	X									110								

### D-TYPE FLIP-FLOP

			-	-	_	-			_		_			-			hnolo	gy			-				_
		PRE		Q		_		Bip	olar	_		CN	IOS	-	BICN	NOS			_		anced	CMOS			_
Trigger	Curcuit	CLR	Output	/Q	Device	E	3	00	ALS	AS	th.	HC	HCT	BCT	ABT	5	ALVT	AC	ACT	AHC	AHC	2	LVC	ALVC	AWA
	2	В	28	В	74	X	OA	0	OA	OA	0	0/0	0/0					0/0/0	0/0/0	0		OA	OA	-	
		C	28	В	171		X									1111		-	1000			-			
	4	C	25	В	175	X	0	0	0	OB	0	0/0	-/0					0/-/0	X/-/O			OA			+
			28	В	379	-	X	-	-	-	X	X/-	-					X/-/-	X/-/-			- CA			+
		C	28	Q	174			0	0	0			-/0				-	X/-/O	X/-/O	0	0	OA		-	+
	6		28	0	378		10	1	-	~	X	X/-	40		-	-	-	X/-/-	X/-/-	- V	-	UN			+
		C	28	Q	273		ŏ	-	0		X	0/0	0/0	-	0	но	-	X/-/O	XI-10	0	0	OA			+
		-	38	Q	374		ŏ	0	OA	0	0	0/0	0/0	0/-	OA	HO	-	X/0/0	0/0/0	ŏ		OA	OA	HO	$\vdash$
		_	28	Q	377		lŏ	1	CA	0	OA		0/0	U/-	OA	nO.	-	X/-/-	X/-/-	10	0	CA	UM	no.	+
	1	_	3S	Q	478		10	-	-	-	UA	OVC	CVO	-	UA	-	-	XI-I-	X/-/-	-	-	-		-	$\vdash$
			3S	/Q	534		-	-	0.0	17	1	5775	37.65	200	~	-	-			-	-	-	-		-
			38	/0	564		-	-		X	X		X/O	X/-	OA	-	-	X/0/0	X/O/-	-	-	-	-		-
		-	38	Q	574		-	-	OB	-	X		X/O	X/-	-			X/O/-	X/O/-	-	-	-	-		4
			3S 3S	0				_	OB	0	0	0/0	0/0	0/-	OA	HO		XIOIO	XIOIO	0	0	OA	OA		╙
					575		-		OA																
			38	/Q	576				OB										110000		100				
	8		38	/Q	577				OA										DOCUME.		200				
			38	Q	825					OA								X/-/-	X/-/-						
			38	Q	826					X		100						X/-/-	X/-/-		100				
		C	38	Q	874				OB	0								X/-/-	X/-/-		100				
		P	38	/Q	876				OA	0															Г
		C	38	Q	878				X	X									17291		. 110				т
		C	38	/Q	879				XA	X									195581		100				1
			38	Q	4374				-	OB									10.701		100				+
			38	Q	29825				×	X				0/-					109-019		12				_
POS			38	Q	29826		+		X	X				X/-					17.00						+
		C	38	Q	823				-	OA				1	0			X/-/-	×/-/-	-		1	OA		+
		C	38	/0	824		-	_		XA					-	11	-	X/-/-	X/-/-	1	-	-	UA.	-	+
	9	C	38	Q	29823				×	X				X/-				74-1-	751-1-	_		-		-	+
		C	38	/Q	29824		_		×	X				X/-	_	1		_	10/1991	_	300	_			+
			38	Q	821		+	-	-	OA				100	OA	+		X/-/-	X/-/-	1	1	1	OA		+
			38	/0	822		+	+	-	X				-	UM	-	-	X/-/-	X/-/-	-	-	-	OM	-	+
	10		38	Q	1821		-	-	-	×	-			-		-	-	747-1-	747-1-	-	-	-		-	+
	10		38	Q	29821		+-	-	0	Ŷ	-		-	0/-	-	-	-	-	18310	-	-	-	-	-	+
		_	38	/Q	29822		-	-	×	Ŷ	-	-	-	X/-	-	1	-	-	1000	-	-	-	-	-	+
		-	38	Q	16820		+-	-	1	-	-	-		100	-		-	-	-	-	-	-		HO	+
	10X2		38	Q	162820		-	-	-		-			-	-	-	-	-	-	-	-	-		HO	+
	-			_	-	_	+-	-	-	-	-	-		-		-	-			-	-	-	177.41	-	+
			38	Q	16374		-	-	-	-			-	19.8	OA	HO	HO	0	0	0	0	1	OA/ HOA	HO	1
	16		38	/Q	16534	-	+	-	-	-	-	-	-	-		-	-	-	l x	-	+	-	n A	-	+
			3S	Q	162374		-	-	-	-	-	-	-	-	-	HO	-	-	^	100	-	1	-	HO	+
		С	38	Q	16823		+	-	-	-	-	-	1000	-	Over			×	0.0	-	+	-			+
	18	C	38	Q	162823		+	-	1		-		-		OVOH	-	-	X	0	1	-	-		HO	+
		0	3S	Q	16721		-	-	-	-	-	-	-	100	OA	-		-		-	-			1100	+
			38	Q			-	-							- 0		1110		- 14	-	-	-	-	HO	1
	20		38		16821							1111		1.00	10	136	HO	L spole	×		7.7			HO	1
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			38	Q	162821		_			_									771					×	1
	22		38	Q	16722														DOD BY	10	00	155	130		
	32		38	Q	32374												HO						HOA	HO	
	-		38	Q	322374											HO									1

Explanatory notes [Trigger] POS: Positive edge NEG: Negative Edge

[PRE · CLR] B : Preset and Clear C : Clear Only
[Output] 2S : Totem pole Output 3S : 3-State Output

[Q-/Q] B:Q-/Q-Output Q:Q-Output /Q:/Q-Output

Status : Product available in technology indicated \*: New product planned in technology indicated

X: Discontinued : Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT : SN74BCTxx / SN64BCTxx

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACxx / CD74ACxx

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AD									Ĭ				1					7.07	201						İ
-	T 4	28		0	75	IV	10					LV/O	LVIO					LOLL			-				-
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							-	-	OA	OA		VIO	VIO	V/	OA			VIOL	VIOL		-	-	-		+
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Explanatory notes [Type] S-R: S-R Latch AD: Addressable Latch BIS: Bistable Latch

R-B : Read-Back Latch D : D-Type Transparent Latch

[PRE · CLR] B : Preset and Clear C : Clear Only [Output] 2S: Totem-Pole Output 3S: 3-State Output

 $[Q\cdot/Q]\quad B:Q\cdot/Q\text{-Output}\quad Q:Q\text{-Output}\quad /Q:/Q\text{-Output}$ 

Status : Product available in technology indicated \*: New product planned in technology indicated

X: Discontinued : Not recommended for new designs

HC : SN74HCxx / CD74HCxx

HCT : SN74HCxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

						900000		1										chnolo	gy							
		Acres.	5	100					Bipi	olar			CM	os		Bit	CMOS				Adv	nced	CMOS			
Input Type	Output Type	No. of Bit	CLR	Shift	Output	Device	I	rs	S	ALS	AS	ш	HC	нст	BCT	ABT	LVI	ALVT	AC	ACT	AHC	AHC	LV	LVC	ALVC	AVC
		111		R	2S	178	X												ity.	0.1		100				
			C	R	25	179	X																			
	-			R	25	195	X	X	X	1	X		X/O							TAT						
		4		В	25	95	×	X	-		X		TIME		1					16						100
				В	28	295		×c																		
	-		C	R	35	395	-	XA	-	-		-			-			100	100	- A-T			-			
S/P	S/P		C	В	2S	194		OA	X	-	0		X/O	-10					X/-/-	X/-/-	1	- 55				
	-	5	C	R	2S	96	X	×				-	1	1					Comment of the last		-	100		- 5		100
			C	R	35	322		X		4			X/-										-			
			C	В	28	198					-	-						-	151	14		-				
		8	C	В	38	299		0	X	0	X	0	X/O	-10	X/-				X/-/O	X/-/O						
			C	В	38	323		X		0	X	X			X/-		- 1		X/-/O	X/-/O		100				
			C	В	2S	199	X							1.3						107		34		15		
				R	28	165		OA		10	-		0/0	-/0			-	-			-	1	IOA			-
S/P	S	8	C	R	2S	166		OA		0		X	0/0	-/0					100	107		100	OA			100
													L							THAT		138		111		
S	S/P	8	C	R	2S	164	X	0		OA			0/0	-/0					-1-10	-1-10		65	OA			
S	P	10	С		25	898													X/-/-	X/-/-		100		101		
S	S	8		R	28	91	×	×										18	121	CRI		155				
	JH AC	4	T C	R	28	9.4	X			-			LUV				-		030	101			-			
P	S	16	-	R	38	674		-	-	-		-				-	-	+	100		-	1	-		-	+

### SHIFT REGISTER WITH LATCH

					Line is	10X											Te	chnolo	gy	10	0.1			18		
									Bip	olar			CN	/OS	K.	BiC	MOS				Adva	nced	CMOS			
Input Type	Output	No. of Bit	CLR	Shift	Output	Device	TT	S	on.	ALS	AS	u.	H <sub>C</sub>	HCT	BCT	ABT	LY.	ALVT	AC	ACT	AHC	AHC	Ľ	LVC	ALVC	AVC
		- 4	C	В	38	671		X												1 5 1				100	-	
S/P	S/P	4	C	В	35	672		X							1	-			12200	1-5-1-					-	
		8	С	R	25	598		0												1-145						
		8	C	R	38	595		0	1				0/-								10	0	OA			
		8	C	R	OC	599		×					1						11000	12.1		133				
0	0/0	0	0	- 0	0.0	500									100	1				11.00				1000	0.00	

	1.0	8	C	R	35	595	101	0/-	1135			0	OA	
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		8	C	R	25	594		0/-		1000	0	0	OA	
	15.7	16	C	В	38	673	0				W		100	

Explanatory notes [Input/Output Type] S: Serial P: Parallel S/P: Alternative Serial/Parallel [CLR] C: With Clear [Shift] R: Right-Shift B: Alternative Shift Right/Left [Output] 25: Totem-Pole Output 35: 3-State Output [Output] 25: Totem-Pole Output 35: 3-State Output [Output] 25: Totem-Pole Output 35: 3-State Output [Output] 25: Totem-Pole Output 35: 3-State Output [Output] 25: Totem-Pole Output 35: 3-State Output [Output] 25: Totem-Pole Output 35: 3-State Output [Output] 25: Totem-Pole Output 35: 3-State Output [Output] 25: Totem-Pole Output 35: 3-State Output [Output] 25: Totem-Pole Output 35: 3-State Output 35: Shift Sh

tion of the P. S. S. R. Lefeb. AD : Addressed in the Bill : District Later

BCT : SN74BCTxx / SN04BCTxx
AC : 74ACT1xx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACxx / CD74ACxx
ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACxx / CD74ACTxx

### REGISTER(ETC)

												Te	chnol	ogy							
18071653 (FRO188999)		- 9		Bip	oolar			CI	NOS	-	BiC	MOS				Adv	nced	CMOS	3		
Description	Device	Ë	23	co	ALS	AS	u.	HC.	нст	BCT	ABT	LVI	ALVT	AC	ACT	AHC	AHC	LV	LVC	ALVC	AVC
REGISTER FILES 8WX2B	172	X						0.1	- 2					100	the state of	200			- 10		
REGISTER FILES 4WX4B	170	X	X					. 5		100					1					1000	117
REGISTER FILES 4WX4B	670		0					-/0	-/0												
REGISTER FILES 16WX5B	870				0	X								X/-/-	X/-/-						
REGISTER FILES 16WX5B	858													X/-/-	X/-/-	117					
REGISTER FILES 16WX6B	871				X	X						1	-01								
REGISTER FILES 32WX4B	859												1000	X/-/-	X/-/-						
MUX WITH STRAGE	298	X	0			OA		X/-						1 11		14.				1	
MUX WITH STRAGE	398		X										100								
4BIT BUS-BUFFER REGISTER	173	X	OA					X/O	-/0				100		7 6 7						
8BIT STORAGE REGISTER	396		X										0.00	1.0	1 7 1	4					
	818									V 1			100	X/-/-	X/-/-						
8BIT DIAGNOTICCS/PIPELINE REGISTER	819							100	V Tx	10 %	6	100	100	X/-/-	X/-/-				-		
	29818				X					X/-		21	735.7								

○ : Product available in technology indicated \* : New product planned in technology indicated X : Discontinued ■ : Not recommended for new designs

HC : SN74HCx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx BCT: SN74BCTxx / SN64BCTxx

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACxx / CD74ACxx

ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACTxx / CD74ACTxx

### MONOSTABLE MULTIVIBRATOR

								100	L.I.						chnolo	gy							
	1					Bip	olar			CN	ios		BiC	MOS				Adva	nced	CMOS			
Curcuit	CLR	Retrigger	Device	Ī	53	on	ALS	AS	Ŀ	E E	HCT	BCT	ABT	LVI	ALVT	AC	ACT	AHC	AHCT	ΓΛ	LVC	ALVC	41.00
			121	0						3.2.1									-		7		+
1	C	R	122	X	0										1000			6			-51		+
	C	R	422		X			10		OVII					100			10-1					
				1				10	9-1	CVOI					1910						31		
	C	R	123	0	0					-/0	-/0				1200			OA	OA	OA			Т
	C		221	0	0					-/0	-/0	25								OA			-
2	C	R	423		0					-/0	-/0							8					+
	C	R	4538							-/0	-10												1

Explanatory notes [CLR] C: With Clear
[Retrigger] R: With Retrigger
Status O: Product available in technology indicated X: Discontinued IN Not recommended for new designs
HC: SNY4HCX: POJP4HCXX

The Sinyandax / Curantax
Heft : Sinyandax / Curantax
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					100		560				X							1797				_			Н
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- 1				S	S	1	698		×		-	-		-	1000	-	-	-	111 1111	70.1011	191	-	10		H
-1				A	A		192		×		×			X/O	-				×/-/-	X/-/-		-	-		+
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				S	S		163		OA	0			OA	0/0	-/0		_		X/-/O	X/-/O		OA		-	t
-1	-			S	S	-	693		X	-	OB	-	OM	CVC	-10		-	_	N-10	NITO	_	UA	-	-	+
-	-	-		A	S	-	161			-	On	0	04	0/0	-/0		-	-	V// 10	X/-/O	_	0.4	-	-	H
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				Α	S	-	691		×										110	SIO BRIDE			nion (	no les	L
- 1						D	4518							-/0				100	Batclett	107 7 31 1	no inte				
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-1			Y		A		191			-	OA		-	0/0	-10				X/-/-	X/-/-	-	100			Ť
- 1				A	S	1	697		ŏ		-			5/0	1.0		_	_	2.47-9-	7.4.7	1.2	1000	. 101		t
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-1				A	A	R	591		X																Ť
-1				A	A	R	592		0										X/-/-	X/-/-					Ť
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_				A	S	+ +	867					ŏ			1				X/-/-	X/-/-	_	1			t
								X																	

Explanatory notes [DEC-BIN] DEC: Decoder BIN: Binary Counter OHE: Other
[ASYN-SYN] ASYN: Asynchronous SVN: Synchronous
[Up/Down] Y: Up/Down
[CLR] A: With Asynchronous Clear S: With Synchronous Clear
[LOAD] A: With Asynchronous Clear S: With Synchronous Clear 9: Preset 9
[LOAD] A: With Asynchronous Clear 9: With Synchronous Clear 9: Preset 9
[LOAD] A: With Asynchronous Clear 9: Preset 9
[

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACxx / CD74ACxx
ACT : 74AC11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACxx / CD74ACTxx

### RATE MULTIPLIER/FREQUENCY DIVIDERS

TOTAL MODELLI ELEMENT MEDICAL	vych	100	7			_					-		chnolo	gy							
BOAC Beauty			100	Big	oolar			CA	IOS		BIC	MOS				Adva	inced (	CMOS			
Description	Device	I	23	o	ALS	AS	ū.	HC	нст	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHC	7	LVC	ALVC	AVC
FREQUENCY DIVIDERS	56	-	×		1		14			10										Spirit C	
FREQUENCY DIVIDERS	57		X																		
6BIT BINARY RATE MULTIPLIER	97	0													- Investment						
DECADE RATE MULTILIER	167	X												TICH	-007		1	11.5			
PROGRAMABLE FREQUENCY	292		0				50							OTSA	1000			68		Section	
DIVIDER/DIGITAL TIMERS	294		0					J. Jane						POIL		1		55	0		

Status O: Product available in technology indicated \*: New product planned in technology indicated X: Discontinued III: Not recommended for new designs HC: SNT4HCXX / CDT4HCXX HCT: SNT4HCXX / CDT4HCXX HCT: SNT4HCXX / CDT4HCXX BCT: SNT4HCXX / SNT4BCTXX / SNT4BCTXX / SNT4BCTXX / SNT4BCTXX / SNT4BCTXX / SNT4BCTXX / SNT4BCTXX / SNT4BCTXX / SNT4BCTXX / SNT4BCTXX / SNT4BCTXX / SNT4BCTXX / SNT4BCTXX / CDT4ACXX ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SNT4ACTxX / CDT4ACTxX |                        |          |             |      |               |        |      |       |      |     |     |        |       |       |      | Te     | chnolo  | ogy       |   |       |        | 00     |      |      |     |
|------------------------|----------|-------------|------|---------------|--------|------|-------|------|-----|-----|--------|-------|-------|------|--------|---------|-----------|---|-------|--------|--------|------|------|-----|
|                        |          |             |      |               |        |      | Bip   | olar |     |     | CM     | IOS   |       | BiC  | MOS    |         |           |   | Adva  | nced ( | CMOS   |      |      |     |
| No. of<br>Input/output | Output   | Curcuit     | ETC  | Device        | TTL    | LS.  | Ø     | ALS  | AS  | u.  | НС     | нст   | BCT   | ABT  | LVT    | ALVT    | AC        | ACT                                     | AHC   | AHCT   | LV     | TAC  | ALVC | 100 |
|                        | 28       | 1           | -    | 150           | 0      |      | _     |      | _   | -   | _      | ocina | 15791 | 10   | 110    |         | X/-/-     | ×1-1-                                   | 100   | -00    | Pouls  | 1128 | -    | +   |
|                        | 38       | 1           |      | 250           |        |      | -     |      | OA  |     |        |       | -     | -    |        | -       | X/-/-     | X/-/-                                   |       |        |        |      |      | +   |
| 16/1                   | 38       | 1           |      | 850           |        | _    | _     |      | X   |     |        |       |       | +    | +-     | -       | APP       | Alter                                   |       |        |        | -    | -    | t   |
|                        | 38       | 1           | 1    | 851           | -      |      | _     |      | X   |     |        | -     |       | 1    |        | 1       | 500,000   | 10000                                   | -     |        |        | -    |      | ۰   |
|                        | 28       | 1           | 100  | 4067          | 110    |      |       |      | -   |     | X/O    | -     | -     | -    | +      | -       | electron. | Position                                | 10 10 | -      | 1000   | -06  |      | ۰   |
|                        | 2.0      | 255 V V V   | X100 | 4001          | 011    |      | CAN   |      | 600 |     | 200    |       |       | -    | 1001   | 257 100 | 000000    | 01-007-0                                | 6321  | 1100   | 200    | 1-28 |      | +   |
|                        | 28       | 1           | T    | 151           | ×Δ     | 0    | 0     | 0    | 0   | ОВ  | 0/0    | -/0   | T     | T    | T-     | T       | X/-/O     | X/-/O                                   | _     |        | _      |      |      | т   |
|                        | 28       | 1           | 1    | 152           | - 104  | ~    | ~     | _    | _   | -   | X/-    | 70    |       | 1    |        |         | 75770     | 74.40                                   | -     |        |        |      |      | t   |
|                        | 38       | 1           |      | 251           | X      | 0    | ×     | 0    | X   | ОВ  |        | -/0   |       |      | -      | _       | X/-/O     | X/-/X                                   |       | -      |        |      |      | +   |
|                        | 38       | 1           | _    | 354           | -      | ×    |       |      |     | 0.0 | X/O    | -/0   |       |      | Anna   |         | 70.10     | 741.775                                 |       |        |        | 1000 |      | t   |
| 8/1                    | 38       | 1           | -    | 356           |        | ×    |       |      |     |     | X/-    | -10   | -     | -    | -      | +       | -         | H 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 | -     | -      | -      |      | -    | ۰   |
|                        | 38       | 1           |      | 4051          |        |      |       |      |     |     | -10    | -/0   |       | _    | -      | 1       |           |   |       |        | OA     |      |      | t   |
|                        | 38       | 1           |      | 4351          |        |      |       |      |     |     | -10    | -/0   |       | 1    |        |         |           |   | -     |        | -      |      |      | t   |
|                        | OC       | 1 -         |      | 355           |        | ×    |       |      | 7   |     | 1 20   | -     |       | 100  |        |         | 100000    |   |       |        | 100    |      |      | t   |
|                        | OC       | 1 5         |      | 357           | 5-1    | ×    | -     |      |     |     |        |       | 100   | 100  | +      | 1       | _         | 1                                       |       |        | -      |      |      | t   |
|                        |          |             |      | 001           | -      |      |       | -    | -   |     | -      |       | -     | 4    | -      | -       |           | -                                       | -     | -      | -      | 1000 | 1000 | ٠   |
|                        | 28       | 2           |      | 352           |        | ×    |       | ×    | ×   | X   | X/-    |       |       | T    |        |         | X/-/-     | X/-/-                                   |       |        |        |      |      | Т   |
|                        | 38       | 2           |      | 153           | X      | 0    | X     | 0    | 0   | 0   | 0/0    | -10   |       |      |        | 100     | X/-/O     | X/-/O                                   |       |        |        |      |      | ۰   |
|                        | 38       | 2           |      | 253           |        | Ö    | -     | 0    | OA  | 0   | 0/0    | -10   |       |      |        | 1       | X/-/O     | X/-/O                                   |       | -      | -      |      |      | ۰   |
|                        | 38       | 2           |      | 353           |        | X    |       | X    | X   | ×   | X/-    | 1.0   |       |      |        | 1       | X/-/-     | X/-/-                                   |       |        | -      | 710  | -    | ۲   |
| 4/1                    | 38       | 2           | 1    | 4052          |        |      |       | -    |     | -   | -10    | -10   |       | 1    |        |         | 1000      | 1                                       |       |        | OA     | -    |      | Ť   |
|                        | 38       | 2           |      | 4352          |        |      |       |      |     |     | -10    | -     |       |      |        |         | Acres .   |   |       | 0.790  | Un     | PURC | 2120 | ۰   |
|                        | 38       | 4           |      | 16460         |        |      |       |      |     |     |        |       |       | HO   |        | 1       |           |   |       |        |        |      | X    | ۰   |
|                        | 38       | 4           |      | 162460        |        |      |       |      |     |     |        |       |       | HO   |        | 1       |           | _                                       |       |        |        |      | -    | ۰   |
|                        |          | -           | _    | at a safety a | 00     | 0711 |       |      | 08  |     | Spinio | 1000  | 100   | 1    | 0.00   | STORY.  | VEGTOR/I  | Set of up                               |       | 1      | 15.033 | 100  | -    | ٠   |
|                        | 28       | 1           |      | 157           | X      | 0    | 0     | OA   | 0   | OA  | 0/0    | 0/0   | 1     | 100  | Trest. | lam.    | X/-/O     | X/-/O                                   | 10    | -0     | OA     | OA   |      | т   |
|                        | 25       | 1           |      | 158           |        | 0    | X     | 0    |     | XA  |        | -/0   | _     |      |        |         | X/-/O     | X/-/O                                   | Ŏ.    | Ó      | 1      |      |      | t   |
|                        | 28       | 4           | S    | 399           |        | 0    |       |      |     |     |        |       |       |      |        |         |           |   |       |        |        | 4.1  |      | Ť   |
|                        | 38       | 1           |      | 257           |        | ОВ   | 0     | OA   | 0   | 0   | 0/0    | 0/0   |       |      |        |         | 0/-/0     | 0/-/0                                   |       | -      |        | OA   |      | T   |
|                        | 38       | 1           |      | 258           |        | OB   | X     | OA   | 0   | 0   | 0/0    | -/0   |       |      |        |         | X/-/-     | X/-/O                                   | 100   |        | 779    | 1    |      | Ť   |
|                        | 38       | 4           | 14.0 | 4053          | 3 [1]  | UT U | 5.0   |      |     |     | -10    | -10   |       | 10-0 |        |         | oldbir.   | 1 Jelius                                | 11.30 | 17.7   | OA     | DI   |      | Ť   |
| 2/1                    |          | 6           | U    | 857           | est in | 8.4  | OKA I | 0    | X   | 100 |        | man d | olon  | 100  | 357    | 10.00   | onlines.  | (Product                                | CERT  | TO.    | 157    | 755  |      | Ť   |
| 2/1                    | 38       |             |      |               |        | X    |       |      |     |     | ×      |       |       |      |        |         |           |   |       |        |        |      |      | Ť   |
| 2/1                    | 38       | 8           | S    | 604           |        |      |       |      |     |     |        |       |       |      |        |         |           |   |       |        |        |      |      |     |
| 2/1                    | 3S<br>OC | 8           | S    | 604<br>605    |        | X    |       |      |     |     |        |       |       |      |        |         |           |   |       |        |        |      |      | Т   |
| 2/1                    | 38       | 8<br>8<br>8 |      |               |        |      |       |      |     |     |        |       |       |      |        | -       |           |   |       |        |        |      |      | Ŧ   |
| 2/1                    | 3S<br>OC | 8           | S    | 605           |        | X    |       |      |     |     |        |       |       |      |        |         |           |   |       |        |        |      |      | I   |

### DECODER/DEMULTIPLEXER

															Te	chnolo	gy							
	(BADADA)	111111				-	Bip	olar			CN	IOS		BIC	MOS				Adva	nced	CMOS		_	_
No. of Input/output	Output	Curcuit	ETC	Device	TTL	rs.	ø	ALS	AS	ш	HC	нст	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	ΓΛ	LVC	ALVC	AVC
	28	1	AD	4514							X/O	-/0									11.0	HAT I	48.4	
	28	1	AD	4515							X/O	-/0								100	500	HT ED	AMA	10
4/16	3\$	1		154	0						X/O	-/0				- 3	X/-/-	X/-/-			11251/	Thursday.		(In
	oc	1		159	0																			
	2S	1	BD	42	XA	0					0/0	-/0									1			
4/10	28	1	BD	43		Ť					-	-												
	28	1	BD	44	X														-					
	28	1		238							X/O	-/0					X/-/O	X/-/O		ITOS	1-188	170		
	2S	1	100	138		0	OA	OA	0	0	0/0	010		20.0			0/-/0	X/-/O	0	0	OA	OA		
3/8	2S	1	AD	237					00		X/O	-10	bout		0.00	de la company	ni didahili	on reulic	100	11111	5635	T I'm		
	28	1	AD	137		X		OA	X		X/O	X/0												
	2S	1	AD	131				X	X															
	2S	2		139		IOA	OA	0	IX	X	0/0	0/0				T	X/-/O	0/-/0	To	ΙO	OA	OA		
1.0	2S	2		239			1	-			X/-	-					X/-/-	X/-/-	1		-			
2/4	2S	2		155	X	OA												1123	UNI	UU	THE.	T-Uzil,	110.9	110
	oc	2		156	X	0		0																

Explanatory notes [Output] 2S:Totem pole Output 3S:3-State Output OC:Open-Collector Output [ETC] AD:Adress Latch BD:BCD TO DECIMAL Status O:Product available in technology indicated \*:New product planned in technology indicated X:Obscontinued B:Not recommended for new designs HC:SN74HCxx / CD74HCxx HCT:SN74HCxx / CD74HCTxx BCT:SN74HCTx / SN64BCTxx AC:74AC1txx (Product available in reduced-noise advanced CMOS:11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

CODE CONVERTER. PRIORITY ENCODER/REGISTER

												Te	chnolo	gy							
				Big	olar			CN	IOS		BIC	MOS	1-0			Adva	anced	CMOS	5		
Description	Device	TI	53	co	ALS	AS	ш	HC	HCT	BCT	ABT	LVI	ALVT	AC	ACT	AHC	AHC	r	LVC	ALVC	AVC
CODE CONVERTER	184								-												
CODE CONVERTER	185	X					-		10		1						- 10				
10-4 PRIORITY ENCODER	147	X	X	1				-/0	-/0									- 0			
8-3 PRIORITY ENCODER	148	X	0				X	0/-				100									
8-3 PRIORITY ENCODER	348		0					1				X		100			100			3.50	
4BIT CASCADABLE PRIORITY REGISTER	278	×												1			I III				

○ : Product available in technology indicated \*: New product planned in technology indicated X : Discontinued 
■ : Not recommended for new designs 
HC : SN74HCX / DD74HCX.

HCT: SN74HCxx / CD74HCTxx BCT: SN74BCTxx / SN64BCTxx

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACxx / CD74ACxx

### Display Decoder/Driver

,		ygral gyvta	11											chnolo	ogy							
86/96/ 083	NAME OF TAXABLE PARTY.	10000		111	Bip	olar			CI	MOS	PH.	BiC	MOS				Adva	nced	CMOS	5		
Function	V <sub>OH</sub> (V)	Device	TTL	SI	o	ALS	AS	ш	HC	HCT	BCT	ABT	F	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AND
D	30	45	0		т		$\overline{}$															
D	60	141	X					-		-					10.00	)			-			
D	15	145	0	0				-0		- 60			100				-		100			
D	7	445		X									1100		106						- 3	
7	30	46	X					10				00	100									
7	15	47	OA	0									-								1.5	
7	5.5	48	X	X						10			-									
7	5.5	49		X								-	1									
7	30	246	X						-													
7	15	247	X	0								100	· ·			and CE 12	- Change		100	a Torres		
7	7	347		1	1111		1	-		1							100				1111111	
7	7	447								100-7	1995	11/1/17	100	Critical	SUCT ANTES	andher	100	Ive				
7	5.5	248		X	100			100	10000	phypo	11 90	11		No.	ast Allem	Carabat n	Printer.	978	20,000	100		
7	5.5	249		X			I			- 1	1000	100	100	SOUTH THE	monone	1001-1		10111	000	9		
В	7	142														0.0141	5 30.	82.0	(23)	11.0		
В	7	143	×			T	T	T								OTOHOT	COV	1000	1717	100		
В	7	144	X					T					1		100	rossai	11 1 2	100	17115	173		

Explanatory notes [Function] D : BCD TO DECIMAL. 7 : BCD TO 7-SEGMENT. B : COUNTER/LATCH/DECODER/DRIVER  $[V_{\rm od}]$  Off-Stage Output Voltage(V)

\(\mathbb{V}\_{out}\) OT-Stage Output Voltage(V)
\(\mathbb{V}\) Product valiable in technology indicated
\(\times\): Discontinued
\(\mathbb{W}\): Not recommended for new designs
\(\mathbb{H}\): SNT4HCxx / CD74HCxx
\(\mathbb{H}\): T: SNT4HCxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC : 74ACT11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACxx / CD74ACxx ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACTxx / CD74ACTxx

### COMPARATOR

							2340		24(2)	(III)	UI II	2077	10.101	Section Co.	SULMI INC.	4	177	Te	chnole	ogy	ORIGINAL IN	til die	Days 1	VIII.		1911	
										Bip	olar			CN	108	W. Fr	BiC	MOS	ontan	Milling	2013 - 70	Adva	anced	CMOS	3		
No. of Bit	Input	P=Q	P=Q	P>Q	P <q< th=""><th>Output</th><th>Device</th><th>TTL</th><th>23</th><th>o</th><th>ALS</th><th>AS</th><th>ш</th><th>HC</th><th>HCT</th><th>BCT</th><th>ABT</th><th>LVT</th><th>ALVT</th><th>AC</th><th>ACT</th><th>AHC</th><th>AHC</th><th>LV</th><th>LVC</th><th>ALVC</th><th>AVC</th></q<>	Output	Device	TTL	23	o	ALS	AS	ш	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHC	LV	LVC	ALVC	AVC
4	S	Υ	N	Y	Y	28	85	X	0	0		X		XA/O	-/0										2-0		
6	S	N	Y	N	N	28	29806	-	1		X	30	111		2 000	1000		1	10000	0.01	Section 1977	1000	1000		2-11		
8	20	Y	N	N	N	OC	518	777	110	999	0	25/1	X	129712	12121720	10.00	141		1023.0	J. DOLLARS	er housely	19.0	9073	21910	1 1 44		
8	20	N	Y	N	N	2S	520				10		×							X/-/-	X/-/-				-		
8	20	N	Y	N	N	oc	522				X																
8	20	N	Y	Y	N	2S	682		0					0/-													
8	20	N	Y	Y	N	oc	683		X																		
8	S	Y	N	N	N	OC	519				X		X						- 20	OUN CLOS	at 1 litera	0.0	2000	100	non.	action.	101
8	S	N	Y	N	N	28	521				0		0						10.00	X/-/-	X/-/-						
8	S	N	Y	Y	N	28	684		0					0/-					-						-	1	
8	S	N	Y	Y	N	oc	685		X			700			100	Thu.					malacia			44.52	5	100	
8	S	N	Y	Y	N	2S	686		X		1		.0	100	10 2		00.1		April	T. L. J. S. S. S. S.	70400	2.79	100	ruo.	140	60.17	ALC: N
8	S	N	Y	Y	N	oc	687		X						113												
8	S	N	Y	N	N	28	688		0		0			0/0	-10			100					Y	TY.			
8	S	N	Y	N	N	oc	689		X		X						DI	150		N. Y.	. Y.		1	Y			1
8	S	Y	N	Y	Y	2S	860											100		×/-/-	X/-/-				1		
8	S	N	N	Y	Y	2S	865				- 1									X/-/-	×/-/-						
8	LP	N	N	Y	Y	25	885					0					K T	155		X/-/-	X/-/-					50.70	
8	LPQ	Y	N	Y	Y	oc	866					XA									Y						
9	-	N	Y	N	N	2S	29809				X						AL.	100						- Y			100

BCT : SN74BCTxx / SN64BCTxx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx ACT: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACTxx ACT: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACTxx

### ADRESS COMPARATOR . FUSE-PROGRAMMABLE IDENTITY COMPARATOR

Tuesternia T			Technology								
	Bipolar CMOS BICMOS Advanced CMOS										
	TITAL										

Explanatory notes [Function] A: Adress Comparator F: Fuse-Programmable Identity Comparators

[ETC] OE : Output-With Enable L : Output-With Latch Status : Product available in technology indicated \*: New product planned in technology indicated

X: Discontinued : Not recommended for new designs

HC : SN74HCxx / CD74HCxx

HCT: SN74HCxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

### PARITY GENERATOR / CHECKER

			81.0	ool		101	10 E	1000100	100 00	1011-D	doub	Tech	nolog	У	auti (Prae	ATT I	CIAN		DAL		
				Bip	olar	W		CN	ios		BIC	MOS			A	dvano	ced CI	MOS			
No. of Bit	Device	E	ES.	o	ALS	AS	u.	£	НСТ	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHC	7	LVC	ALVC	AVC
8	180							×													
9	280		0	0	10	0	OB	X/O	-/0					X/-/O	X/-/O						
9	286					0	X							X/-/-	0/-/-						

HC: SN74HCxx / CD74HCxx

HCT : SN74HCxx / CD74HCTxx

BCT : SN74BCTxx / SN64BCTxx

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

### VOLTAGE CONTROLLED OSCILLATOR(VCO)

																1		Tech	nology	1							100
7,000										Bip	olar			CN	ios		BiC	MOS				Advan	ced CI	MOS			1801
Curcuit	Fmax (MHz)	Z OUT	ENABLE	RANGE	Rext	PLL	Device	I	23	on	ALS	AS	ш	HC	НСТ	BCT	ABT	LVI	ALVT	AC	ACT	AHC	AHC	r.	LVC	ALVC	AVC
	20	Y	Y	Y			624		0				7	1 14	130					11.00		10		1			
1	20	Y	Y	Y	Y		628		0						111				2		THE			15			
	24			-1-176	Υ	Y	7046							-10	-10			10					15.	7	L.E		
	20			1	1 3		627		X	_										1 88	1	1				-	T
	20		Y	Y			629		0											AU.	11 11			7	5116		1
	20	Y					625		X									18	(BES.)	-85.	TILL			111			
2	20	Y	Y				626		X													1					
	60		Y	Y	dolo	100	124	70		0	no		9	210	el sal	du	9.7	1-15	08	Smbm	18.13	lus		10/0	1011		1
	24				Y	Y	4046							-10		14.57	111	V	W.	0.50.0	CO. 10	0.0					$\Box$

- HCT : SN74HCxx / CD74HCTxx
- BCT: SN74BCTxx / SN64BCTxx
- AC : 74AC11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACxx / CD74ACxx
- AC : 74AC11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN/4ACxx / CD/4ACxx

  ACT : 74AC111xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN/4ACxx / CD/4AC1xx

### ACCUMULATORS, ARITHMETIC LOGIC UNIT(ALU), LOOK-AHEAD CARRY GENERATOR

											To	chno	ology								
Advantable (2008	2 NATHE		- 3	Bip	olar			CN	<b>AOS</b>		BIC	MOS			Ad	vanc	ed C	MOS		Lan B	
Description	Device	TTL	23	s)	ALS	AS	u	HC	HCT	BCT	ABT	LVI	ALVT	AC	ACT	AHC	AHCT	r	LVC	ALVC	AVC
4BIT PARALLEL BINARY ACCUMULATORS	281			X					IX	1	(0)				J. SPIS	100	100	1933	2046	Y	
4BIT PARALLEL BINARY ACCUMULATORS	681		X						1.35		10				27134	DRI	100	High	Marile.	178	940
4BIT ALU/FUNCTION GENERATORS	181	X	0	X		OA			1.8					X/-/-	X/-/-	2811	100	1463	1 111	YEL	
4BIT ALU/FUNCTION GENERATORS	381		X	×			×		1 %		10				PE	130	11119	307.3	627)	No.	16.5
4BIT ALU/FUNCTION GENERATORS	881					XA			18		10			X/-/-	X/-/-		18	139		SOF	
4BIT ALU WITH RIPPLE CARRY	382		X				X		1 %	1	0						1.5	1295	ASA.	Hon	9/1
LOOK AHEAD CARRY GENERATORS	264					X			LX					Contract of	1100 A	753	10.8	137	684	SPOR	100
LOOK AHEAD CARRY GENERATORS	182	X		0		X			1.76	. 1		TY.			HUTA	HIL	17.8	-117	1474	1924	140
LOOK AHEAD CARRY GENERATORS	282					X		. 10			100							101/	9.33	diffe	23.0
LOOK AHEAD CARRY GENERATORS	882					XA					75			×/-/-	X/-/-		1933	0108	O M	DAKE	
QUAD SERIAL ADDER/SUBTRACTOR	385		X									2									

- : Product available in technology indicated \*: New product planned in technology indicated
- X : Discontinued : Not recommended for new designs HC : SN74HCxx / CD74HCxx
- HCT : SN74HCxx / CD74HCTxx

- BOT : SN/HACT.xx / SN6-BBCT.xx

  BOT : SN/HACT.xx / SN6-BBCT.xx

  AC : 74ACT1xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACTxx / CD74ACTxx

  ACT : 74ACT1xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACTxx / CD74ACTxx

											Te	chno	logy								
				Bip	olar		6	CI	MOS		BICI	MOS			Ad	vanc	ed C	MOS			
Description	Device	TTL	23	so	ALS	AS	u.	HC	HCT	BCT	ABT	LVI	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
4BIT BINARY FULL ADDER	83	×	×											- 100							
4BIT BINARY FULL ADDER	283	X	0	0			0	-/0	-10					-/-/0	-/-/0						
DUAL CARRY SAVE FULL ADDER	183		X											100							
GATED FULL ADDER	80	X												-				14.5			1016
2BIT BINARY FULL ADDER	82	X			100						1										

### Status

- : Product available in technology indicated \*: New product planned in technology indicated X : Discontinued ■: Not recommended for new designs HC : SN74HCx / CD74HCx.

- HCT: SN74HCxx / CD74HCTxx BCT: SN74BCTxx / SN64BCTxx
- AC : 74AC11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACxx / CD74ACxx
- ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACTxx / CD74ACTxx

Electron September 1				Technology																	
Description	Device	Bipolar					CMOS		BICMOS			Advanced CMOS									
		TTL	23	S	ALS	AS	ш	HC	нст	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	2	LVC	ALVC	AVC
2-4 PARALLEL BINARY MULTIPLIERS	261		X		Tr.						100					een-		100			
4-4 PARALLEL BINARY MULTIPLIERS	284	X			77.7						100										
4-4 PARALLEL BINARY MULTIPLIERS	285	X								19	100			HUNTAN	PH11-191	2.5	177	-	12.00	1.00	
2'S COMPLEMENT MULTIPLIERS	384		X																		

- O: Product available in technology indicated \*: New product planned in technology indicated
- X: Discontinued II: Not recommended for new designs HC: SN74HCxx / CD74HCxx
- HCT : SN74HCxx / CD74HCTxx
- BCT: SN74BCTxx / SN64BCTxx
- AC : 74AC11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACxx / CD74ACxx ACT : 74AC11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74AC7xx / CD74AC7xx

#### MEMORY

	Technology																					
TOTAL STREET	11 (1440)			Bip	olar			CI	NOS	IOS BICMOS						Advanced CMOS						
Description	Device	E	1.3	so.	ALS	AS	ш	HC	HCT	BCT	ABT	LVI	ALVT	AC	ACT	AHC	AHCT	2	LVC	ALVC	AVC	
MEMORY REFRESH CONTROLLERS	600		×											3.0	TARRE	101	71	MIS	SILU	10.17		
MEMORY REFRESH CONTROLLERS	601		X						1.8		10			100	TAJUNE		711	HID	191.13	700		
MEMORY REFRESH CONTROLLERS	603		X				AL.			100	63				1500	10		400	11111	12110		
MEMORY CYCLE CONTROLLER	608		X			111			1 X						IDita	100		0.1	110	10.10		
MEMMORY MAPPERS	612		X				20								81101		100	-	110	11.11		
MEMMORY MAPPERS	613		X			100			12	13	1					100		1471	117	Total		
MEMMORY MAPPERS WITH LATCH	610		X												TOROT.	A TOP	197	1714	A DE	PAR.	150	
MEMMORY MAPPERS WITH LATCH	611		×							10 10					DIDE	1	10	1194	0.00	THAT !	110	
MULTI-MODE LATCH	412			X											RECT	4 190	10	HULA	. 114	104	100	
3-8 MEMORY DECIDER	2414						2			0/-					SAUT		10.	100	1 34	115	100	

○ : Product available in technology indicated \*: New product planned in technology indicated X : Discontinued ■ : Not recomended for new designs HC : SN74HCXX / CD74HCXX

HC: SNY4BCXX / CD74BCXX
HCT: SNY4BCXX / CD74BCXX
BCT: SNY4BCXX / CD74BCXX
BCT: SNY4BCXX / SN64BCTXX
AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
ACT: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACTxx

#### CLOCK GENERATOR CIRCUIT

											Т	echno	ology									
A STATE OF THE SAM	The second			Bip	oolar		200	CN	CMOS			MOS			Advanced CMOS							
Description	Device	TTL	1.8	ø	ALS	AS	ш	£	нст	BCT	ABT	LY	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	
QUAD COMPLEMENTARY-OUTPUT LOGIC	265	X																	-			
DUAL PULSE SYNCHRONIZERS/DRIVERS	120	X									100						1			1		
CRYSTAL-CONTOROLLED OSCILLATORS	320		X					-10			11			-	24.00	100				100	100	
CRYSTAL-CONTOROLLED OSCILLATORS	321		X																			
DIGITAL PHASE-LOCK LOOP	297		0					-10	-/0						-/-/0							

- ○: Product available in technology indicated

  X: Discontinued

  I: Not recommended for new designs

  KO: SNY4HCxx / DDY4HCXx

  HCT: SNY4HCxx / CD74HCTxx

  BCT: SNY4BCTxx / SN4BCTxx

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACxx / CD74ACxx ACT : 74AC11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACxx / CD74AC7xx

#### SWITCH, SHIFTER, ERROR DETECTION CORRECTION CIRCUIT, HARD DISK DRIVER

		Technology Bipolar CMOS BiCMOS Advanced CMOS																			
Description	Land and			Bip	olar			CN	ios		BIC	MOS		Advanced CMOS							
	Device	I	53	on	ALS	AS	ш	HC	нст	BCT	ABT	LVI	ALVT	AC	ACT	AHC	AHCT	r.	LVC	ALVC	AVC
QUAD BILATERAL SWITCHES	4016							-/0	1 4 3						Epm N		1	OA	172	100	
	4066							0/0	-/0		10				Brims		1 V	13,600		100	100
ANALOG SWITCHES WITH LEVEL TRANSLATION	4316							-/0	-10						THAT			100	-		
4BIT SHIFTERS	350			X			×		123							10	0.00	1 130		100	15.0
8BIT PARALLEL ERROR DETECTION CORRECTION CIRCUIT	636		X																		
	637	30	X			100	11 11	A PRINT	SMA		1281	100	1.100	TOTAL POP	olds!	-	110	05		1.0	
	616				X			100	e-h v	90 Y		Mor	(7)90	in Intil		110	101	nici.	×		
16BIT PARALLEL ERROR DETECTION CORRECTION	617													2307	17 U.O. 1	100	10.7	984	224		
CIRCUIT	630		×											De TOHI	100 11	o OH	1	117	311		
	631		×											er tomb	100 A 3150	dos	17	2.3	201		
	632	1 (4)	700	100	X	×	100	DOM: N	who a	des per	200	-		Minus 5	mboods)		-07	NT 5	TLA:		
32BIT PARALLEL ERROR DETECTION CORRECTION	633				X										-		100		SA		
CIRCUIT	634				X	X															
	635				X																
HARD DISK DRIVER	1250				X																

Status

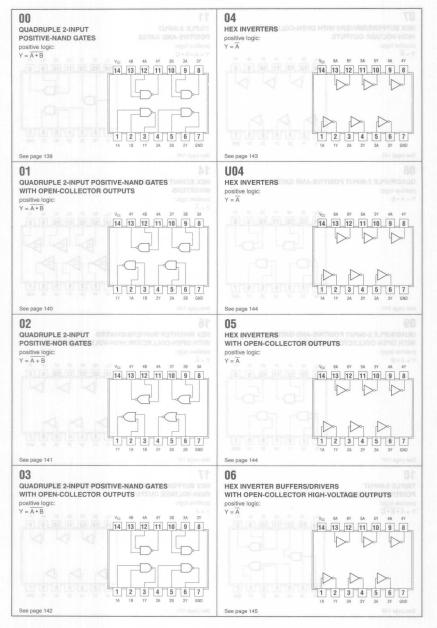
- O: Product available in technology indicated \*: New product planned in technology indicated
- C : Product available in technology indicated
   ∴ New product
   ∴ Discontinued
   ∴ Not recommended for new designs
   HCT : SN74HCxx / CD74HCxx

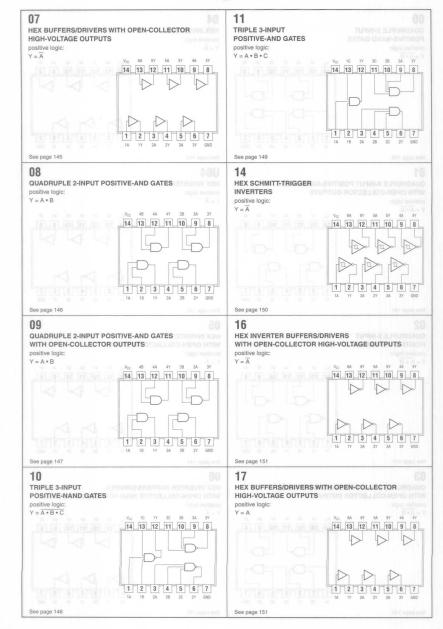
BCT : SN74BCTxx / SN64BCTxx
AC : 74AC11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACxx / CD74ACxx

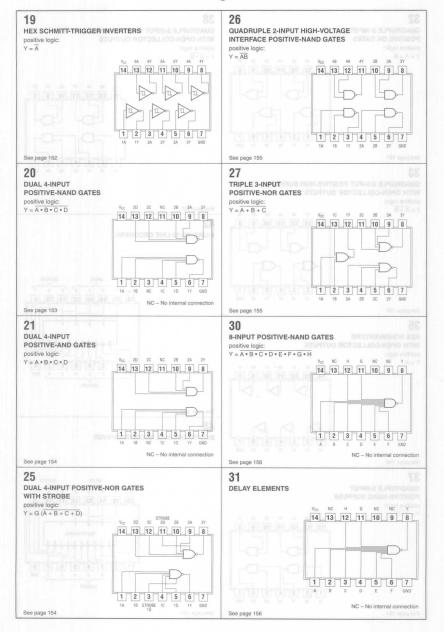
ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS : 11000 Series) / SN74ACTxx / CD74ACTxx

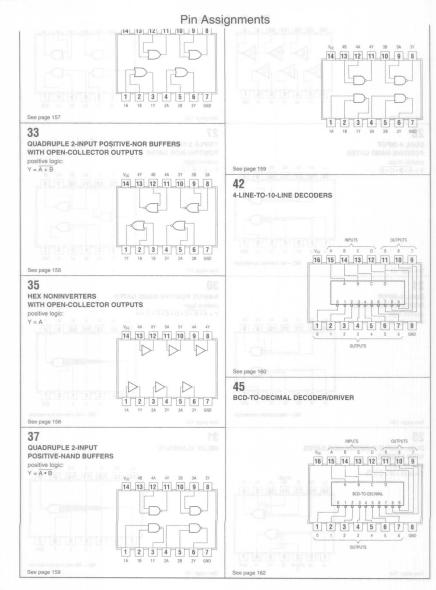
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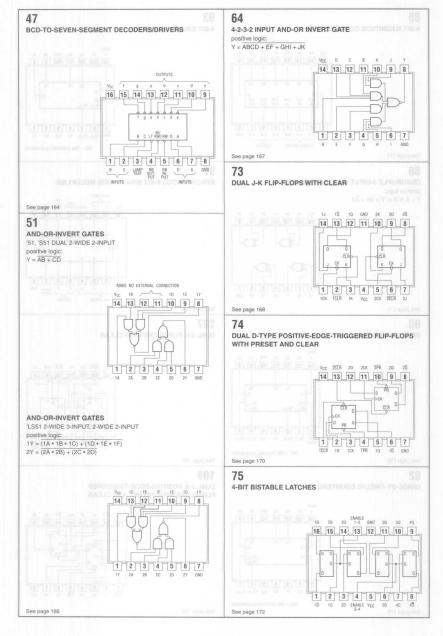
## PIN ASSIGNMENTS

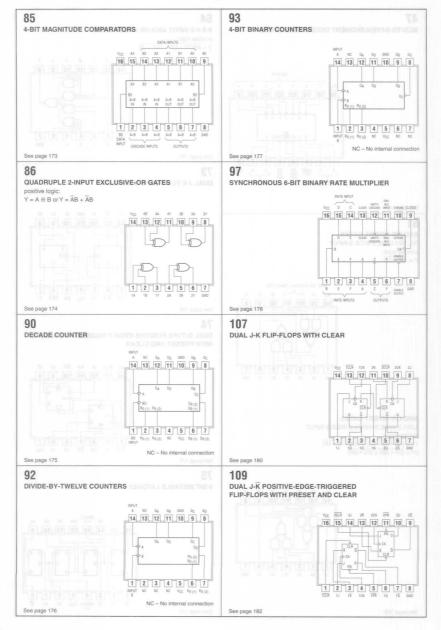


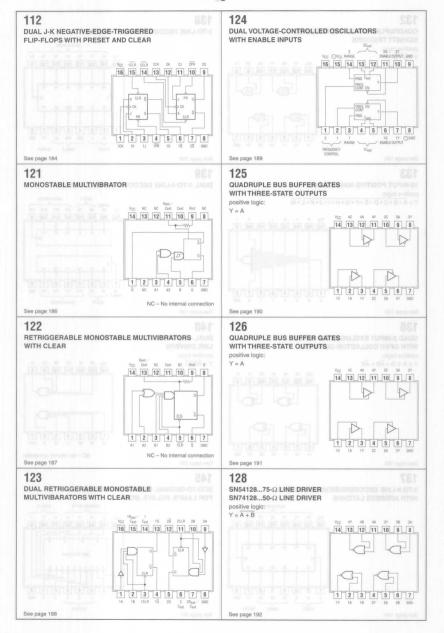


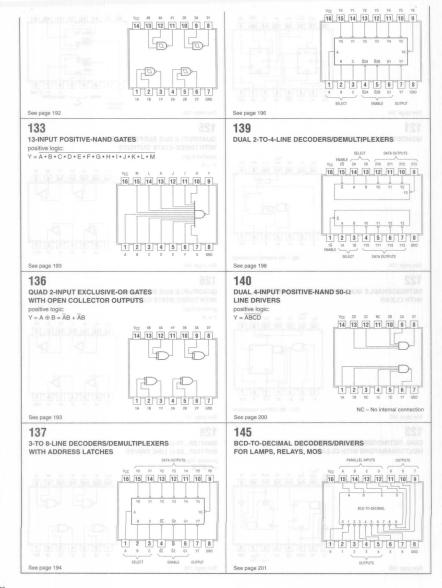


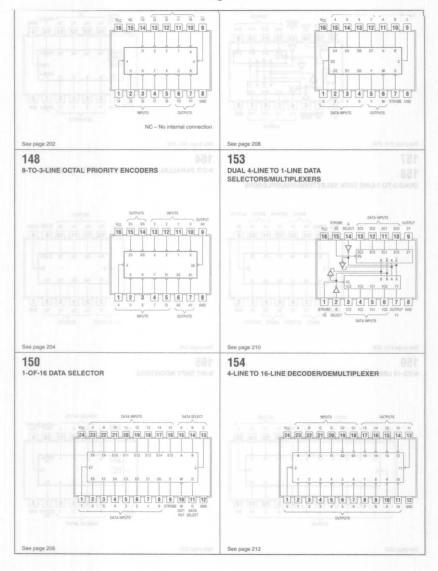


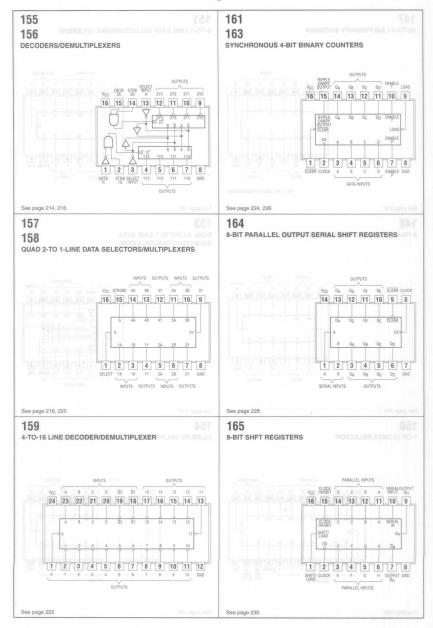


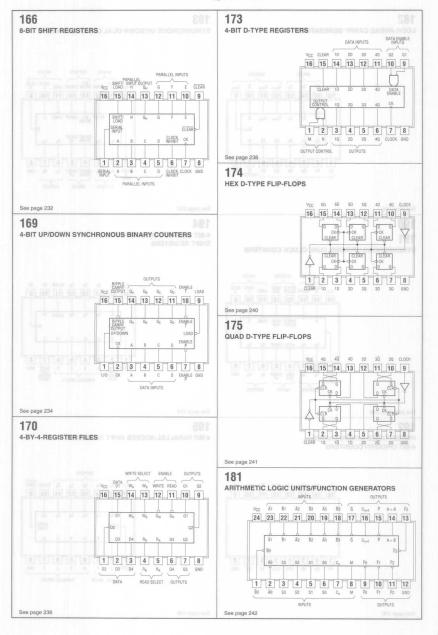


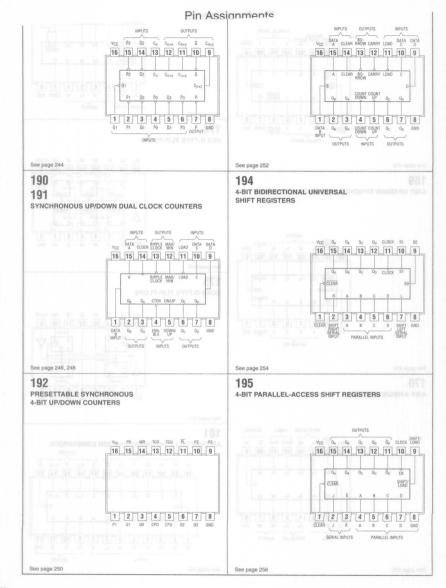


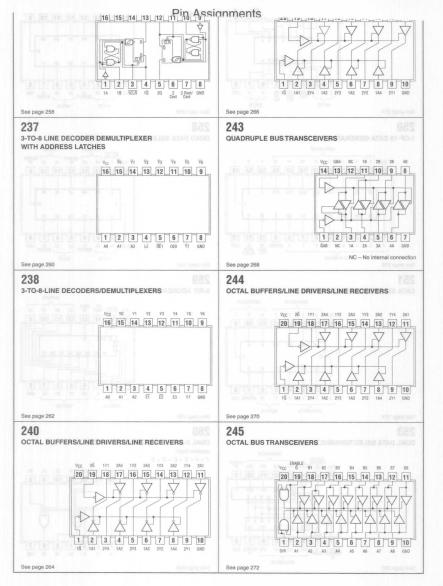


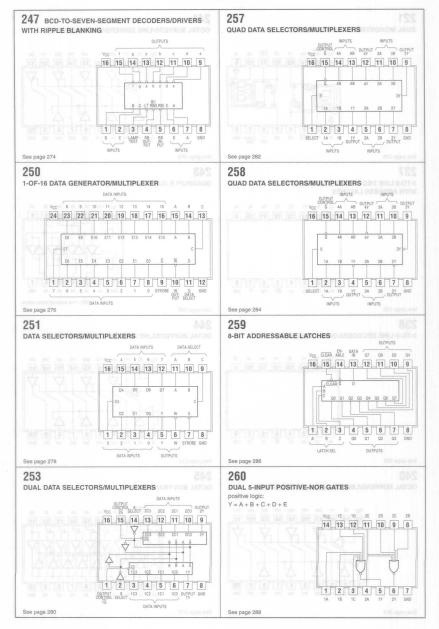


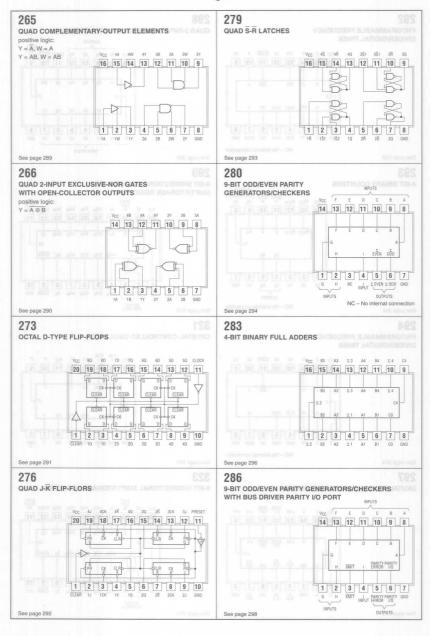


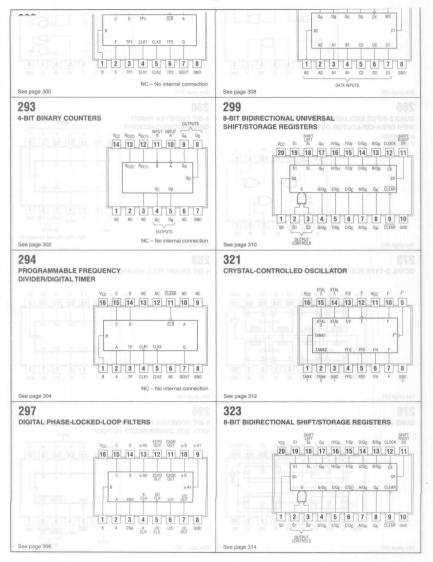


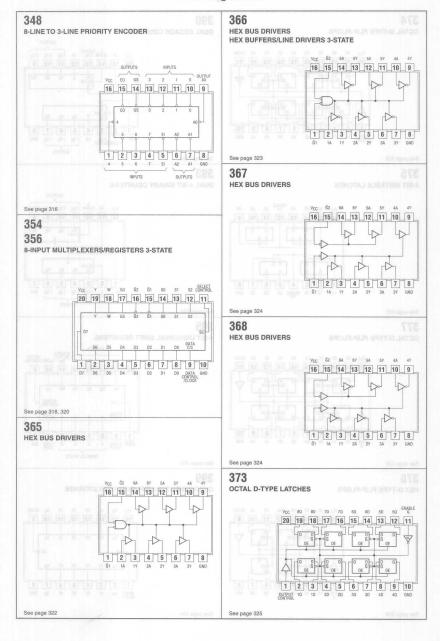


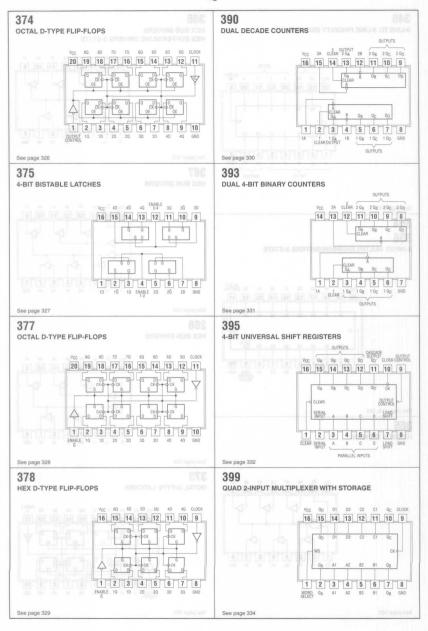


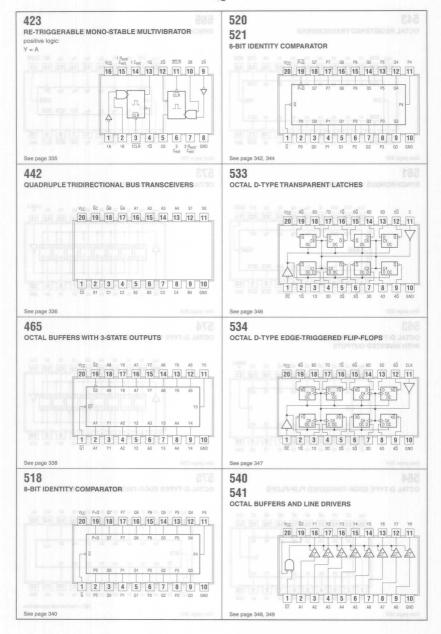


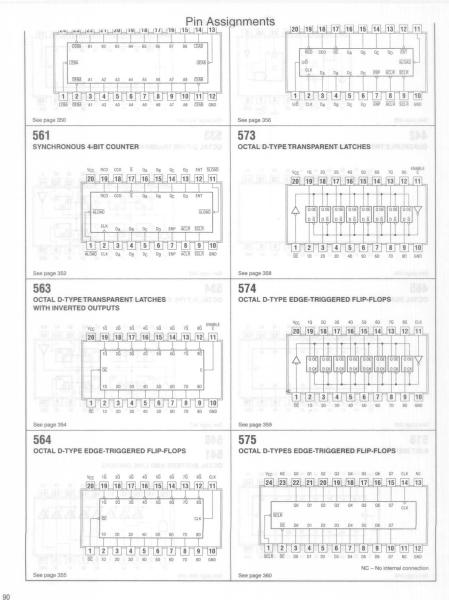


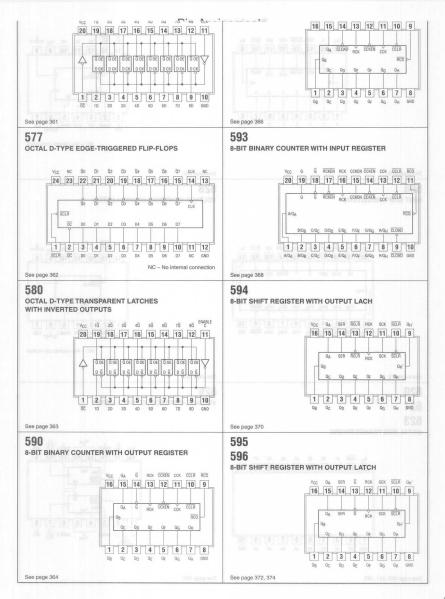


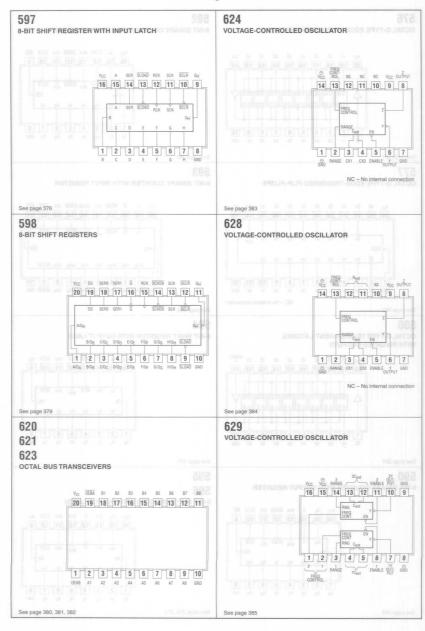


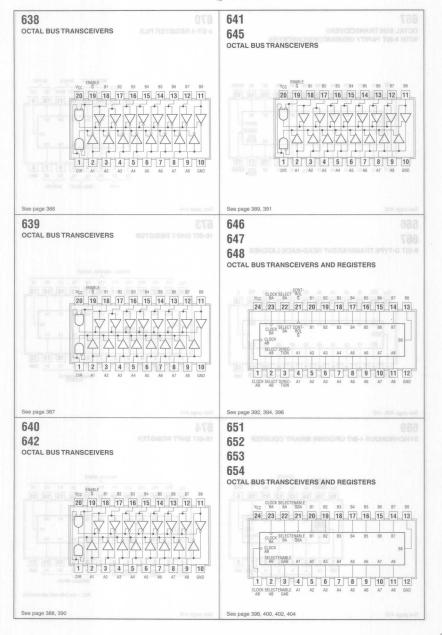


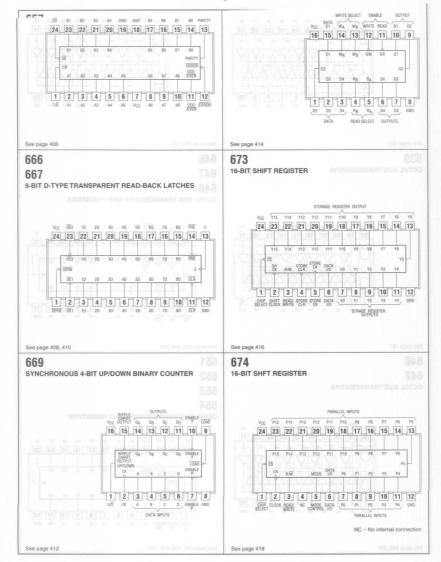


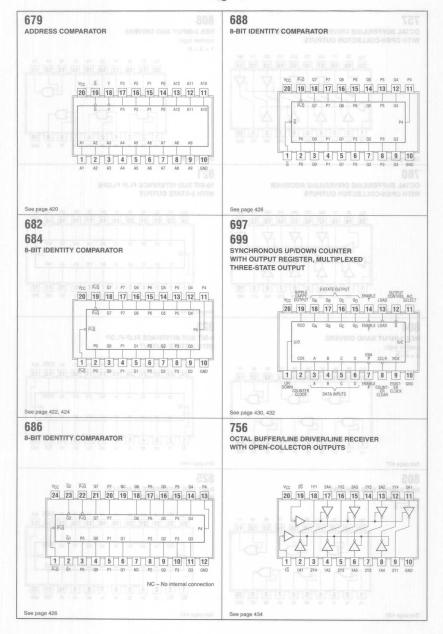


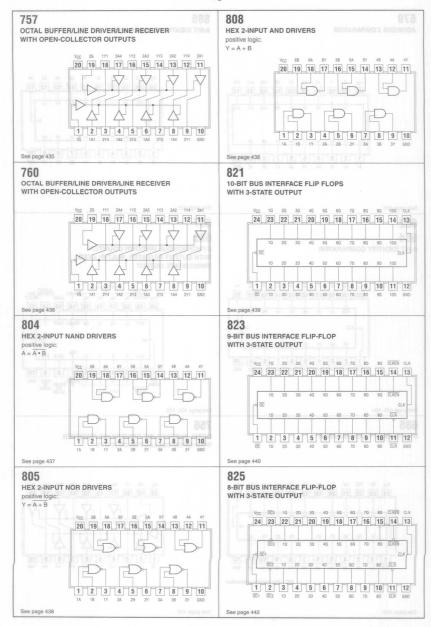


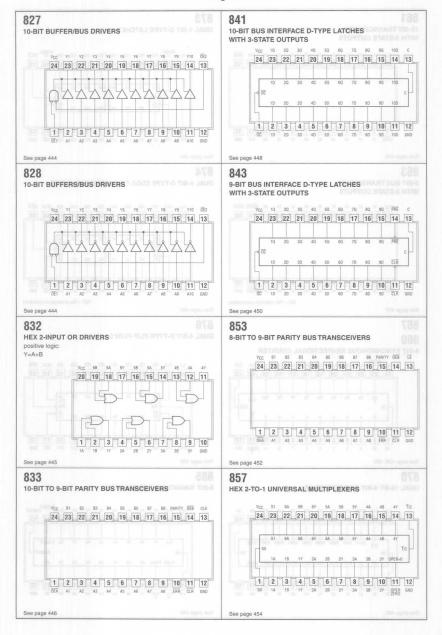


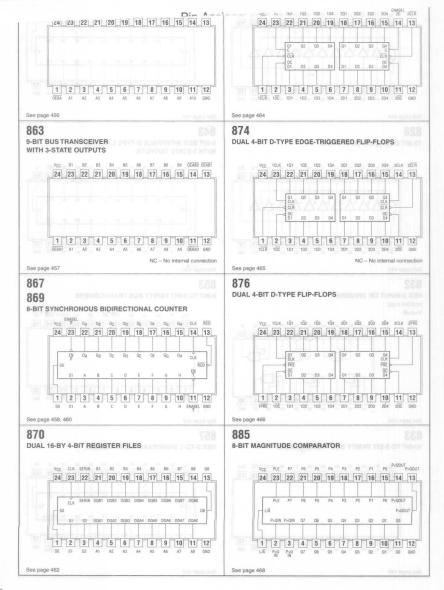


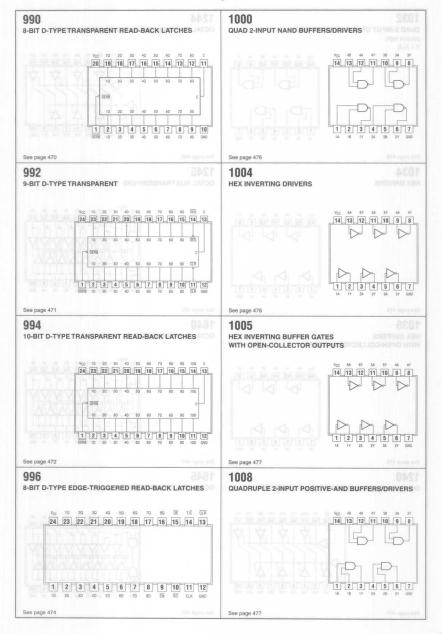


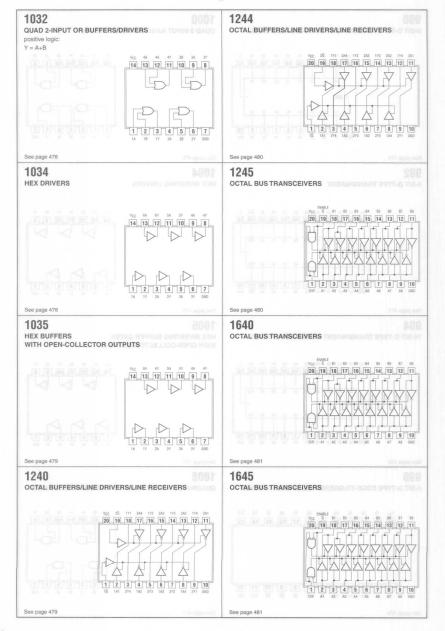


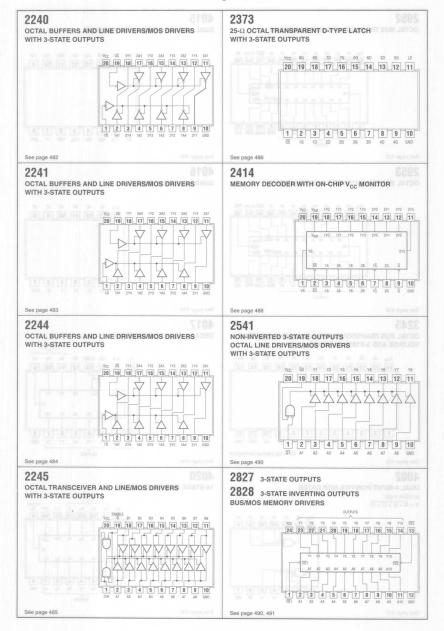


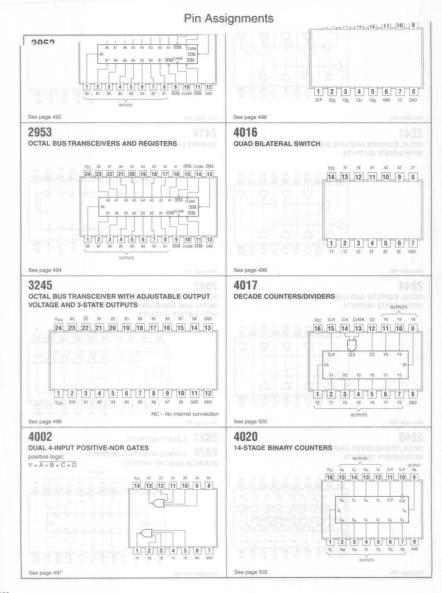


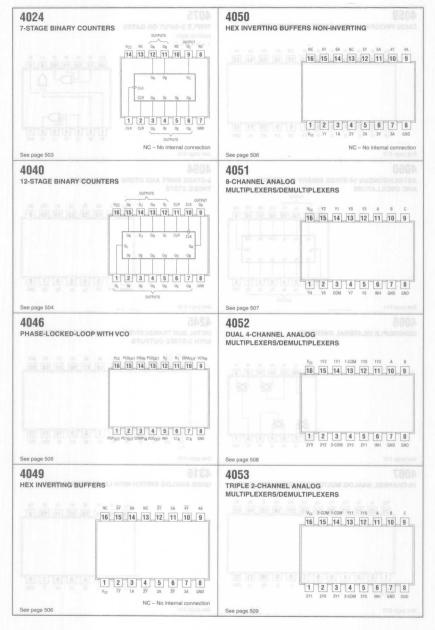


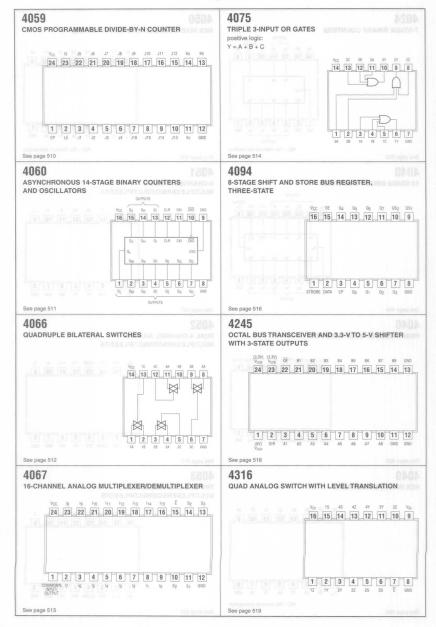


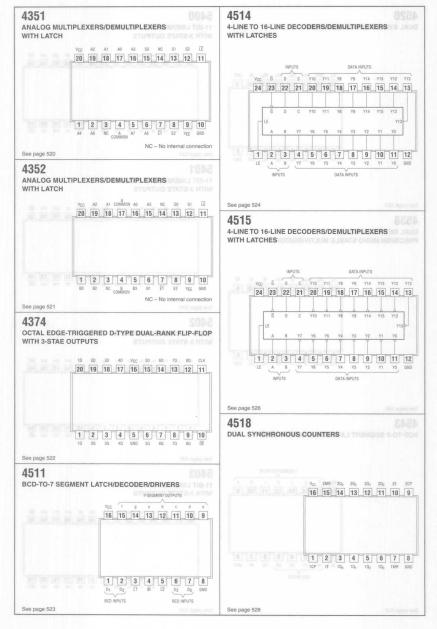


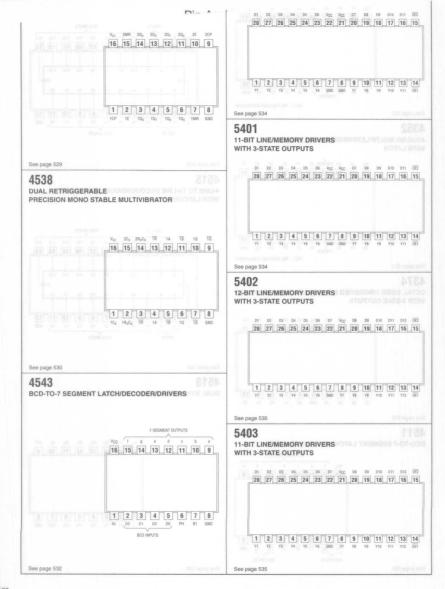


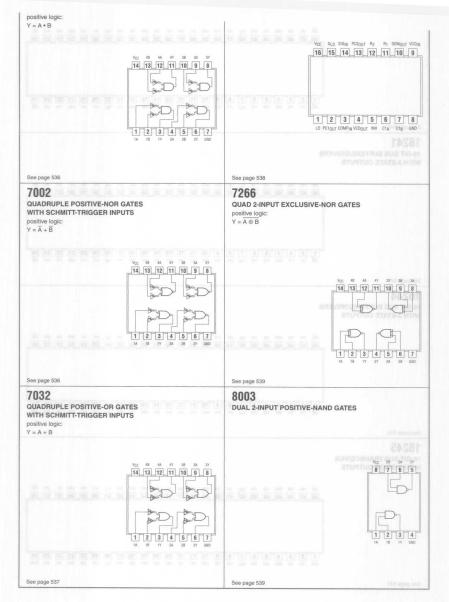


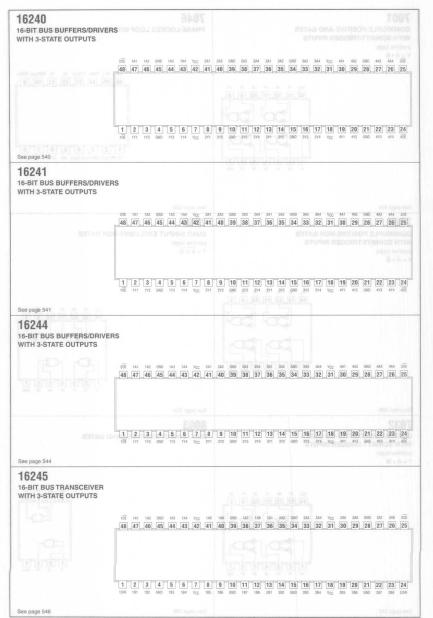


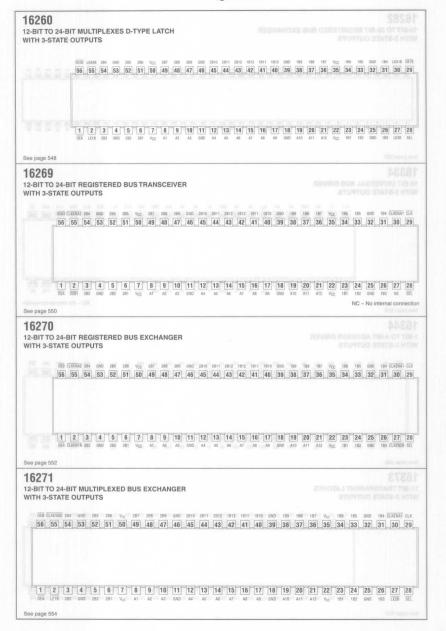




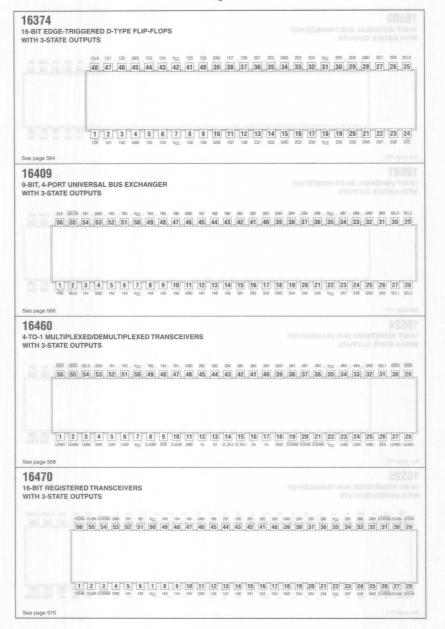


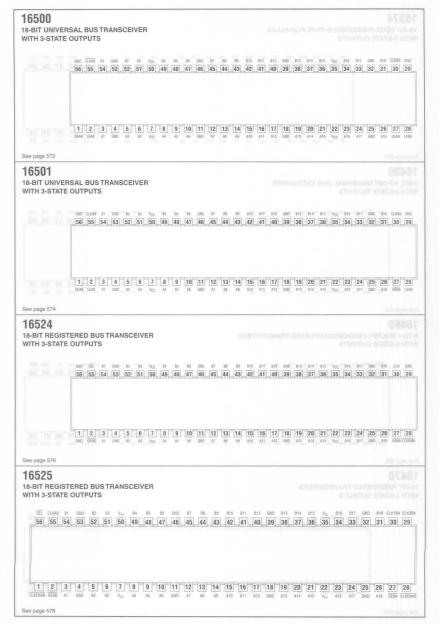


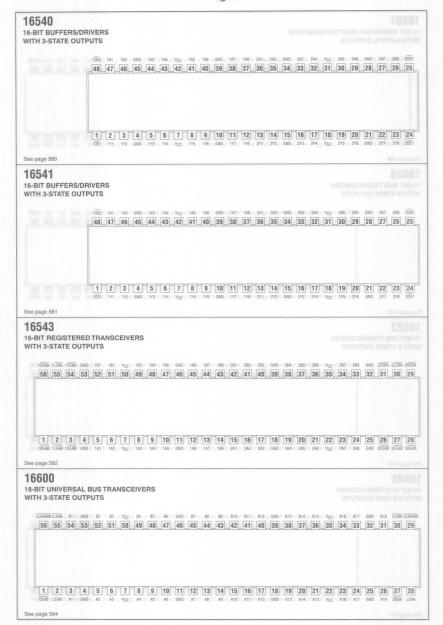


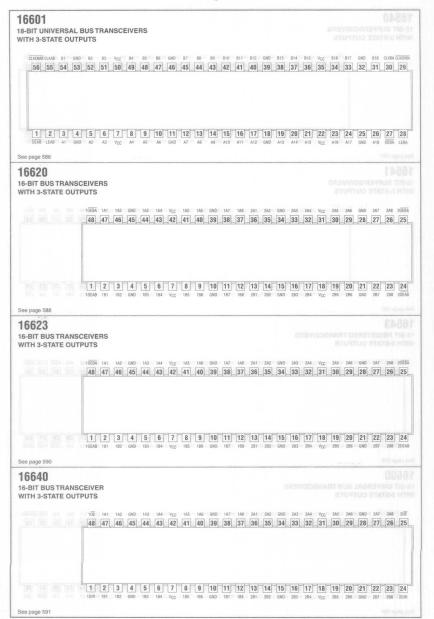


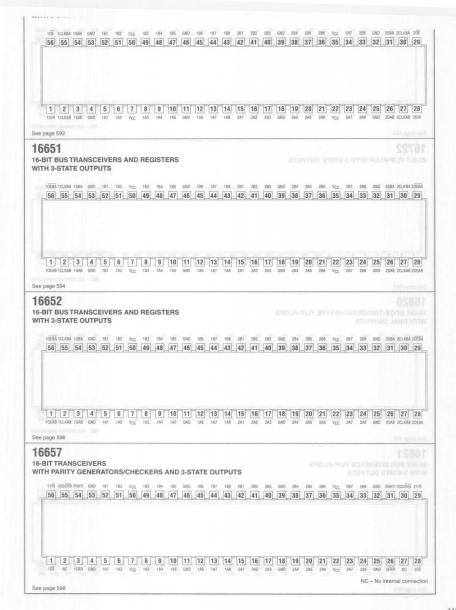
# Pin Assignments 74 73 72 71 70 69 68 67 66 65 64 63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 See page 556 16334 16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS CLK A1 A2 GND A3 A4 $V_{CC}$ A5 A6 GND A7 A8 A9 A10 GND A11 A12 $V_{CC}$ A13 A14 GND A15 A16 $\overline{LE}$ 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 OE Y1 Y2 GND Y3 Y4 VCC Y5 Y6 GND Y7 Y8 Y9 Y10 GND Y11 Y12 VCC Y13 Y14 GND Y15 Y16 NC NC - No internal connection See page 558 16344 1-BIT TO 4-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS OE4 881 882 GND 883 884 VCC 8A 781 782 GND 783 784 7A 6A 681 682 GND 683 684 5A VCC 5B1 582 GND 5B3 5B4 OE3 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32 31 30 29 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 See page 560 16373 16-BIT TRANSPARENT LATCHES WITH 3-STATE OUTPUTS ILE 1D1 1D2 GND 1D3 1D4 V<sub>CC</sub> 1D5 1D6 GND 1D7 1D8 2D1 2D2 GND 2D3 2D4 V<sub>CC</sub> 2D5 2D6 GND 2D7 2D8 2LE 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 See page 562

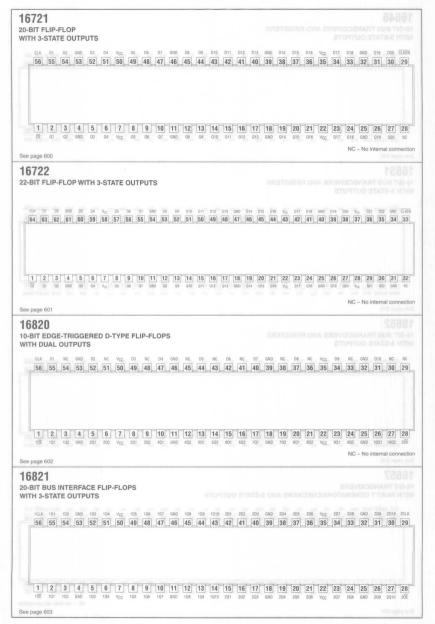


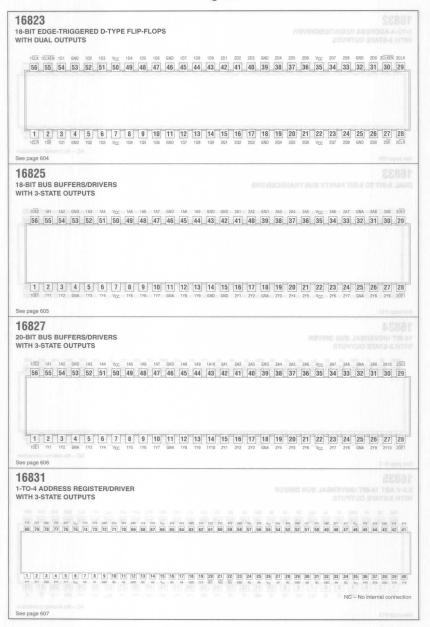




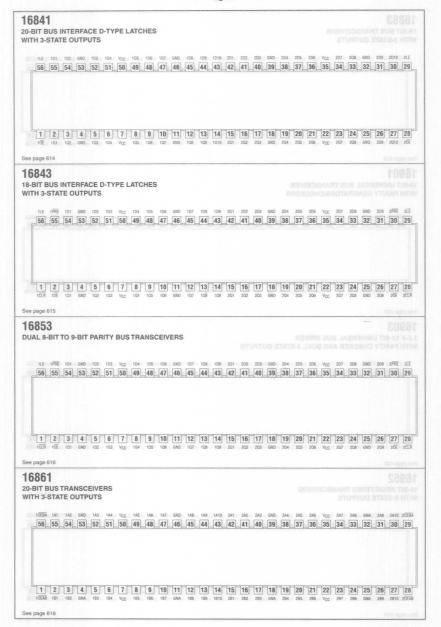


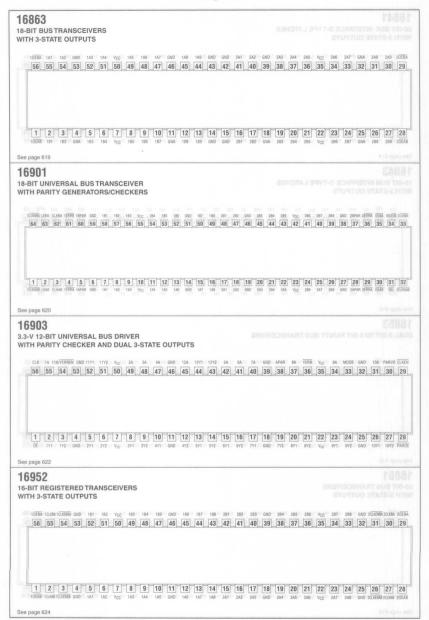


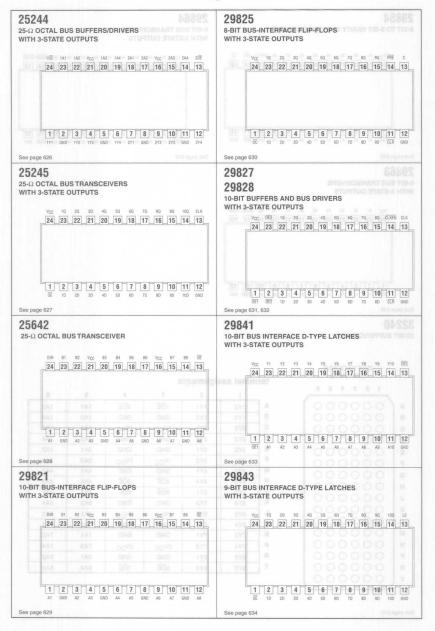


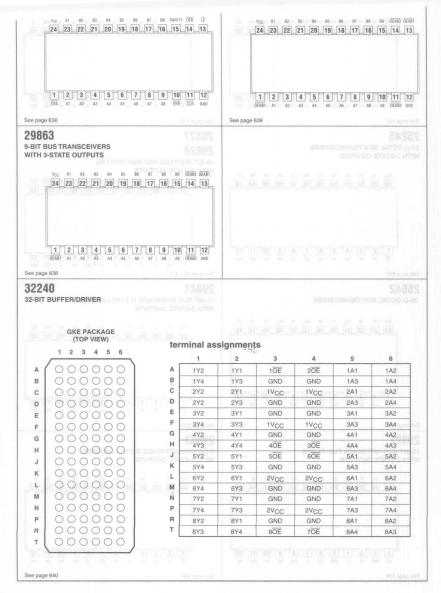


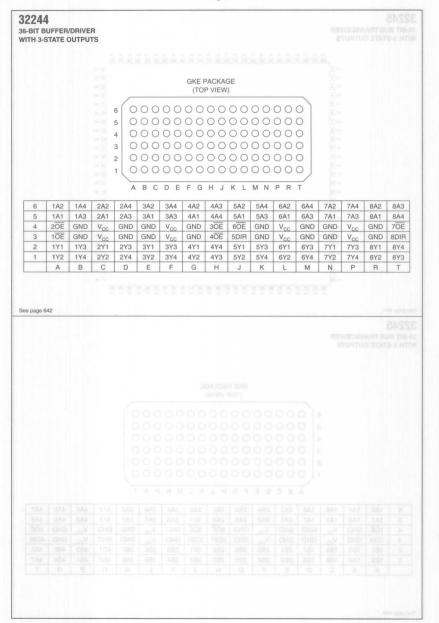
1 2 4Y1 3Y1	3 4 5 GND 2Y1 1Y		8 9 GND A2	10 11 GND A3	12 13 V <sub>CC</sub> NC			16 17 DE1 DE			0 21	22 V <sub>CC</sub>	23 GND				27 2 Voc 4	8 29 97 3Y		31 297	32
See page 608																	NC	– No i	nterna	l con	
16833																				25	88
DUAL 8-BI	TTO 9-BI	r Parity	BUSTE	RANSCI	EIVERS	•															
10EA 10	R 1PARITY GND	181 182	VCC 18	13 184	1B5 GND	186	187	188 2	B1 282	283	GND	284	285	286	VCC	287	288	GND :	PARITY	2CLR	20EA
56 5	5 54 53	52 51	50 4	9 48	47 46	45	44	43 4	2 41	40	39	38	37	36	35	34	33	32	31	30	29
		-			- 14 - 1			. Hed		<b>—</b>		-	7	4	No	7		-	7	rF	- Total
1 0EB 10	LK 1ERR GND				10 11 1A5 GND	12 1A6			15 16 A1 2A2	17 2A3	GND	19 2A4	20 2A5	21 2A6	VCC	23 2A7	24 2A8	GND	26 2ERR	27 2CLK	28 20E8
See page 610																				08 0	THE R
16834																					
16-BIT UN WITH 3-ST			IVER																		
GND NO			V <sub>CC</sub> A4	110	A6 GND	100	1116		10 A11	A12	GND		-	A15			A17		_	CLK	_
56_55	54_53	5251	50 49	48_4	17 46	45_	44	43 4	2 41	40	39	38	37	36	35	34	33	32	31	30	29
1 2	3 4	5 6	7 7 8	9 1	0 11	12	13	14 1	5 16	17	18	19	20	21	22	23	24	25	26	27	28
NC NO		Y2 Y3	V <sub>CC</sub> Y4		Y6 GND	Y7	Y8		10 Y11	Y12	GND	Y13	Y14	Y15	Voc	Y16	Y17	GND	Y18	ŌĒ	LE
See page 612																	NC	– No	interna	l con	necti
16835																				18	
3.3-V ABT			L BUS I	DRIVER																	
WITH 3-ST		A2 A3	V <sub>CC</sub> A	4 A5	A6 GND	A7			10 A11		GND	A13	A14	A15		A16	A17	-		CLK	
GND N	C A1 GNE							43	12 41	40	39	38	37	36	35	34	33	32	31	30	29
			50_4	9 48	47 46	45	44	43	41	140	100	177			100	0.4	100	OL	10.1	00	23

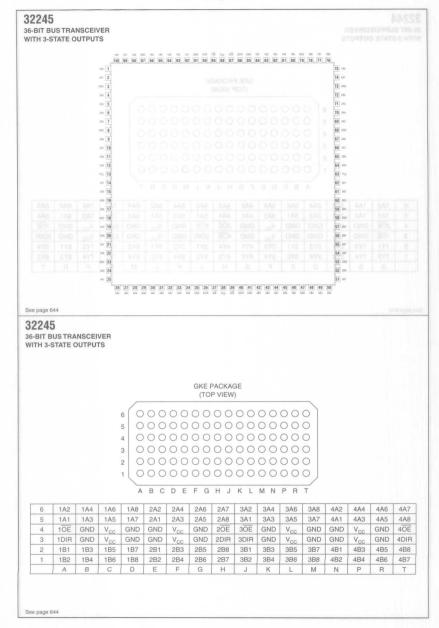


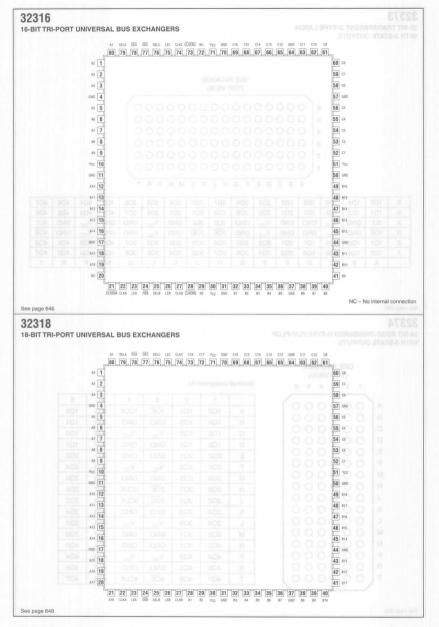












# 

GKE PACKAGE

ABCDEFGHJKLMNPRT

6	1D2	1D4	1D6	1D8	2D2	2D4	2D6	2D7	3D2	3D4	3D6	3D8	4D2	4D4	4D6	4D7
5	1D1	1D3	1D5	1D7	2D1	2D3	2D5	2D8	3D1	3D3	3D5	3D7	4D1	4D3	4D5	4D8
4	1LE	GND	V <sub>cc</sub>	GND	GND	V <sub>cc</sub>	GND	2LE	3LE	GND	V <sub>cc</sub>	GND	GND	V <sub>cc</sub>	GND	4LE
3	10E	GND	V <sub>cc</sub>	GND	GND	V <sub>cc</sub>	GND	2OE	3OE	GND	V <sub>cc</sub>	GND	GND	V <sub>CC</sub>	GND	40E
2	1Q1	1Q3	1Q5	1Q7	2Q1	2Q3	2Q5	2Q8	3Q1	3Q3	3Q5	3Q7	4Q1	4Q3	4Q5	4Q8
1	1Q2	1Q4	1Q6	1Q8	2Q2	2Q4	2Q6	2Q7	3Q2	3Q4	3Q6	3Q8	4Q2	4Q4	4Q6	4Q7
	Α	В	С	D	E	F	G	Н	J	K	L	M	N	P	R	Т

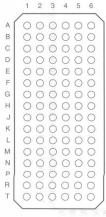
See page 650

#### 32374

32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

> GKE PACKAGE (TOP VIEW)

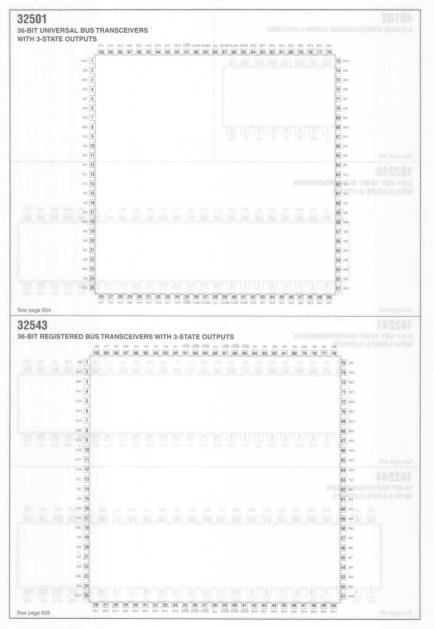
(TOP VIEW)

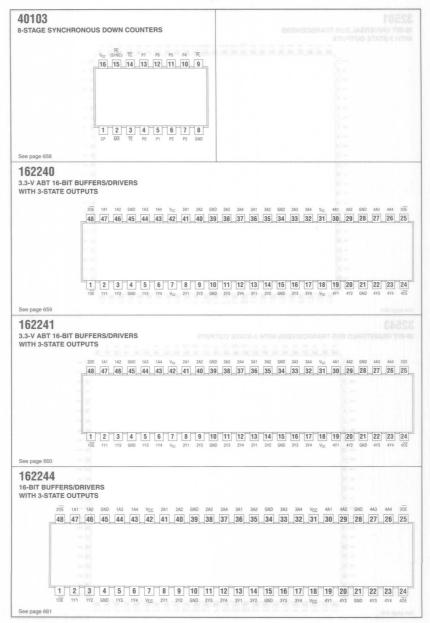


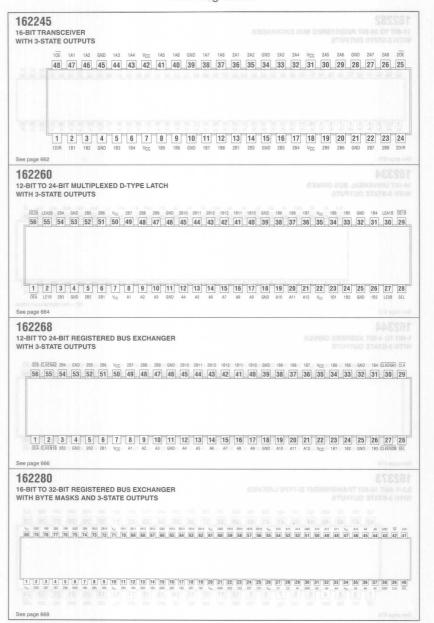
terminal assignments

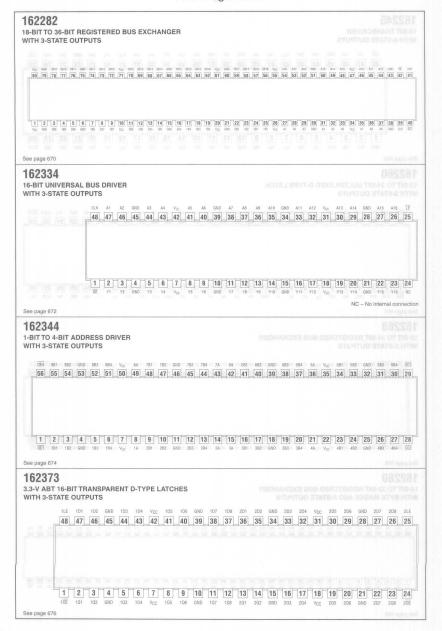
	1	2	3	4	5	6
Α	1Q2	1Q1	1OE	1CLK	1D1	1D2
В	1Q4	1Q3	GND	GND	1D3	1D4
С	1Q6	1Q5	V <sub>cc</sub>	V <sub>cc</sub>	1D5	1D6
D	1Q8	1Q7	GND	GND	1D7	1D8
Е	2Q2	2Q1	GND	GND	2D1	2D2
F	2Q4	2Q3	V <sub>CC</sub>	V <sub>CC</sub>	2D3	2D4
G	2Q6	2Q5	GND	GND	2D5	2D6
Н	2Q8	2Q7	2OE	2CLK	2D7	2D8
J	3Q2	3Q1	3OE	3CLK	3D1	3D2
K	3Q4	3Q3	GND	GND	3D3	3D4
L	3Q6	3Q5	V <sub>CC</sub>	V <sub>CC</sub>	3D5	3D6
М	3Q8	3Q7	GND	GND	3D7	3D8
N	4Q2	4Q1	GND	GND	4D1	4D2
P	4Q4	4Q3	V <sub>CC</sub>	V <sub>CC</sub>	4D3	4D4
R	4Q6	4Q5	GND	GND	4D5	4D6
Т	4Q7	4Q8	4OE	4CLK	4D8	4D7

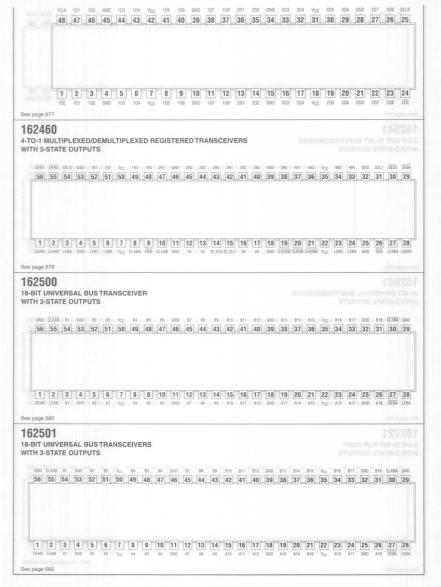
See page 652



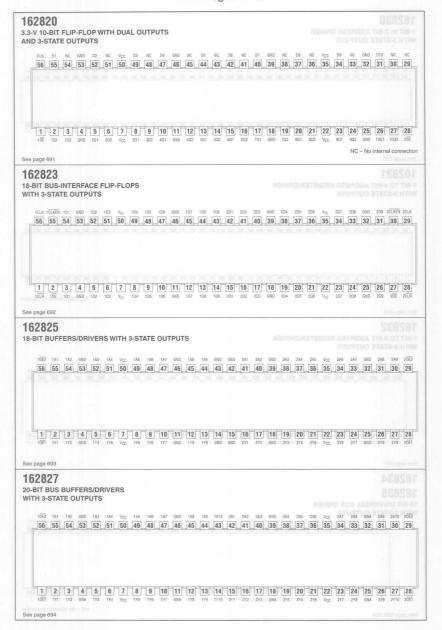




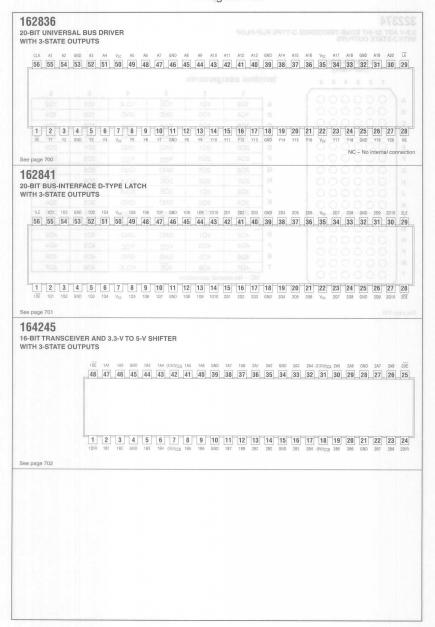




<b>62525</b> -BIT REGISTEREI ITH 3-STATE OUT		TRA	NSC	EIV	ER																			
SEL CLKAB B1 GNC 56 55 54 53			0.0	84 <b>49</b>	85 48	86 47	GND 46	87 45	88	89 43	810	811	B12	GND 39	813	814 37	B15	Vcc 35	B16	B17		B18	30	
1 2 3 4 CLKENAB DEAB A1 GNO					9 A5	10 A6	11 GND	12 A7	13 A8		15 A10	16 A11	17 A12		19 A13			22 Vcc			25 GND	A18	OEBA	
62541 8-V ABT 16-BIT BITH 3-STATE OUT		RS/DI	RIVE	RS				8	RSN	(E)	215A)	AT O	SAS	nau	)BR	oax	eue	ntau		okas num		NIT.		52
		1A1 47																						
	1 10E1	2	3	4 GND	5 1Y3	6	7 V <sub>00</sub>	8	9 146	10 GND	11 1Y7	12 1Y8	13 2Y1	14 2Y2	15 GND	16 2Y3	17 2Y4	18 Vcc	19 2Y5	20 2Y6	21 GND	22	23	24
			_		_															_	_	-	019	
62601 BIT UNIVERSAL	PUTS	B3	VCC	84	B5											B14	B15		816	B17	GND	113 V 314	CLKBA	CLKEN
62601 BIT UNIVERSAL TH 3-STATE OUT  GENNA GLAS 81 GN  56 55 54 53	PUTS  82  3 52	B3 <b>51</b>	V <sub>CC</sub> 50	84 49	85 48	47	46		44	43	42	41	40	39	38	B14	B15 36	Vcc 35	816	B17	GND 32	818 31	CLXBA 30	29 28
56 55 54 53	PUTS  B2  B2  B 52  D A2	83 51 6 A3	V <sub>CC</sub> 50	84 49	85 48	10	46	12	13	43	42	41	40	39	38 19 A13	814 37 20 A14	815 36 21 A15	Vcc 35	816 34 34 A16	B17 33 33 24 A17	GND 32	818 31 26 A18	CLKBA 30	29 28 LEBA
62601 BIT UNIVERSAL TH 3-STATE OUT  CUEBUS CLASS   15 CM  56 55 54 52  1 2 3 4  6628 LEAB A1 GM  P page 688  62721  3-V 20-BIT FLIP-F	PUTS  B2  B2  B2  B2  B2  B2  B3  B2  B3  B3	83 51 51 6 A3	Vcc 50 Vcc Vcc	84 49	85 48	10	46	12	13	43	42	41	40	39	38 19 A13	814 37 20 A14	36 36 21 A15	Vcc 35]	816 34 34	817 333 24 A17	GND 32 25 GND GND	26 A18	27 068A	29 28 LEBA



162830 1-BIT to 2-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS	
173 752 000 714 754 56 75 754 753 752 771 750 690 680 677 665 654 653 652 61 650 559 555 557 5	111 V <sub>2</sub> 1102 770 000 1113 7113 000 1141 714 V <sub>2</sub> 1115 7713 000 1181 7144 V <sub>3</sub> 1115 7713 000 1181 7181 565 565 54 533 52 51 50 449 448 477 465 445 44 43 42 41
्त्रव १७ ७० ७० १० १० ६८ म म १०० म म १०० म म १०० म विहे हिंद सब ४०० मा	25   28   27   28   29   30   31   32   33   34   35   38   37   38   39   40   30   50   A3   A4   50   A1   54   500   A0   A8   50   211   118   500   217   117
162831 1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS	30-200 HI 162623 REST BUS-INTERFACE FUR-FLORE WITH S-STATE OUTPUTS
172 FRZ 006 372 FRZ No. 110 771 000 372 FRZ No. 110 771 000 372 FRZ NO 100 174 274 No. 274 FRZ 000 171 FRZ NO 175 000 174 000 177 76 75 74 773 772 771 770 60 68 67 66 65 64 63 62 61 60 59 55 57	THE VG. THE CTS DOC 117 277 DOC 317 GET VG. THE THE DOC 318 GET SEC. SEC. SEC. SEC. SEC. SEC. SEC. SEC.
1 2 3 4 5 8 7 8 9 10 11 12 13 14 15 16 17 16 19 20 21 22 23 24 47 27 00 27 17 18 5 14 00 5 5 17 18 5 14 00 5 5 17 18 5 14 00 5 5 18 18 18 18 18 18 18 18 18 18 18 18 18	M. $v_{\rm SC}$ As no GaO as no GNO as no $v_{\rm SC}$ are are one one of the NC – No internal connection
162832 1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS	SHAND OR 162825 18-BIT BUFFERSIDRIVERS WITH 3-STATE OUTP
172 272 040 372 472 V <sub>01</sub> 173 273 040 373 473 040 V <sub>12</sub> 040 174 274 374 474 040 64 63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46	115 275 V <sub>6.</sub> 376 475 600 600 V <sub>6.</sub> 176 274 600 376 476 445 44 43 42 41 40 39 38 37 36 35 34 33
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 47 371 040 271 171 V <sub>G</sub> AI 040 A2 040 A2 V <sub>G</sub> NC 040 CLK 0E 0E 0E 0E 0E	
162834 162835	SHORDS TO SHORD SHOP SHOP SHOP SHOP SHOP SHOP SHOP SHOP
	A12 GAD A13 A14 A15 M <sub>CC</sub> A19 A17 GAD A19 GLA GAD A10 GAD A19 GLA GAD A10 GAD



#### 322374 3.3-V ABT 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS GKE PACKAGE (TOP VIEW) terminal assignments 1 2 3 4 5 6 3 4 5 6 10E 1Q1 1CLK 1D1 1D2 В GND 1D4 В 1Q4 1Q3 GND 1D3 C C 1Q6 1Q5 Vcc Vcc 1D5 1D6 000000 D D 108 1Q7 GND GND 1D7 1D8 E 2Q1 GND GND 2D1 2D2 2Q2 000000 2Q4 2Q3 2D3 2D4 VCC VCC G G 2Q6 2Q6 GND GND 2D5 2D6 Н 2OE Н 2Q7 2Q8 2CLK 2D8 2D7 J 3Q2 3Q1 3OE 3CLK 3D1 3D2 3Q4 3Q3 GND GND 3D3 3D4 3Q6 3Q5 3D5 3D6 VCC VCC M 3Q8 3Q7 GND GND 3D7 3D8 M N 4Q2 4Q1 GND GND 4D1 4D2 N Р 4Q4 4Q3 4D3 4D4 VCC VCC P 4Q6 4Q5 GND GND 4D5 4D6 R 40E 4CLK 4Q8 NC - No internal connection See page 703

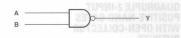
# FUNCTION AND ELECTRICAL CHARACTERISTICS

# FUNCTION AND ELECTRICAL CHARACTERISTICS

#### Logic Diagram

#### QUADRUPLE 2-INPUT POSITIVE-NAND GATES

- $\bullet$  Y =  $\overline{A \bullet B}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC	SN74 AC	CD74 AC	ACT	UNIT
Icc	MAX	22	4.4	36	3	17.4	10.2	0.02	0.04	0.02	0.04	0.04	0.02	0.08	0.04	mA
Іон	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	-24	-24	mA
lou	MAX	16	8	20	8	20	20	4	4	4	4	24	24	24	24	mA

PARAMETER	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC 3V	UNIT
Icc	MAX	0.02	0.08	0.02	0.02	7.5	0.02	0.01	0.01	mA
Юн	MAX	-24	-24	-8	-8	-6	-12	-24	-24	mA
lou	MAX	24	24	8	8	6	12	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11
tPLH	AorB	Υ	MAX	22	15	4.5	11	4.5	6	23	27	25	30	7.4	8.5	7.3	12.3
tPHL .	A or B	Υ	MAX	15	15	5	8	4	5.3	23	27	25	30	6.8	7	7.3	8.8

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	TAC 3A	ALVC 3V
tPLH .	A or B	Υ	MAX	9.5	10.8	8.5	9	13	8.5	4.3	3
tPHL .	AorB	Υ	MAX	8	13.2	8.5	9	13	8.5	4.3	3

UNIT:ns

QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

 $\bullet$  Y =  $\overline{A \bullet B}$ 

1A	- 1Y
	SAA = Y
3A 3B 2 OOO   2	
4A ————————————————————————————————————	- 4Y

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	нс	UNIT
Icc	MAX	22	4.4	3	0.02	mA
Vон	MAX	5.5	5.5	5.5	Vcc	V
lor	MAX	16	8	8	4	mA

SWITCHING CHARACTERISTICS

OVVII OTITIVO 1	IIIAIIAOI	LINOTICO	1				
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	нс
tplH	A or B	Y	MAX	55	32	54	31
tPHL .	A or B	Υ	MAX	15	28	28	25

# **QUADRUPLE 2-INPUT**

- **POSITIVE-NOR GATES**
- $\bullet$  Y =  $\overline{A + B}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

**Logic Diagram** 



NECOMINICIANE	DUPENATING	CONDI	ITUNS	_	_	_	_	_		_	_		20011		100
PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	n (F)	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	CD74 AC	ACT 11	UNIT
lcc	MAX	27	5.4	45	4	20.1	13	0.02	0.04	0.02	0.04	0.04	0.08	0.04	mA
Іон	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	-24	mA
lou	MAX	16	8	20	8	20	20	4	4	4	4	24	24	24	mA

PARAMETER	MAX or MIN	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	TAC TAC	UNIT
lcc	MAX	0.08	0.02	0.02	-31	0.02	0.01	mA
Іон	MAX	-24	-8	-8	-6	-12	-24	mA
lou	MAX	24	8	8	6	12	24	mA

SWITCHING CHARACTERISTICS

			_	-			_	_			_					
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	s	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	CD74 AC	ACT 11
tPLH .	A or B	Y	MAX	22	15	5.5	12	4.5	6.5	23	27	25	32	6.9	11.5	10.6
tPHL .	A or B	Y	MAX	15	15	5.5	10	4.5	5.3	23	27	25	32	6.4	11.5	8.7

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V
tPLH .	A or B	Υ	MAX	12.2	8.5	8.5	13	8.5	4.4
tPHL .	A or B	Y	MAX	12.2	8.5	8.5	13	8.5	4.4



RECOMMENDE	D OPERATING	CONDIT	IONS									
PARAMETER	MAX or MIN	TTL	LS	S	ALS	SN74 HC	CD74 HC	CD74 HCT	UNIT	āA.		
lcc	MAX	22	4.4	36	4	0.02	0.04	0.04	mA	20.1		
Vон	MAX	5.5	8	5.5	8	0.05	Vcc	Vcc	٧	3		
lou	MAX	16	0.1	20	0.1	4	4	4	mA	US		

SWITCHING C	HARACTER	RISTICS	_			710	1 37	I V.	1/1	1010		
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	SN74 HC	CD74 HC	CD74 HCT		
							100	nc.	nc	пы		
tPLH	A or B	Υ	MAX	45	32	7.5	50	31	30	36		
tphl.	A or B	Υ	MAX	15	28	7	13	25	30	36		

# HEX **INVERTERS**

- Logic Diagram

- $Y = \overline{A}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

RECOMMENDED	<b>OPERATING</b>	COND	ITIONS

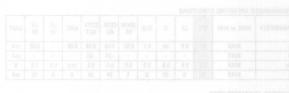
RECOMMENDE	D OPERATING	CONDI	TIONS		,											
PARAMETER	MAX or MIN	ŤTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	UNIT
Icc	MAX	33	6.6	54	4.2	26.3	15.3	0.02	0.04	0.02	0.04	0.04	0.02	0.08	0.04	mA
Іон	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	-24	-24	mA
lou	MAX	16	8	20	8	20	20	4	4	4	4	24	24	24	24	mA

PARAMETER	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	TAC 3A	ALVC 3V	UNIT
lcc	MAX	0.02	0.08	0.02	0.02		0.02	0.01	0.01	mA
Іон	MAX	-24	-24	-8	-8	-6	-12	-24	-24	mA
lot	MAX	24	24	8	8	6	12	24	24	mA

# SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11
tPLH	A or B	Y	MAX	22	15	4.5	11	5	6	24	26	25	29	7.1	7.5	6.5	9.7
tPHL .	A or B	Υ	MAX	15	15	5	8	4	5.3	24	26	25	29	6	7	6.5	9.6

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 ACT	CD74 ACT	АНС	АНСТ	LV 3V	LV 5V	LVC 3V	ALVC 3V
tPLH	A or B	Υ	MAX	9	9.3	8.5	8.5	12	8.5	4.5	2.8
<b>TPHL</b>	AorB	Υ	MAX	8.5	9.3	8.5	8.5	12	8.5	4.5	2.8



U04

HEX **INVERTERS** 





 $\bullet$  Y =  $\overline{A}$ 

Unbuffered Output

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	AHC	LV 3V	LV 5V	LVC 3V	UNIT
Icc	MAX	0.02	0.04	0.02		0.02	0.01	mA
Іон	MAX	-4	-4	-8	-6	-12	-24	mA
lou	MAX	4	4	8	6	12	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	AHC	LV 3V	LV 5V	LVC 3V
tplh	A or B	Υ	MAX	20	21	8	13	8	3.8
tphl.	AorB	Υ	MAX	20	21	8	13	8	3.8

UNIT: ns

Logic Diagram 05 **HEX INVERTERS** WITH OPEN-COLLECTOR **OUTPUTS**  $\bullet$  Y =  $\overline{A}$ 

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	SN74 HC	CD74 AC	CD74 ACT	AHC	LV 3V	LV 5V	UNIT
Icc	MAX	33	6.6	54	4.2	0.02	0.08	0.08	0.02	-	0.02	mA
Іон	MAX	-	-	-	-	-	-24	-24	-	-	-	mA
Vон	MAX	5.5	5.5	5.5	5.5	5.5	5.5	5.5	Vcc	5.5	5.5	V
lou	MAX	16	8	20	8	4	24	24	8	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	SN74 HC	CD74 AC	CD74 ACT	AHC	LV 3V	LV 5V
tPLH	A or B	Y	MAX	55	32	7.5	54	29				12	8.5
tPHL .	A or B	Υ	MAX	15	28	7	14	21		-	-	12	8.5
tPLZ	А	Υ	MAX	-	-	-	187	-	8.2	9.3	8.5	-	-
tPZL	A	Υ	MAX	1.	-	-	-	-	6.5	10.8	8.5	-	-

# **HEX INVERTER BUFFERS/DRIVERS** WITH OPEN-COLLECTOR **HIGH-VOLTAGE OUTPUTS**

 $\bullet$  Y =  $\overline{A}$ 



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	TA TA	LV 5V	3V	UNIT
lcc	MAX	51	60	(15)	0.02	0.01	mA
Іон	MAX	0.25	0.25	13	±0.0025	H : 1	mA
Vон	MAX	30	30	5.5	5.5	5.5	V
loc	MAX	40	40	8	16	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	LV 3V	LV 5V	LVC 3V
tPLH	A or B	Y	MAX	15	15	12	8.5	3.7
<b>TPHL</b>	A or B	Y	MAX	23	20	12	8.5	3.7

UNIT: ns

07

**HEX BUFFERS/DRIVERS** WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

Y = A

**Logic Diagram** 



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	LV 3V	LV 5V	LVC 3V	UNIT
Icc	MAX	41	45	-	0.02	0.01	mA
Іон	MAX	0.25	0.25	-	±0.0025	-	mA
Vон	MAX	30	30	5.5	5.5	5.5	٧
Ini	MAX	40	40	8	16	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	LV 3V	LV 5V	TAC TAC
tPLH	A or B	Υ	MAX	15	10	12	8.5	2.9
tphl.	A or B	Υ	MAX	26	30	12	8.5	2.9

Advanced CMOS (11000 Series)

• 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logia Diagram

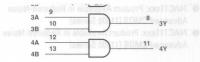
RECOMMENDE	D OPERATING	CONDI	IUNS		,	-	_	-								
PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	UNIT
Icc	MAX	33	8.8	57	4	24	12.9	0.02	0.04	0.02	0.04	0.04	0.02	0.08	0.04	mA
Іон	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	-24	-24	mA
lou	MAX	16	8	20	8	20	20	4	4	4	4	24	24	24	24	mA

PARAMETER	MAX or MIN	SN74 ACT	CD74 ACT	AHC	АНСТ	LV 3V	LV 5V	LVC	ALVC	UNIT
Icc	MAX	0.02	0.08	0.02	0.02	-	0.02	0.01	0.01	mA
Іон	MAX	-24	-24	-8	-8	-6	-12	-24	-24	mA
lou	MAX	24	24	8	8	6	12	24	24	mA

# SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	s	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	AC1
tPLH .	A or B	Y	MAX	27	15	7	14	5.5	6.6	25	27	30	38	6.9	8.5	8.7	9
tPHL .	A or B	Υ	MAX	19	20	7.5	10	5.5	6.3	25	27	30	38	6.5	7.5	8.7	8.2

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC	ALVO
tPLH .	A or B	Y	MAX	10	12.9	9	9	14	9	4.1	2.9
tPHL .	A or B	Υ	MAX	10	12.9	9	9	14	9	4.1	2.9



RECOMMENDED OPERATING CONDITIONS

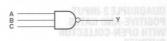
PARAMETER	MAX or MIN	TTL	LS	S	ALS	F	SN74 HC	UNIT
lcc	MAX	33	8.8	- 57	4.2	26.3	15.3	mA
Іон	MAX	36	0.1	0.25	0.1	1.	-	mA
Vон	MAX	5.5	5.5	5.5	5.5	5.5	Vcc	mA
lou	MAX	16	8	20	8	20	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	F	SN74 HC
tPLH	A or B	Y	MAX	32	35	10	54	9.6	31
tPHL .	A or B	Υ	MAX	24	35	10	15	4.8	25

# TRIPLE 3-INPUT POSITIVE-NAND GATES

- Y = A•B•C
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	UNIT
lcc	MAX	16.5	3.3	27	2.2	13	7.7	0.02	0.04	0.02	0.04	0.04	0.02	0.08	0.04	mA
Іон	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	-24	-24	mA
lou	MAX	16	8	20	8	20	20	4	4	4	4	24	24	24	24	mA

PARAMETER	MAX or MIN	SN74 ACT	CD74 ACT	LV 3V	LV 5V	TAC 3A	ALVC	UNIT
Icc	MAX	0.04	0.08	-	0.02	0.01	0.01	mA
Гон	MAX	-24	-24	-6	-12	-24	-24	mA
lou	MAX	24	24	6	12	24	24	mA

SWITCHING CHARACTERISTICS

SWITCHING C	HARACTERI	STICS								Symm				42, 145	n		
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11
tPLH	A, B or C	Y	MAX	22	15	4.5	11	4.5	6	24	30	19	36	6.7	8	12.2	8.9
<b>TPHL</b>	A, B or C	Υ	MAX	15	15	5	10	4.5	5.3	24	30	19	36	7	6.5	12.2	8.2

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 ACT	CD74 ACT	LV 3V	LV 5V	LVC 3V	ALVO
tplh	A, B or C	Υ	MAX	10	-	13.5	9	4.9	3
tPHL .	A, B or C	Υ	MAX	9.5	13.5	13.5	9	4.9	3



# TRIPLE 3-INPUT **POSITIVE-AND GATES**

- Y = A•B•C
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

RECOMMENDE	D OPERATING	CONDI	IUNS	(A) (M)	At 12				NO F					2.1	III	11185	to XAI
PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	ACT 11	SN74 ACT	LV 3V	LV 5V	UNIT
lcc	MAX	6.6	42	3	18	9.7	0.02	0.04	0.02	0.04	0.04	0.02	0.04	0.02	-	0.02	mA
Іон	MAX	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	-24	-24	-6	-12	mA
lou	MAX	8	20	8	20	20	4	4	4	4	24	24	24	24	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	s	ALS	AS	F	SN74 HC		SN74 HCT	CD74 HCT	AC 11	SN74 AC	ACT 11	SN74 ACT
tPLH .	A, B or C	Υ	MAX	15	7	13	6	6.6	25	30	21	42	6.5	8.5	9.6	10.5
tPHL .	A, B or C	Υ	MAX	20	7.5	10	5.5	6.5	25	30	21	42	6.9	7.5	8.7	10.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	LV 3V	LV 5V
tPLH	A, B or C	Y	MAX	14	9
tPHL .	A, B or C	Y	MAX	14	9

 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 AC	CD74 AC	SN74 ACT	CD74 ACT	AHC	AHCT	UNIT
lcc	MAX	60	21	0.02	0.04	0.02	0.04	0.02	0.08	0.02	0.08	0.02	0.02	mA
Іон	MAX	-0.8	-0.4	-4	-4	-4	-4	-24	-24	-24	-24	-8	-8	mA
lou	MAX	16	8	4	4	4	4	24	24	24	24	8	8	mA

PARAMETER	MAX or MIN	LV 3V	LV 5V	LVC 3V	ALVC 3V	UNIT
Icc	MAX		0.02	0.01	0.01	mA
Іон	MAX	-6	-12	-24	-24	mA
lou	MAX	6	12	24	24	mA

SWITCHING CHARACTERISTICS

OVVII OTTITAL O	HAHAUILI	1101100											
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC		CD74 HCT	SN74 AC	CD74 AC	SN74 ACT	CD74 ACT
tPLH	A or B	Υ	MAX	22	22	31	41	40	57	11	10.5	12.5	14.5
tPHL .	A or B	Υ	MAX	22	22	31	41	40	57	9.5	10.5	11	9.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC 3V
tPLH	A or B	Υ	MAX	12	9	18.5	12	6.4	3.4
tPHL .	A or B	Υ	MAX	12	9	18.5	12	6.4	3.4

HEX INVERTER
BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

 $\bullet$  Y =  $\overline{A}$ 

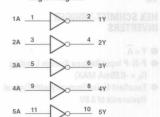
RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
Icc	MAX	51	mA
Vон	MAX	15	V
lou	MAX	40	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
tplH	A	Υ	MAX	15
tPHL .	A	Υ	MAX	23

Logic Diagram



6A 13 6

TIRU 2.3 VIIIA ve SAM (ETTINA)
Am 0.0 XAM
Am 0.0 XAM

HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

Y = A

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Logic Diagram

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
lec	MAX	41	6.6
Vон	MAX	15	V
lou	MAX	40	mA

SWITCHING CHARACTERISTICS

SWITCHING C	HANACIE	1131163	_	
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
tPLH .	A	Υ	MAX	15
tPHL .	A	Υ	MAX	26

# HEX SCHMITT-TRIGGER INVERTERS

- $\bullet$  Y =  $\overline{A}$
- P-N-P Input Reduce System Loading (I<sub>IL</sub> = -0.05mA MAX)
- Excellent Noise Immunity with Typical Hysteresis of 0.8V

RECOMMENDED OPERATING CONDITIONS

TILCONNINILIADE	D OI LIMINO	T	T
PARAMETER	MAX or MIN	LS	UNIT
lcc	MAX	30	mA
Гон	MAX	-0.4	mA
lou	MAX	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
tPLH	A or B	Y	MAX	20
tPHL	A or B	Y	MAX	30

UNIT: IIS

Logic Diagram

1A .	1		2	1Y	
2A	3	1	4	2Y	

EX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HON-VOLTAGE OUTPUTS

A=T

# DUAL 4-INPUT POSITIVE-NAND GATES

- $Y = \overline{A \cdot B \cdot C \cdot D}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

# Logic Diagram





RECOMMENDED OPERATING CONDITIONS

NECOMMENDE	U UPENATING	CUIVUI	ITUIVS	WI.	VIII		34.	11001	MINI	DIME.							
PARAMETER	MAX or MIN	TTL	LS	s	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	CD74 AC	ACT 11	CD74 ACT	LV 2V	LV 5V	UNIT
Icc	MAX	11	2.2	18	1.5	8.7	5.1	0.02	0.04	0.04	0.04	0.08	0.04	0.08	. 8	0.02	mA
Іон	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-24	-24	-24	-24	-6	-12	mA
lou	MAX	16	8	20	8	20	20	4	4	4	24	24	24	24	6	12	mA

SWITCHING CHARACTERISTICS AND MICHAEL S 24 EUR 21 MM WARM TISTUD TURN FETIMAL

SAALLCHIIAO C	HANAGILINGII	00	1016   211   2					_								
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	CD74 AC	ACT 11	CD74 ACT
tPLH	A, B, C or D	Υ	MAX	22	15	4.5	11	5	6	28	30	42	6.7	12.2	9.1	13.5
tPHL .	A, B, C or D	Υ	MAX	15	15	5	10	4.5	5.3	28	30	42	7.3	12.2	9.2	13.5

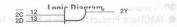
PARAMETER	INPUT	OUTPUT	MAX or MIN	LV 3V	LV 5V
tPLH	A, B, C or D	Y	MAX	11.5	8
tPHL .	A, B, C or D	Y	MAX	11.5	8





# 2

- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	ACT 11	LV 3V	LV 5V	UNIT
lcc	MAX	4.4	2.3	12	7.3	0.02	0.04	0.04	0.04	0.04	-	0.02	mA
Іон	MAX	-0.4	-0.4	-2	-1	-4	-4	-4	-24	-24	-6	-12	mA
lou	MAX	8	8	20	20	4	4	4	24	24	6	12	mA

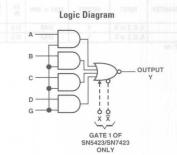
### SWITCHING CHARACTERISTICS

PARAMETER	. INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	ACT 11	LV 3V	LV 5V
tPLH .	A, B, C or D	Y	MAX	15	15	6	5.3	28	33	41	8.8	9.8	12	6
tPHL .	A, B, C or D	Υ	MAX	20	10	6	5.5	28	33	41	6.9	8.9	12	8

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# DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE

 $\bullet$  Y =  $\overline{G(A + B + C + D)}$ 

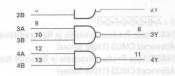


## RECOMMENDED OPERATING CONDITIONS

		1	
PARAMETER	MAX or MIN	TTL	UNIT
Icc	MAX	19	mA
Іон	MAX	-0.8	mA
Inc	MAX	16	mA

# SWITCHING CHARACTERISTICS

OVVITORING C	IMINUTEI	1101100		_
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
tPLH .	A or B	Υ	MAX	22
<b>TPHL</b>	A or B	Υ	MAX	15



# RECOMMENDED OPERATING CONDITIONS

TIE O O ITTITE I TO E	D OT BIDITING		10.110	_
PARAMETER	MAX or MIN	TTL	LS	UNIT
Icc	MAX	22	4.4	mA
Vон	MAX	15	15	V
lou	MAX	16	8	mA

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
tPLH	A or B	Y	MAX	24	32
tphL .	A or B	Y	MAX	17	28

UNIT: ns

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# **TRIPLE 3-INPUT POSITIVE-NOR GATES**

- $\bullet$  Y =  $\overline{A + B + C}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise

# Logic Diagram



Advanced CMOS (11000 Series)

# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	ACT 11	LV 3V	LV 5V	UNIT
Icc	MAX	26	6.8	4	17.1	12	0.02	0.04	0.04	0.04	0.04		0.02	mA
Іон	MAX	-0.8	-0.4	-0.4	-2	-1	-4	-4	-4	-24	-24	-6	-12	mA
lou	MAX	16	8	8	20	20	4	4	4	24	24	6	12	mA

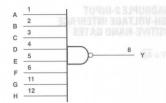
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	ACT 11	LV 3V	LV 5V
tPLH de	A, B or C	Y	MAX	15	15	15	5.5	5.5	23	29	35	7.7	10.1	14	9
TPHL 2	A. B or C	Y	MAX	11	15	9	4.5	4.5	23	29	35	8.1	9.4	14	9

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# 8-INPUT POSITIVE-NAND GATES

- Y = A•B•C•D•E•F•G•H
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

# Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	ACT 11	UNIT
Icc	MAX	6	1.1	10	0.9	4.9	4	0.02	0.04	0.04	0.04	0.04	mA
Іон	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-24	-24	mA
lou	MAX	16	8	20	8	20	20	4	4	4	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	ACT 11
tPLH .	A thru H	Y	MAX	22	15	6	10	5	5.5	33	39	42	7.2	8.5
tPHL.	A thru H	Υ	MAX	15	20	7	12	4.5	5	33	39	42	7.4	8.7

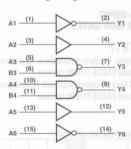
UNIT: ns

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# **DELAY ELEMENTS**

- Delay Elements for Generating Delay Line
- Inverting and Non-inverting Elements
- Buffer NAND Elements Rated at I<sub>OL</sub> of 12/24mA
- P-N-P Inputs Reduce Fan-In (I<sub>IL</sub> = -0.2mA MAX)
- $\bullet$  Worst Case MIN/MAX Delays Guaranteed Across Temperature and  $V_{\text{CC}}$  Range

# Logic Diagram



RECOMMENDED RECOMMENDED OPERATING CONDITIONS

	PARAMETER	MAX or MIN	LS	UNIT
Icc	PER STORY	MAX	20	mA
Іон	Y3, Y4 outputs	MAX	-1.2	mA
IUH	All other outputs	MAX	-0.4	mA
1	Y3, Y4 outputs	MAX	24	mA
IOL	All other outputs	MAX	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
tPLH	A1 AC	V1 V0	MAY	65
tPHL 200	A1, A6	Y1, Y6	MAX	45
tplh .	A2 A5	Y2, Y5	MAN	80
tPHL .	A2, A5	Y2, Y5	MAX	95
tPLH B	A3, B3	Vo Va	MAY	15
tPHL .	A4, Y4	Y3, Y4	MAX	15
UNIT: ns				

# QUADRUPLE 2-INPUT POSITIVE-OR GATES

● Y = A + B



# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	UNIT
Icc	MAX	38	9.8	68	4.9	26.6	15.5	0.02	0.04	0.02	0.04	0.04	0.02	0.08	0.04	mA
Іон	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	-24	-24	mA
lou	MAX	16	8	20	8	20	20	4	4	4	4	24	24	24	24	mA

PARAMETER	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	TAC TAC	ALVC	UNIT
Icc	MAX	0.02	0.08	0.02	0.02	0.02	0.02	0.01	0.01	mA
Іон	MAX	-24	-24	-8	-8	-6	-12	-24	-24	mA
lor	MAX	24	24	8	8	6	12	24	24	mA

## SWITCHING CHARACTERISTICS

C T T C T T T T T T T T T T T T T T T T	AIIAO I EIIIO I I O	T	T		- 0				200				8 10 7		
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC
tPLH	A or B	Y	MAX	15	22	7	14	5.8	6.6	25	27	30	36	6.7	8.5
tPHL .	A or B	Y	MAX	22	22	7	12	5.8		25	27	30	36	5.9	7.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	АНСТ	LV 3V	LV 5V	LVC 3V	ALVC 3V
tPLH	A or B	Y	MAX	9.5	9	10	12.1	8.5	9	13	8.5	3.8	2.8
tPHL	A or B	Y	MAX	9.5	8	10	12.1	8.5	9	13	8.5	3.8	2.8

# QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS WITH OPEN-COLLECTOR OUTPUTS

 $\bullet$  Y =  $\overline{A + B}$ 

1A	1	1Y
1B ——		AD RU-B
2A		2Y
2B ——		
3A		3Y
3B ——		31
4A		4Y
4B		TARBED OF

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	UNIT
Icc	MAX	16.5	13.8	9	mA
Vон	MAX	5.5	5.5	5.5	V
lou	MAX	48	24	24	mA

SWITCHING CHARACTERISTICS

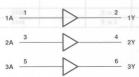
PARAMETER	INPUT	OUTPUT	MAX or MIN	ΠL	LS	ALS
tPLH	A or B	Υ	MAX	15	32	33
tPHL .	A or B	Y	MAX	18	28	12

HMIT: ns

Logic Diagram

# 35 HEX NONINVERTERS WITH OPEN-COLLECTOR OUTPUTS

Y = A

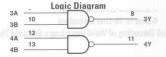


RECOMMENDED OPERATING CONDITIONS

NEGOIVIIVIEIVDE	D OF LINATING	T	110143
PARAMETER	MAX or MIN	ALS	UNIT
Icc	MAX	63	mA
Vон	MAX	5.5	V
lor	MAX	8	mA

SWITCHING CHARACTERISTICS

SWITCHING C	HANAGIEN	1131163		
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
tplH	А	Υ	MAX	50
tPHL.	A	Υ	MAX	14



RECOMMENDED OPERATING CONDITIONS

TIE O O WINTE TO E	D OI LIBITING	001101	10110				
PARAMETER	MAX or MIN	TTL	LS	S	ALS	F	UNIT
Icc	MAX	54	12	80	7.8	33	mA
Іон	MAX	-1.2	-1.2	-3	-2.6	-15	mA
lot.	MAX	48	24	60	24	64	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	F
tPLH .	A or B	Υ	MAX	22	24	6.5	8	6.5
<b>TPHL</b>	A or B	Υ	MAX	15	24	6.5	7	5

UNIT: ns

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QUADRUPLE 2-INPUT
POSITIVE-NAND BUFFERS
WITH OPEN-COLLECTOR OUTPUTS

 $\bullet$  Y =  $\overline{A \cdot B}$ 

**Logic Diagram** 



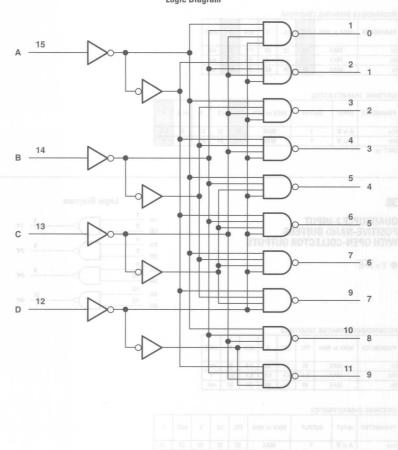
RECOMMENDED OPERATING CONDITIONS

		1	10.10	-	_		-
PARAMETER	MAX or MIN	TTL	LS	S	ALS	F	UNIT
Icc	MAX	54	12	80	7.8	30	mA
Von	MAX	5.5	5.5	5.5	5.5	4.5	V
lou	MAX	48	24	60	24	64	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	F
tPLH	A or B	Υ	MAX	22	32	10	33	13
tPHL .	A or B	Y	MAX	18	28	10	12	5.5

- All Outputs Are High for Invalid Input Conditions
- Also for Applications as
   3-Line to 8-Line Decoders
  - 4-Line to 16-Line Decoders
- Full Decoding of Valid Input Logic Ensures That All Inputs Remain Off for All Invalid Input Conditions



# **FUNCTION TABLE**

		INP	UTS						OUT	PUTS				
No.	D	С	В	Α	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н
1	L	L	L	Н	Н	L	H	H	Н	H	H	H	H	H
2	L	L	H	L	Н	H	L.	H	H	Н	H	H	H	Н
3	L	L	H	H	Н	H	H	L	H	Н	H	H	H	Н
4	L	Н	L	L	Н	H	Н	Н	L	Н	Н	H	H	Н
5	L	Н	L	Н	н	Н	Н	Н	Н	L	H	H	H	Н
6	L	Н	H	L	н	H	H	Н	Н	Н	L	Н	H	Н
7	L	H	H	H	Н	H	H	H	H	H	H	L	H	Н
8	H	L	L	L	H	H	Н	H	H	H	H	H	L	H
9	Н	L	L	Н	Н	H	H	H	Н	Н	H	Н	H	L
	Н	L	Н	L	Н	Н	Н	Н	Н	Н	H	Н	Н	Н
0	H	L	H	H	H	H	H	H	H	H	H	H	H	Н
7	H	H	L	L	Н	H	H	H	H	H	H	H	H	Н
INVALID	H	H	L	Н	H	H	H	H	H	H	H	H	H	Н
=	H	H	H	L	H	H	H	H	Н	H	H	Н	H	Н
	H	Н	H	Н	H	H	Н	H	H	H	H	H	H	H

RECOMMENDED OPERATING CONDITIONS

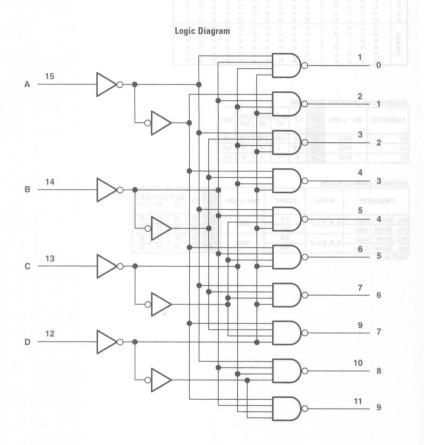
PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
Icc	MAX	56	13	0.08	0.16	0.16	mA
Іон	MAX	-0.8	-0.4	-4	-4	-4	mA
lou	MAX	16	8	4	4	4	mA

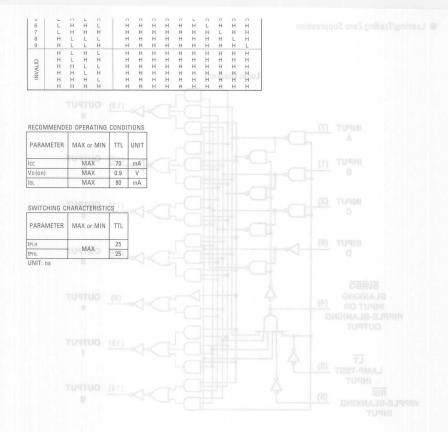
SWITCHING CHARACTERISTICS

SVVITCHING CHARAC	TEMOTICS				_			
PARAMETER	INTPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
tPLH 2Level - Logic	A, B, C or D	0-9	MAX	25	25	38	45	53
tPHL 2Level - Logic	A, B, C or D	0-9	IVIAX	25	25	38	45	53
tPLH 3Level · Logic	A. B. C or D	0-9	MAX	30	30	38	45	53
tPHL 3Level · Logic	A, B, C OI D	0-9	IVIAA	30	30	38	45	53

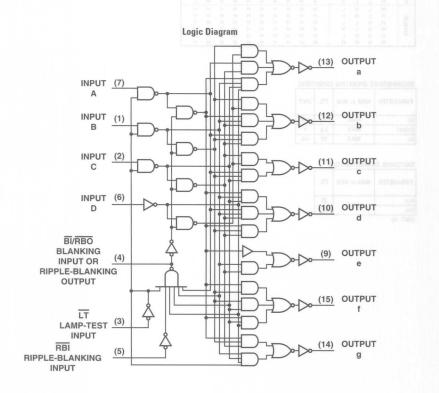
# **BCD-TO-DECIMAL DECODER/DRIVER**

- 80-mA Sink-Current Capability
- All Outputs Are Off for Invalid BCD Input Conditions





- Open-Collector Outputs
- Lamp-Test Provision
- Leading/Trailing Zero Suppression



# FUNCTION TABLE

		H	NPU'	rs			DUDDO			0	UTPUT	rs		
No.	LT	RBI	D	C	В	Α	BI/RBO	a	b	C	d	е	f	g
0	Н	Н	L	L	L	L	Н	ON	ON	ON	ON	ON	ON	OFF
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON
3	H	X	L	L	Н	H	H	ON	ON	ON	ON	OFF	OFF	ON
4	н	X	L	Н	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON
5	H	X	L	Н	L	H	H	ON	OFF	ON	ON	OFF	ON	ON
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON
7	Н	X	L	Н	Н	Н	H	ON	ON	ON	OFF	OFF	OFF	OFF
8	H	X	Н	L	L	L	H	ON	ON	ON	ON	ON	ON	ON
9	H	X	Н	L	L	Н	H	ON	ON	ON	OFF	OFF	ON	ON
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON
11	H	X	Н	L	Н	H	H	OFF	OFF	ON	ON	OFF	OFF	ON
12	Н	X	Н	Н	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON
13	H	X	Н	Н	L	Н	H	ON	OFF	OFF	ON	OFF	ON	ON
14	H	X	Н	Н	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON
15	Н	X	Н	Н	Н	Н	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF
RBI	Н	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON

# WD-OR INVEST GATES

# RECOMMENDED OPERATING CONDITIONS

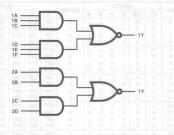
PARAMETER	MAX or MIN	TTL	LS	UNIT
Icc	MAX	103	13	mA
Іон	MAX	-0.2	-0.05	mA
lou	MAX	8	3.2	mA

## SWITCHING CHARACTERISTICS

SWITCHING C	HANALIER	1131163			_
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
toff	A	A to g	MAX	100	100
ton	A	A to g	MAX	100	100
toff	RBI	A to g	MAX	100	100
ton	RBI	A to g	MAX	100	100

# **AND-OR INVERT GATES**

- '51, 'S51: Y = AB + CD
- 'F51, 'LS51: 1Y = (1A•1B•1C) + (1D•1E•1F) 'HC51: 2Y = (2A•2B) + (2C•2D)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	F	SN74 HC	UNIT
Icc	MAX	14	2.8	22	7.5	0.08	mA
Іон	MAX	-0.4	-0.4	-1	-1	-4	mA
lou	MAX	16	8	20	20	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	F	SN74 HC
tPLH .	Any	Y	MAX	22	20	5.5	6.5	35
tPHL.	Any	Υ	MAX	15	20	5.5	4.5	35



# 4-2-3-2 INPUT AND-OR INVERT GATE

•  $Y = \overline{ABCD + EF + GHI + JK}$ 

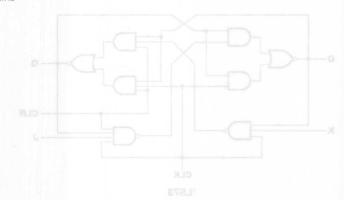


RECOMMENDED OPERATING CONDITIONS

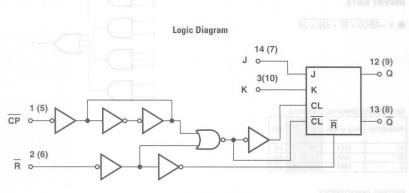
PARAMETER	MAX or MIN	S	F	UNIT
lcc	MAX	16	4.7	mA
Іон	MAX	-1	-1	mA
lou	MAX	20	20	mA

SWITCHING CHARACTERISTICS

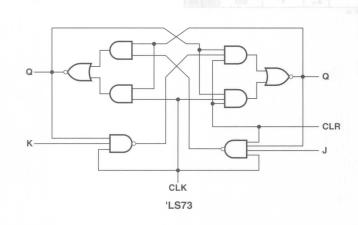
PARAMETER	INPUT	OUTPUT	MAX or MIN	S	F
tplH	Any	Υ	MAX	5.5	7
tphl.	Any	Υ	MAX	5.5	5.5



# **DUAL J-K FLIP-FLOPS WITH CLEAR**



CD74HC/HCT73



# **FUNCTION TABLE (SN74)**

	INPUTS			OUTPUTS
CLEAR	CLOCK	J	K	Q Q
L	X	X	X	L H
H	1	L	L	Q0 Q0
H	1	H	L	H L
H	1	L	H	L H
Н	1	H	H	TOGGLE
10	13	v	~	0- 0-

# TRUTH TABLE (CD74)

	INP		OUT	PUTS	
R	CP	CP J		Q	ā
L	Х	X	X	L	Н
Н	1	L	L	No C	nange
Н	1	Н	L	Н	L
Н	3 Nes	to Lb/	Hio	A-600	Н
Н	hekan	HA	Hol/	Toggle	
Н	Н	X	Х	No C	nange

• 74ACT11xxx: Product Available

NOTE:
H = High Level (Steady State)
L = Low Level (Steady State)
X = Irrelevant
↓ = High-to-Low Transition

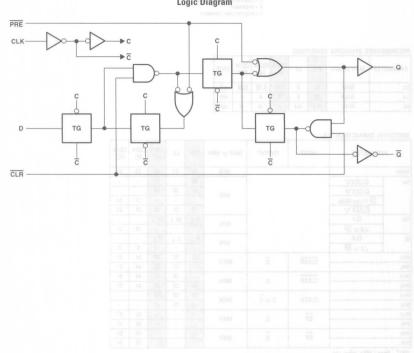
# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
Icc	MAX	20	6	0.04	0.08	0.08	mA
Іон	MAX	16	8	4	4	4	mA
lou	MAX	-0.4	-0.4	-4	-4	-4	mA

# SWITCHING CHARACTERISTICS

	PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
fmax				MIN	15	30	25	20	20
tw	CLOCK"L"				20	-	20	-	-
	CLOCK"H"			MIN	47	20	20	-	-
	CP Pulse Wide			IVIIIV				24	24
	CLEAR "L"				25	20	20	24	27
tsu	CLK			MIN	0 ↑	20 ↓	25 ↓	-	-
	J,K to CP			IVIIIV			-	24	24
th	CLK			MIN	0 1	0 1	01		
	J,K to CP			IVIIIV		-		3	3
tPLH		CLEAR	ā	MAX	25	20	39	44	51
tPHL .		CLEAR	u	IVIAX		20	39	44	51
tPLH		CLEAR	Q	MAX		20	39	44	51
tPHL .		CLEAR	u	IVIAX	40	20	39	44	51
tPLH .		CLOCK	0	MAN	25	20	32		-
<b>TPHL</b>		CLOCK	Q or Q	MAX	40	20	32		-
tPLH		CP	Q	MAN	-	-	-	48	57
tPHL		LP	u u	MAX	-	-		48	57
tPLH		CP	<u>-</u>	1111	-	-	-	48	54
<b>TPHL</b>		UP	u	MAX		-	-	48	54

UNIT fmax : MHz, other : ns



# **FUNCTION TABLE**

	INP	UTS		OUT	PUTS
PRESET	CLEAR	CLOCK	D	Q	Q
L	Н	×	X	Н	L
H	L	X	×	L	Н
L	L	X	X	H*	H*
Н	Н	1	H	H	L
Н	Н	1	L	L	Н
Н	Н	L	X	Qn	Qn

<sup>†</sup> This configuration is unstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

# RECOMMENDED OPERATING CONDITIONS

NECOMMENDE	DUILIMINU	CONDI	TONS	-				_			1 10		_			
PARAMETER	MAX or MIN	ΠL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	UNIT
Icc	MAX	15	8	25	4	16	16	0.04	0.08	0.04	0.08	0.04	0.02	0.08	0.04	mA
Гон	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	-24	-24	mA
lou	MAX	16	8	20	8	20	20	4	4	4	4	24	24	24	24	mA

PARAMETER	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	TA 3A	LV 5V	LVC 3V	UNIT
lcc	MAX	0.02	0.08	0.02	0.02	-	0.02	0.01	mA
Іон	MAX	-24	-24	-8	-8	-6	-12	-24	mA
lor.	MAX	24	24	8	- 8	6	12	24	mA

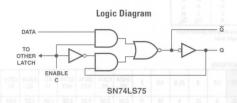
# SWITCHING CHARACTERISTICS

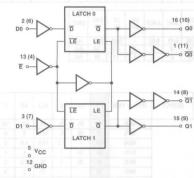
	PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11
fmax		_	(II) 24 (II) 0	MIN	15	25	75	34	105	100	25	20	24	16	125
tw	CLOCK"H"			MIN	30	25	6	14.5	4	4	20	24	23	27	4
	CLOCK"L"	7		MIN	37	-	7.3	14.5	5.5	5	20	24	23	27	4
	RESET or CLEAR "L"			MIN	30	25	7	15	4	4	25	24	20	24	4
tsu	D			MIN	20	20	3	15	4.5	3	25	18	15	18	3.5
	PRE, CLR INACTIVE			MIN	20	-	-	10	2	2	6		0	5	1
th				MIN	5	5	2	0	0	1	0	3	0	3	0
tPLH		RESET	Q	MAX	25	25	6	13	7.5	7.1	58	60	44	60	7.1
tPHL		HESEI	ā	IVIAX	40	40	13.5	15	10.5	10.5	58	60	44	60	9
tPLH		OLEAD	ā	MAX	25	25	6	13	7.5	7.1	58	60	44	60	7.1
<b>TPHL</b>		CLEAR	Q	IVIAX	40	40	13.5	15	10.5	10.5	58	60	44	60	9
tPLH		CLOCK	0 0	MAX	25	25	9	16	8	7.8	44	53	35	53	8.2
tPHL		CLOCK	Q or Q	IVIAX	40	40	9	18	9	9.2	44	53	35	53	7.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	TAC TAC
		Am a	MIN	125	110	85	125	85	75	65	45	75	100
CLOCK"H"			MIN	5	4.5	5	6	5.7	5	5	7	5	3.3
CLOCK"L"			MIN	5	4.5	5	6	5.7	5	5	7	5	3.3
RESET or CLEAR "L"			MIN	5	4	5	6	5	5	5	7	5	3.3
D			MIN	3	3.5	4.5	3.5	4	5	5	7	5	3
PRE, CLR INACTIVE	3H 3H		MIN	0	-	2	0	-	3	3.5	5	3	2
	100		MIN	0.5	0	0	1	9.5	0.5	0	0.5	0.5	0
	DECET	0	MAN	10	10.5	9.6	11.5	11.5	11	13	18	11	5.4
	NESEI		IVIAA	10.5	11.5	12.5	12.5	12.5	11	13	18	11	5.4
	CLEAD	ā	MAN	10	10.5	9.6	11.5	11.5	11	13	18	11	5.4
	CLEAN	0	IVIAX	10.5	11.5	12.5	12.5	12.5	11	13	18	11	5.4
	CLOCK	0 0	MAN	10.5	10	9.4	14	9.5	10.5	10	17.5	10.5	5.2
	CLUCK	uoru	WAX	10.5	10	8.8	12	9.5	10.5	10	17.5	10.5	5.2
	CLOCK"H" CLOCK"L"  RESET or CLEAR "L" D	CLOCK"H" CLOCK"L" RESET or CLEAR "L"	CLOCK'H' CLOCK'L' RESET or CLEAR 'L' D PRE, CLR INACTIVE  RESET 0 CLEAR 0 0	CLOCK'H' CLOCK'L' MIN  RESET OF CLEAR 'L' D MIN MIN MIN MIN MIN MIN MIN MIN MIN MIN	NAC   NAC	MIN   125   110	MAX of MIN	NAC   NAC	MIN   125   110   85   125   85	MIN   125   110   85   125   85   75	MIN   125   110   85   125   85   75   65	MIN   125   110   85   125   85   75   65   45	MAX of MIN   AC   AC   11   ACT

UNIT fmax : MHz, other : ns

# **4-BIT BISTABLE LATCHES**





CD74HC/HCT75

# **FUNCTION TABLE**

INP	UTS	OUT	PUTS
D	C	Q	Q
L	Н	L	Н
Н	H	H	L
X	L	Qo	Qo

# RECOMMENDED OPERATING CONDITIONS

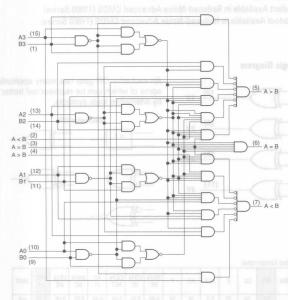
PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
Icc	MAX	53	12	0.04	0.08	0.08	mA
Іон	MAX	-0.4	-0.4	-4	-4	-4	mA
lor and an analysis	MAX	16	8	4	4	4	mA

# SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT								
tw			MIN	20	20	20	24	24								
tsu		2.01	IVIIN	20	20	25	18	18								
th		8.11	MIN	5	5	5	3	3								
tPLH		0	MAX	30	27	30	33	42								
tphL .	D	0	MAX	25	17	30	33	42								
tPLH		-	MANY MAI	40	20	30	39	42								
tphl.	D	0	MAX	15	15	30	39	42								
tPLH		0		MAN	MAY	MAN	MANY	MAN	MAX	MAN	MAN 3	30	27	33	39	42
tPHL .	- G C	и	WAX	15	25	33	39	42								
tPLH	- G Q		MAX	30	30	33	39	45								
tPHL .	U	u.	IVIAX	15	15	33	39	45								

# **4-BIT MAGNITUDE COMPARATORS**

# **Logic Diagram**



# FUNCTION TABLE

1. 1. 2		ARING UTS			SCAD		0	UTPU	rs
A3, B3	A2, B2	A1, B1	A0, B0	A>B	A <b< th=""><th>A=B</th><th>A&gt;B</th><th>A<b< th=""><th>A=B</th></b<></th></b<>	A=B	A>B	A <b< th=""><th>A=B</th></b<>	A=B
A3>B3	X	X	X	X	X	X	Н	L	- La
A3 <b3< td=""><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>L</td><td>Н</td><td>L</td></b3<>	X	X	X	X	X	X	L	Н	L
A3=B3	A2>B2	X	X	X	X	X	Н	L	L
A3=B3	A2 <b2< td=""><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>L</td><td>H</td><td>L</td></b2<>	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1 <b1< td=""><td>X</td><td>X</td><td>X</td><td>X</td><td>L</td><td>Н</td><td>L</td></b1<>	X	X	X	X	L	Н	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0 <b0< td=""><td>X</td><td>X</td><td>X</td><td>L</td><td>H</td><td>L</td></b0<>	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	Н	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	Н	H	L	L	L	L
A3=B3	A2≃B2	A1=B1	A0=B0	L	L	L	H	H	TUE
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H

# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	SN74 HC	CD74 HC	CD74 HCT	UNIT
Icc	MAX	88	20	115	0.08	0.16	0.16	mA
Іон	MAX	-0.4	-0.4	-1	-4	-4	-4	mA
lou	MAX	16	8	20	4	4	4	mA

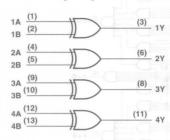
# SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	Nunber of Gate Levels	MAX or MIN	TTL	LS	S	SN74 HC	CD74 HC	CD74 HCT
to. u	Any A or B	A < B, A > B	3	MAX	26	36	16	58	59	56
tPLH .	data input	A =B	4	MAX	35	45	18	50	53	60
******	Anv A or B	A < B, A > B	3	MAX	30	30	16.5	58	59	56
tphl.	data input	A =B	4	MAX	30	45	16.5	50	53	60
tPLH	A < B, A = B	A>B	1	MAX	11	22	7.5	44	42	45
tphl .	A < B, A = B	A>B	1	MAX	17	17	8.5	44	42	45
tPLH	A =B	A =B	2	MAX	20	20	10.5	37		
tPHL	A =B	A =B	2	IVIAX	17	26	7.5	37		
tPLH	A >B, A =B	A < B	1	MAX	11	22	7.5	44	42	47
tPHL .	A >B, A =B	A < B	1	IVIAX	17	17	8.5	44	42	47

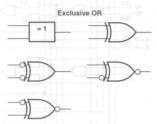
# QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

- $Y = A \oplus B \text{ or } Y = \overline{A}B + \overline{A}B$
- 74AC11xxx : Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

# Logic Diagram



An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



# RECOMMENDED OPERATING CONDITIONS

	D OPERATING						F	SN74	CD74	CD74	AC	SN74	CD74	ACT	
PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	1	HC	HC	HCT	11	AC	AC	11	UNIT
lcc	MAX	50	10	75	5.9	38	28	0.02	0.04	0.04	0.04	0.02	0.08	0.04	mA
Іон	MAX	16	8	20	8	20	20	4	4	4	24	24	24	24	mA
lor	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-24	-24	-24	-24	mA

PARAMETER	MAX or MIN	SN74 ACT	CD74 ACT	АНС	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
Icc	MAX	0.04	0.08	0.02	0.02	- 1	0.02	0.01	mA
Іон	MAX	24	24	8	8	6	12	24	mA
lou	MAX	-24	-24	-8	-8	-6	-12	-24	mA

# SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11
tplh	A or B	Υ	MAX	23	23	10.5	17	7.5	6.5	25	36	48	7.6	9	10.8	9.6
tPHL .	AOFB	Υ	MAX	17	17	10	12	6.5	6.5	25	36	48	6.8	9.5	10.8	9
tPLH	4 0	Υ	MAX	30	30	10.5	17	6.5	8	25	36	48	7.6	9	10.8	9.6
tPHL .	A or B	Y	MAX	22	22	10	10	7	7.5	25	36	48	6.8	9.5	10.8	9

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	TAC 3A
tPLH Input Low	A D	Y	MAX	10	14.6	10	10	16.5	10	4.6
tPHL Input Low	AorB	Y	MAX	10.5	14.6	10	10	16.5	10	4.6
tРLH Input High	A D	Υ	MAX	10	14.6	10	10	16.5	10	4.6
tPHL Input High	A or B	Υ	MAX	10.5	14.6	10	10	16.5	10	4.6

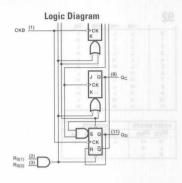




	OUTPUTS							
Count	QA	QD	QC	QB				
0	L	L	L	L				
1	L	L	L	Н				
2	L	L	H	L				
2	L	L	H	H				
4	L	Н	L	L				
5	H	L	L	L				
6	H	L	L	Н				
7	H	L	H	L				
8	H	L	H	H				
9	H	Н	L	L				

# RESET/COUNT FUNCTION TABLE

1	RESET	INPUTS	3		OUT	PUTS	
R0(1)	R0(2)	R9(1)	R9(2)	QD	QC	QB	QA
H	Н	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	Н
X	L	X	L		Co	unt	
L	X	L	X		Co	unt	
L	X	X	L		Co	unt	
X	L	L	X		Co	unt	



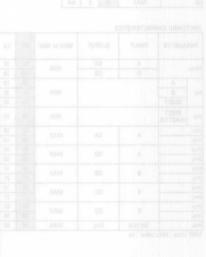
RECOMMENDED OPERATING CONDITI	NN

PARAMETER	MAX or MIN	TTL	LS	UNIT
Icc	MAX	39	15	mA
Іон	MAX	-0.8	-0.4	mA
loc	MAX	16	8	mA

SWITCHING CHARACTERISTICS

SWI	TCHING CHA	RACTERISTIC	S			
PA	RAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
		А	QA	MIN	32	32
fmax	,	В	QB	IVIIIV	16	16
	A				15	15
tvv	В			MIN	30	30
RESET					15	30
tsu	RESET INACTIVE			MIN	25	25
tPLH		А	QA	MAX	16	16
tPHL		A	UA	IVIAX	18	18
tPLH		А	QD	MAX	48	48
tPHL		-	ub.	IVIAA	50	50
tPLH		В	QB	MAX	16	16
tPHL		D	db.	IVIAA	21	21
tPLH		В	QC	MAX	32	32
tPHL		D	46	IVIAA	35	35
tPLH		В	QC	MAX	32	32
tPHL.		U	ut.	IVIAA	35	35
tPHL .		Set to 0	Any	MAX	40	40
tPLH		Set to 9		MAX	30	30
tPHL.		361 (0 3	QB, QC	IVIAA	40	40





# **DIVIDE-BY-12 COUNTERS**

COUNT				
COUNT	QD	QC	QB	QA
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	Н	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	Н	Н
10	H	Н	L	L
11	H	H	L	Н

RESET	INPUTS	OUTPUTS					
R0(1)	R0(2)	QD	QC	QB	QA		
Н	Н	L	L	o L	L		
L	×		CO	JNT			
X	L		CO	UNT			

# RECOMMENDED OPERATING CONDITIONS

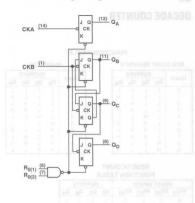
RECOMMENDE	D OPERATING	CONDI	TIONS	_
PARAMETER	MAX or MIN	TTL	LS	UNIT
Icc	MAX	39	15	mA
Іон	MAX	-0.8	-0.4	mA
lou	MAX	16	8	mA

# SWITCHING CHARACTERISTICS

PAI	RAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
fmax		A QA MIN		NAIN	32	32
ımax	,	В	QB	IVIIN	16	16
	A				15	15
tw	В			MIN	30	30
	RESET				15	30
tsu RESET INACTIVE				MIN	25	25
tPLH tPHL			0.4	MAX	16	16
		Α	QΑ	IVIAA	18	18
tPLH		Α	QD	MAX	48	48
tPHL		А	ub.	IVIAX	50	50
tPLH		В	QB	MAX	16	16
tPHL.		В	цв	WAX	21	21
tPLH		В	QC	MANY	16	16
tPHL .		В	uc	MAX	21	21
tPLH tPHL tPHL		В	QD	MAX	32	32
		D	dD.	IWAX	35	35
		Set to 0	Any	MAX	40	40

UNIT fmax : MHz, other : ns

# Logic Diagram



# **4-BIT BINARY COUNTERS**

**FUNCTION TABLE** 

COUNT		OUT	PUTS	
COUNT	QD	QC	QB	QA
0	L	L	L	L
1	L	L	L	Н
2	L	L	H	L
3	L	L	H	H
4	L	Н	L	L
5	L	Н	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	Н	L
11	H	L	H	H
12	H	Н	L	L
13	H	H	L	H
14	H	H	Н	L
15	H	H	H	H

RESET	INPUTS	OUTPUTS						
R0(1)	R0(2)	QD	QC	QB	QA			
Н	Н	L	L	L	L			
L	X	COUNT						
X	L	COUNT						

CKB (1)[8] J Q (9)[9] Q CK K W (1)[12] Q CK K W (1)[12] Q CK K K W (1)[12] Q CK K K W (1)[12] Q CK K K K W (1)[12] Q CK K K K W (1)[12] Q CK K K K K W (1)[12] Q CK K K K K W (1)[12] Q CK K K K W (1)[12] Q CK K K K W (1)[12] Q CK K K K W (1)[12] Q CK K K K W (1)[12] Q CK K K K W (1)[12] Q CK K K K W (1)[12] Q CK K K K W (1)[12] Q CK K K K W (1)[12] Q CK K K K W (1)[12] Q CK K K K W (1)[12] Q CK K K K W (1)[12] Q CK K K W (1)[12] Q CK K K W (1)[12] Q CK K K W (1)[12] Q CK K K W (1)[12] Q CK K K W (1)[12] Q CK K K W (1)[12] Q CK K K W (1)[12] Q CK K K W (1)[12] Q CK K K W (1)[12] Q CK K K W (1)[12] Q CK K K W (1)[12] Q CK K K W (1)[12] Q CK W (1)[12] Q CK

CKA (14)[14]

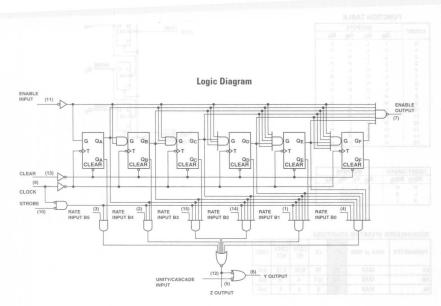
RECOMMENDED OPERATING CONDITIONS

HEOOMMETADE	D OI LINTING	001401	110110	_	_	
PARAMETER	MAX or MIN	TTL	LS	CD74 HC	CD74 HCT	UNIT
Icc	MAX	39	15	0.16	0.16	mA
Іон	MAX	-0.8	-0.4	-4	-4	mA
lou	MAX	16	8	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	CD74 HC	CD74 HCT
		А	QA	MIN	32	32	20	20
fmax	,	В	QB	IVIIIV	16	16	20	20
	A				15	15	24	24
tw	В			MIN	30	30	24	24
RESET					15	30	24	24
tsu	RESET			MIN	25	25	-	-
tPLH					16	16	38	51
tPHL .		А	QΑ	MAX	18	18	38	51
tPLH .			0.0	MAN	70	70	-	87
tPHL		А	QD	MAX	70	70		87
tPLH			0.0	MAN	16	16	41	51
tPHL		В	QΒ	MAX	21	21	41	51
tPLH		В	QC	MAY	32	32	56	69
tPHL tPLH		В	uc	MAX		35	56	69
				MAN	51	51	74	87
tPHL		В	QD	MAX	51	51	74	87
tPHL.		Set to 0	ANY	MAX	40	40	-	-

UNIT fmax : MHz, other : ns



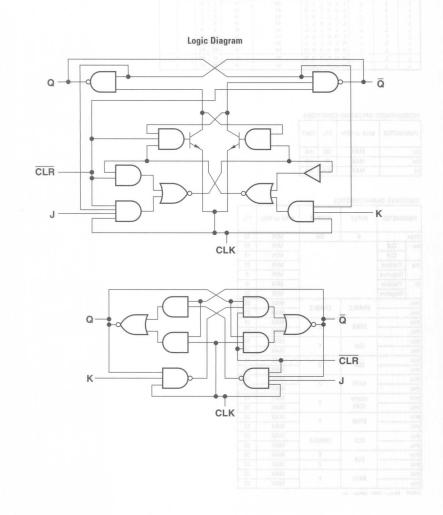
-	-	-	17	-	-	7	Н	H	64	10	2	2	
-	-	-	17	-	-	Н		-	64 64	H	4	4	4
-	-	7	1.	-	Н	7	-	-		Н	8	8	- 1
_	-	-	L	H	п	L	L	1	64		16	16	1
1	1	-	H		ī	i	1		64	H	32	32	ul i
L	L	L		H	Н	Н	Н	Н	64	H	63	63	1
L	L	L	Н	Н	Н	Н	Н	Н	64	L	Н	63	1
L	L	L	H	L	Н	L	L	L	64	Н	40	40	1

# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
Icc	MAX	120	mA
Іон	MAX	16	mA
lou	MAX	-0.4	mA

SWI	TCHING CHA	ARACTERISTI	CS	- 17_	_
PAI	RAMETER	INPUT	OUTPUT	MAX or MIN	TTL
fmax		A	Q.A	MIN	25
tw	CLK			MIN	20
	CLR			MIN	15
tsu	Positive			MIN	25
	Negative			MIN	0
th	Positive			MIN	0
	Negative			MIN	20
tPLH		ELLA DI E	ELLEDIE.	MAX	20
tPHL.		ENABLE	ENABLE	MAX	21
tPLH		AWRE	7-0	MAX	18
tPHL.		STRB	Z	MAX	23
tPLH		0.11	Y	MAX	39
tPHL .		CLK	CLK T		30
tPHL tPHL tPHL		OLK	2	MAX	18
		CLK	Z	MAX	26
tPLH		DATE		MAX	10
tPHL		HATE	RATE Z		14
tPLH		UNITY	γ	MAX	14
tPHL		/CAS	,	MAX	10
tPLH		STRB	Y	MAX	30
tPHL		SINB	T.	MAX	33
tPLH		CLK	ENABLE	MAX	30
tPHL		ULK	ENABLE	MAX	33
<b>t</b> PLH		CLR	Υ	MAX	36
tPHL		CLH	Z	MAX	23
tPLH		DATE	v	MAX	23
tPHL		KAIL	RATE Y		23

IINIT fmax · MHz other · ns



	INPUTS		183	OUTPUTS	ų
CLEAR	CLOCK	J	K	QQ	
L	X	X	X	L H	П
H		L	L	Q0 Q0	
H		H	L	H L	
H	JL	L	H	L H	
HE		H	н	TOGGLE	

### 'LS107A,'HC107

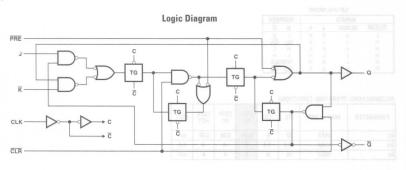
	INPUTS			OUTPUTS
CLEAR	CLOCK	J	K	Q Q
L	X	X	X	L H
H	1	L	L	Q0 Q0
H	1	H	L	H L
H	1	L	H	L H
H	1	H	H	TOGGLE
H	H	X	X	Qn Qn

# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
lcc	MAX	20	6	0.04	0.08	0.08	mA
Іон О	MAX	-0.4	-0.4	-4	-4	-4	mA
lou	MAX	16	8	4	4	4	mA

SWIII	CHING CHARACTER	RISTICS			,				
F	PARAMETER	INPUT	OUTPUT	MAX or MIN	ΠL	LS	SN74 HC	CD74 HC	CD74 HC
fmax				MIN	15	30	25	20	19
tw	CLK H			MIN	20	20	20		-
	CLK L			MIN	47	-	20	-	
	CP			MIN	-	-	100	24	27
	CLR L (or R)			MIN	25	25	20	25	36
tsu	J, K			MIN	0	20	25	30	30
	CLR INACTIVE			MIN	0	25	25	-	-
th				MIN	0	0	0	3	5
tPLH		CLR (or R)	ā	MAX	25	20	39	47	57
<b>TPHL</b>		CLN (OF N)	Q	MAX	40	20	39	47	57
tPLH		CLK	ā	MAX	25	20	32		-
tPHL		ULK	Q	MAX	40	20	32		-
tPLH		CP	Q	MAX	-	-	-	51	65
<b>TPHL</b>		CF	u	MAX	-			51	65
tPLH		CP	ā	MAX		-		51	60
<b>TPHL</b>		CF	u	MAX	-	-		51	60

UNIT fmax : MHz, other : ns



n n L A A Q0 Q0

† The output levels in this configuration are not guaranteed to meet the minimum levels for V<sub>OH</sub>. Furthermore, this configuration is nonstable; that is, it will not persist when either PRE or CLR returns to its inactive (high) level.

### RECOMMENDED OPERATING CONDITIONS

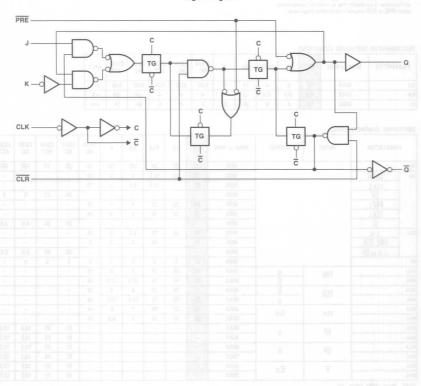
PARAMETER	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
Icc	MAX	15	8	4	17	17	0.04	0.08	0.08	0.08	0.08	mA
Іон	MAX	-0.8	-0.4	-0.4	-2	1	-4	-4	-4	-24	-24	mA
lou	MAX	16	4	8	20	20	4	4	4	24	24	mA

### SWITCHING CHARACTERISTICS

SWITE	CHING CHARACTE	RISTICS						197. 19	1					
F	PARAMETER	INPUT	ОИТРИТ	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
fmax			- 5	MIN	25	25	34	105	90	25	25	19	100	100
tw	CLK H			MIN	20	25	14.5	4	4	20		-	275	-
	CLK L			MIN	20	-	14.5	5.5	5	20	-	-		-
	CP			MIN			-	-		-	24	27	5	5
	PRE L			MIN	20	25	15	4	4	25	-	-	-	-
	CLR L			MIN	20	25	15	4	4	25	-	-	-	
	R			MIN			-	-		12.1	24	36	4.5	5.5
tsu	J, K			MIN	10	25	15	5.5	3	25	-	-	-	-
	PRE, CLR			MIN	10	-	10	2	2	6	-	-		-
	J, K to CP			MIN	-	-	-			-	30	30	5.5	5.5
th				MIN	6	5	0	0	1	0	3	5	0	1
tPLH		PRE	0	MAX	15	25	13	8	8	58	2	-	-	-
tPHL		PRE	ā	MAX	35	40	15	10.5	10.5	58	-	-	-	-
tPLH		CLR	ā	MAX	15	25	13	8	8	58	-	-	-	-
tPHL.		LLH	Q	MAX	25	40	15	10.5	10.5	58	-	-	-	-
tPLH		CLK	ā,a	MAX	16	25	16	9	8	44	-	-	1.0	19
tPHL.		LLK	u,u	MAX	28	40	18	9	9.2	44	-	-		
tPLH		CP	Q	MAX		-	-	-	-	-	51	65	10.3	10.3
tPHL.		LP	u	MAX	-	-	-		-	-	51	65	10.3	10.3
tPLH		CP	ā	MAX	- 1		140	-		-	51	60	10.3	10.3
tPHL		CP	u	MAX		-	1-0	-	-	-	51	60	10.3	10.3
tPLH		R	<u>ā</u> ,a	MAX		-	-	-	-		47	57	12.2	12.2
tPHL	A A	н	u,u	MAX	-	-	-	-	-	-	47	57	12.2	12.2

UNIT fmax : MHz, other : ns

# Logic Diagram



FUNCTION TABLE

	INF	PUTS			OUTPUTS
CLEAR	A1	A2	В	B2	QQ
L	X	X	X	X	L H
X	H	H	X	X	L† H†
X	X	X	L	X	L† H†
X	X	X	X	· L	L† H†
Н	L	X	1	H	JL JL
Н	L	X	Н	1	JL J
Н	X	L	1	H	TLT
Н	X	L	H	1	
Н	Н	1	H	H	
H	1	1	H	H	11.11
Н	1	Н	H	H	122
1	L	X	H	H	TLT
Ť	X	L	Н	H	52.75

See explanation of function table on page

† These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	LVC 3V	UNIT
lcc	MAX	6	25	4.5	19	0.04	0.08	0.08	0.08	0.08	0.01	mA
Іон	MAX	-0.4	-1	-0.4	-1	-4	-4	-4	-24	-24	-24	mA
lou	MAX	8	20	8	20	4	4	4	24	24	24	mA

	PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	F	SN74 HC	CD74 HC	CD74 HCT	3V
fmax				MIN	30	80	30	100	20	20	20	150
tw	PRE, CLR			MIN	25	8	10	5	25	24	27	
	CLK H			MIN	20	6	16.5	5	25		444	3.3
	CLK L			MIN		6.5	16.5	5	25			3.3
	CP			MIN	-	-	-	-	-	24	24	-
tsu	DATA			MIN	20	7	22	5	25	24	24	2.3
	PRE INACTIVE			MIN	25		20	5	25			2.4
	CLR INACTIVE			MIN	20	May X	20	5	25	- 1	PIPE	2.4
th				MIN	0	0	0	0	0	0	3	0.7
tPLH		PRE or CLR	Q or $\overline{\mathbb{Q}}$	MAX	20	7	15	7.5	41	-	-	4.8
tPHL		FRE OF CEN	u or u	MAX	20	7	18	7.5	41		A -	4.8
tPLH		CLK	Q or Q	MAX	20	7	15	7.5	31	-	8 -	5.9
tphl.		CLK	u or u	MAX	20	7	19	7.5	31		A -	5.9
tPLH.		CP CP	Q or Q	MAX	1		-	-		53	53	-
tPHL		LP	uoru	MAX	-			-	-	53	53	-
tPLH		- S	0 - 0	MAX		-	-	12	-	47	48	
tPHL		0	Q or Q	MAX	1.00	-			-	47	48	-
tPLH		R	0 0	MAX	-	-	-	-	-	54	56	-
tPHL.		н	Q or Q	MAX			-	-	-	54	56	-

UNIT fmax : MHz, other : ns

	INPUTS		OUTP	UTS
A1	A2	В	Q	Q
L	X	H	L	Н
X	L	H	L†	H†
X	X	L	L†	H†
H	H	X	L†	H†
H	1	H	JT.	L
1	H	H	TT.	T
1	1	H	LT.	T
L	X	1	J.	T
X	L	1		ш

Logic Diagram

A1 (3)
A2 (4)
B (5)

(10)
Cext

NOTES: 1. An external capacitor may be connected between C<sub>Ext</sub> (positive) and R<sub>Ext</sub>/C<sub>Ext</sub>.

2. To use the internal timing resistor, connect R<sub>int</sub> to V<sub>CC</sub>. For improved pulse width accuracy and repestability, connect an external resistor between R<sub>Ext</sub>/C<sub>Ext</sub> and V<sub>CC</sub> with R<sub>int</sub> open-circuited.

See explanation of function table on page

† These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
lcc	MAX	40	mA
Іон	MAX	-0.4	mA
lou	MAX	16	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
tw (IN)	0 0	0 0	MIN	50
tPLH 8	A	14 0 EX	BI MAY	70
tPHL PA	В	18 45	MAX	80
tPLH .	Α	E -	MAY	55
tPHL -	В	u	MAX	65

### Rint is nominally 10 kW for '122 and 'LS122

**FUNCTION TABLE** 

INPUTS					OUTPUTS
CLEAR	A1	A2	В	B2	QQ
L	X	X	X	X	L H
×	H	H	X	X	L† H†
X	X	X	L	X	L† H†
X	X	X	X	L	L† H†
H	L	X	1	H	111
Н	L	X	н	1	1 11 11
H	X	L	1	H	JLT
H	X	L	H	1	
H	H	1	H	H	1111
H	1	1	Н	H	TIT
H	1	Н	Н	H	JL 7L
1	L	×	H	H	JLJ
1	X	L	H	H	

See explanation of function table on page

# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
Icc	MAX	66	11	mA
Гон	MAX	-0.8	-0.4	mA
lou	MAX	16	8	mA

### SWITCHING CHARACTERISTICS

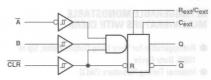
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
tw	61 55	91 61	MIN	40	40
	A		MAN	33	33
tplH -	В	1 0	MAX	28	44
1000	A	ā	4444	40	45
tphl.	В	u u	MAX	36	56
tPLH	OLEAD	Q	1447	27	27
tphl.	CLEAR	ō	MAX	40	45

<sup>†</sup> These lines of the functional tables assume that the indicated

steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

# DUAL RETRIGGERABLE MONOSTABLE MULTIVIBARATORS WITH CLEAR

 Retriggerable for Very Long Output Pulse, Up to 100% Duty Cycle



### **FUNCTION TABLE**

INPUTS			OUTPUTS
CLEAR	Ā (A)	В	Q Q
L	X	X	L H
X	H	×	L† H†
X	X	L	L† H†
H	L	1	127
H	1	Н	
1	L	H	11.11

See explanation of function table on page † These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

RECOMMENDED OPERATING CONDITIONS

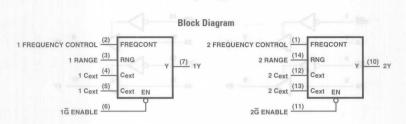
PARAMETER	MAX or MIN	TTL	LS	CD74 HC	CD74 HCT	AHC	AHCT	LV 3V	LV 5V	UNIT
Icc	MAX	66	20	0.16	0.16	0.65	0.975	0.28	0.65	mA
Іон	MAX	-0.8	-0.4	-4	-4	-8	-8	-6	-12	mA
lou	MAX	16	8	4	4	8	8	6	12	mA

			STICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	CD74 HC	CD74 HCT	AHC	AHCT	LV 3V	LV 5V
tw			MIN	40	40	30	30	5	5	5	5
to	A (A)		MAX	33	33	90	141	16	12	27.5	16
tPLH	В	1 4	IVIAA	28	44	90		16	12	27.5	16
	A (A)	ā	MAX	40	45	96		16	12	27.5	16
TPHL -	В	1 u	MAX	36	56	96	-	16	12	27.5	16
tPLH	CLEAR	0	MAN	27	27	65	-	13	14	22	13
tphL .	(R)	ā	MAX	40	45	65		13	14	22	13

# DUAL VOLTAGE-CONTROLLED OSCILLATORS WITH ENABLE INPUTS 1999 2018 2018 2018 2018

- Frequency Spectrum: 1Hz to 60MHz
- Typical fmax: 85MHz
- Typical Power Dissipation: 525mW



RECOMMENDED	OPERATING CON	DITION	S
PARAMETER	MAX or MIN	S	UNI
lcc	MAX	150	mA

77110111121211	110.01.01.11111	1	
lcc	MAX	150	mA
Іон	MAX	-1	mA
lor	MAX	20	mA

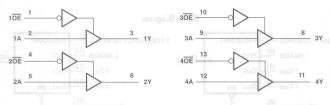
SWITCHING	CHARACTERISTICS

PARAMETER	MAX or MIN	5
fo	MIN	60

UNIT: NS



# Logic Diagram



### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	E	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	SN64 BCT	ABT	UNIT
Icc	MAX	54	20	40	0.08	0.16	0.08	0.16	49	49	30	mA
Іон	MAX	-5.2	-2.6	-15	-6	-6	-6	-6	-15	-15	-32	mA
lou	MAX	16	24	64	6	6	6	6	64	64	64	mA

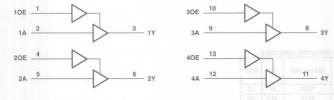
PARAMETER	MAX or MIN	LVTH 3V	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC	UNIT
lcc	MAX	7	0.04	0.02	0.02	0.02	0.01	0.01	mA
Іон	MAX	-32	-8	-8	-8	-16	-24	-24	mA
lou	MAX	64	8	8	8	16	24	24	mA

### SWITCHING CHARACTERISTICS

SVVII CHING CHAR	ACTEMISTICS	,											
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	SN64 BCT	ABT
tPLH	^	V	MAX	13	15	6.5	30	30	33	38	5.7	6	4.9
PHL	А	1	MAX	18	18	8	30	30	33	38	7.7	8	4.9
tPZH			MAX	17	20	8.5	30	38	35	38	10.3	11.1	5.9
tPZL	G	V	MAX	25	25	9	30	38	35	38	11.7	12.8	6.8
tPHZ	ь	Y	MAX	8	20	6	30	38	33	42	8.9	9.4	6.2
tPLZ			MAX	12	20	6	30	38	33	42	8.6	9.9	6.2

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC
tPLH .		v	MAX	3.5	8.5	8.5	13	8.5	4.8	2.8
tphL .	А	Y	MAX	3.9	8.5	8.5	13	8.5	4.8	2.8
tPZH			MAX	4	8	8	13	8	5.4	3.5
tPZL	G	v	MAX	4	8	8	13	8	5.4	3.5
tрнz	G	Y	MAX	4.5	10	10	15	10	4.6	4
tPLZ			MAX	4.5	10	10	15	10	4.6	4

# Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 BCT	SN64 BCT	ABT	LVTH 3V	UNIT
Icc	MAX	62	22	48	0.08	0.16	0.16	51	51	30	7	mA
Гон	MAX	-5.2	-2.6	-15	-6	-6	-6	-15	-15	-32	-32	mA
lou	MAX	16	24	- 64	6	6	6	64	64	64	64	mA

PARAMETER	MAX or MIN	AHC	АНСТ	LV 3V	LV 5V	LVC 3V	ALVC	UNIT
Icc	MAX	0.04	0.02	0.02	0.02	0.01	0.01	mA
Іон	MAX	-8	-8	-8	-16	-24	-24	mA
lou	MAX	8	8	8	16	24	24	mA

SWITCHING CHAP	RACTERISTICS	100					_						
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 BCT	SN64 BCT	ABT	LVTH 3V
tPLH .		v	MAX	13	15	7	30	30	36	6.3	6.3	6.3	3.8
tPHL .	A	Y	MAX	18	18	8.5	30	30	36	7.4	7.4	5.7	3.9
tPZH .			MAX	18	25	8.5	30	38	38	7.9	7.9	6.5	5.4
tPZL			MAX	25	35	8.5	30	38	38	10.5	10.5	6.5	5.2
tPHZ	G	,	MAX	16	25	7.5	30	38	42	10	10	6.8	3.8
tPLZ			MAX	18	25	8	30	38	42	12.3	12.3	6.7	5.5

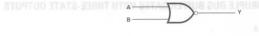
PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LV 5V	LV 3V	TAC 3A	ALVC
tPLH .	, Am	1 ST- V	MAX	8.5	8.5	8.5	13	4.7	3.1
tPHL .	A	ET 1	MAX	8.5	8.5	8.5	13	4.7	3.1
tPZH			MAX	8	8	8	13	5.7	3.3
tPZL			MAX	8	8	8	13	5.7	3.3
tPHZ	G	Y	MAX	10	10	10	15	6	3.7
tPLZ			MAX	10	10	10	15	6	3.7



# **50-** $\Omega$ LINE DRIVERS

 $\bullet$  Y =  $\overline{A + B}$ 





12

RECOMMENDED	OPERATING CON	DITIONS	
PARAMETER	MAX or MIN	TTL	UNIT
Icc	MAX	57	mA
Іон	MAX	-42.4	mA
Ini	MAY	48	mΛ

VI B S AI

SWITCHING CHARACTERISTICS

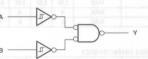
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
tPLH .	A, B	Y	MAX	9
tphL .	A, B	Y	MAX	12

132

# Logic Diagram

# QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

 $Y = \overline{A \cdot B}$ 



### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ΠL	LS	S	SN74 HC	CD74 HC	CD74 HCT	AHC	AHCT	LV 3V	LV 5V	UNIT
Icc	MAX	40	14	68	0.02	0.04	0.04	0.02	0.02	0.02	0.02	mA
Гон	MAX	-0.8	-0.4	-1	-4	-4	-4	-8	-8	-6	-12	mA
In	MAX	16	8	20	4	4	4	8	8	6	12	mA

### SWITCHING CHARACTERISTICS

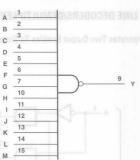
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	SN74 HC	CD74 HC	CD74 HCT	AHC	AHCT	LV 3V	LV 5V
tPLH .	A, B	Y	MAX	22	22	10.5	31	38	50	. 11	10	17.5	11
tPHL .	A, B	Y	MAX	22	22	13	31	38	50	11	8	17.5	11

133

# Logic Diagram

# 13-INPUT POSITIVE-NAND GATES

 $\bullet$  Y =  $\overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M}$ 



# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	S	ALS	SN74 HC	UNIT
Icc	MAX	10	0.34	0.02	mA
Іон	MAX	-1	-0.4	-4	mA
lor.	MAX	20	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	S	ALS	SN74 HC
TPLH	A to M	Y	MAX	6	11	38
tPHL	A to M	Y	MAX	7	25	38

# 136

QUAD EXCLUSIVE-OR GATES WITH OPEN-COLLECTOR OUTPUTS

 $\bullet$  Y = A  $\oplus$  B =  $\overline{A}B + \overline{A}B$ 

# **FUNCTION TABLE**

	1 01	10110	HA IMPLE
ľ	INP	UTS	OUTPUT
ľ	Α	В	Y
ľ	L	L	L
ı	L	H	H
ı	H	L	H
ı	H	Н	L

# Logic Diagram



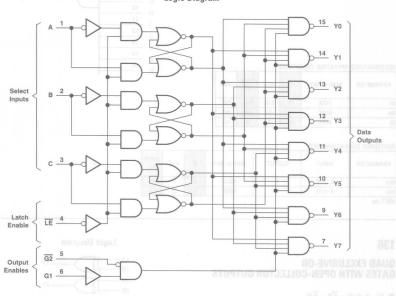
RECOMMENDED OF	ERATING CUNDITI	UNS				_
PARAMETER	MAX or MIN	TTL	LS	ALS	AS	UNIT
Icc	MAX	50	10	5.9	31	mA
Vон	MAX	5.5	5.5	5.5	5.5	V
lou	MAX	16	8	8	20	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	AS
tPLH	A or B	Y (Other Output = L)	MAX	18	30	50	12.5
tphl.	A or B	Y (Other Output = L)	MAX	50	30	15	7.1
tPLH	A or B	Y (Other Output = L)	MAX	22	30	50	11.4
tPHL .	A or B	Y (Other Output = L)	MAX	55	30	15	10.7

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters. See www.ti.com/sc/logic for the most current data sheets.





L	Н	L	L	H	L	H	H	L	H	H	Н	Н	H
L	H	L	L	H	Н	H	H	H	L	H	H	H	H
L	Н	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н
L	H	L	H	L	H	H	Н	H	H	H	L	H	H
L	Н	L	H	H	L	H	H	H	H	Н	H	L	H
L	H	L	H	Н	Н	H	Н	H	Н	H	H	H	L
Н	Н	L	Х	X	X	Dep	ends u	pon thas at a	ne add a logic	ress p	reviou	sly ap	plied

### RECOMMENDED OPERATING CONDITIONS

HEGGIVIIVIEIVEE	OI LIMITING COIL	DITTOTE	,			1.11			
PARAMETER	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	UNIT
Icc	MAX	18	11	24	0.08	0.16	0.08	0.16	mA
Іон	MAX	-0.4	-0.4	-2	-4	-4	-4	-4	mA
lou	MAX	8	8	20	4	4	4	4	mA

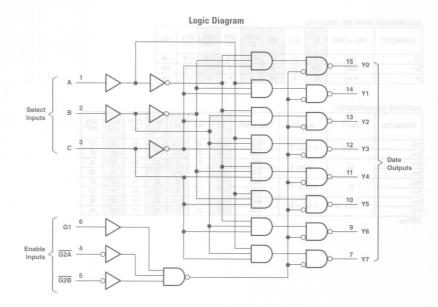
# SWITCHING CHARACTERISTICS

SWITCHING CHA	TIMOTETTOO			_			_			_
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT
tplh	A D C	V (0D74. V)	MAX	24	20	12.5	48	54	48	57
tphl.	A, B, C	Y (CD74: Y)	MAX	38	20	12.5	48	54	48	57
tPLH .	- <u>G2</u>	V (CD74. V)	MAX	21	12	8	36	44	36	56
tPHL .	62	Y (CD74: Y)	MAX	27	15	8.5	36	44	36	56
tPLH .	G1	Y (CD74; Y)	MAX	21	17	10	36	44	36	53
tPHL .	- 61	Y (CD74: Y)	MAX	27	15	9	36	44	36	53
tPLH	LE (CD74: LE)	V (CD74. V)	MAX	27	22	13.5	48	57	52	66
tphl .	LE (GD/4: LE)	Y (CD74: Y)	MAX	38	20	14	48	57	52	66

IINIT:ns

# 3-TO-8 LINE DECODERS/DEMULTIPLEXRS

- 3 Enable Inputs to Simplify Cascading and /or Data Reception
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



								-	_			
	INPI	JTS						TUC	DIII	re		
EN	ABLE	SE	LE	CT			-	100	PUI	5		
G1	G2*	C	В	Α	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	Н	X	X	X	H	Н	Н	Н	Н	Н	Н	Н
L	X										Н	
H	L	L	L	L	L	H	H	H	H	H	H	H
Н	L	L	L	Н	H	L	H	Н	H	H	H	H
H	L	L	H	L	Н	H	L	H	H	H	H	H
Н	L	L	H	Н	H	H	Н	L	Н	Н	H	H
Н	L	H	L	L	H	H	Н	H	L	Н	Н	H
Н	L	Н	L	Н	Н	H	H	H	H	L	Н	H
H	L	Н	H	L	H	H	Н	Н	Н	H	L	Н
H	L	H	H	Н	Н	H	Н	H	Н	H	H	L

 $\overline{G}2^* = \overline{G}2A*\overline{G}2B$ 

# DECOMMENDED OBERATING CONDITIONS

RECOMMENDED	UPENATING CON	DITIONS		1			01174	0074	00174	0074	4.0	
PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	UNIT
Icc Pyr	MAX	10	74	10	20	20	0.08	0.16	0.08	0.16	0.04	mA
Іон	MAX	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	mA
lor	MAX	8	20	8	20	20	4	4	4	4	24	mA

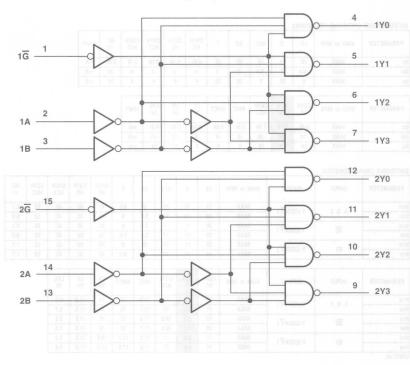
	3	1		-01						
PARAMETER	MAX or MIN	CD74 AC	ACT 11	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
Icc	MAX	0.16	0.04	0.16	0.04	0.04	0.02	0.02	0.01	mA
Іон	MAX	-24	-24	-24	-8	-8	-6	-12	-24	mA
lou	MAX	24	24	24	8	8	6	12	24	mA

# SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11
									nc nc	nc.	nci	nui	1.1
tPLH	A, B, C	Y (CD74:\(\overline{Y}\))	MAX	27	12	22	10	8.5	45	45	45	53	8.1
tPHL TYS —	A, D, U	1 (6074.1)	MAX	39	12	18	9.5	9	45	45	45	53	8.8
tPLH	G2	Y (CD74:Y)	MAX	26	11	17	7.5	8	39	53	42	53	8.3
tphl .	02	1 (6074.1)	MAX	38	11	17	8.5	7.5	39	53	42	53	8.3
tPLH .	GF G1	Y (CD74:\(\overline{Y}\)	MAX	26	11	17	10	9	39	53	42	53	7.5
tPHL CYC -	GI	Y (CD/4:Y)	MAX	38	-11	17	10	8.5	39	53	42	53	7.7

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 AC	ACT 11	CD74 ACT	AHC	AHCT	TA TA	LV 5V	LVC 3V
tPLH .	4.0.0	V (0074 V)	MAX	-11	9.8	12	11.5	13	18	11.5	6.7
tphl.	A, B, C	Y (CD74:Y)	MAX	11	9.7	12	11.5	13	18	11.5	6.7
tPLH .	G2	V (ODZAVI)	MAX	10	8.9	10.5	11.5	12	18	11.5	6.5
<b>TPHL</b>	62	Y (CD74:Y)	MAX	10	8.9	10.5	11.5	12	18	11.5	6.5
tPLH	0.	Y (CD74:Y)	MAX	11	9.3	11	11.5	11.5	18.5	11.5	5.8
tPHL .	G1	Y (CD/4:Y)	MAX	11	9.8	11	11.5	11.5	18.5	11.5	5.8

# Logic Diagram



INPL	JTS				PUT	_
ENABLE	SEL	ECT		100	PUI	5
G	В	A	Y0	Y1	Y2	YS
Н	X	X	Н	Н	Н	Н
L	L	L	L	H	H	H
L	L	H	H	L	H	Н
L	Н	L	Н	Н	L	Н
1	H	н	H	H	н	1

# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	CD74 AC	ACT 11	CD74 ACT	UNIT
Icc	MAX	11	90	13	0.08	0.08	0.08	0.16	0.16	0.08	0.16	mA
Іон	MAX	-0.4	-1	-0.4	-4	-4	-4	-4	-24	-24	-24	mA
lou	MAX	8	20	8	4	4	4	4	24	24	24	mA

PARAMETER	MAX or MIN	AHC	AHCT	SV SV	LV 5V	LVC 3V	UNIT
lcc	MAX	0.04	0.02	1.	0.02	0.01	mA
Іон	MAX	-8	-8	-6	-12	-24	mA
loL	MAX	8	8	6	12	24	mA

# SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	CD74 AC	ACT 11	CD74 ACT
tPLH .	A or B	Y (CD74: Y)	MAX	29	12	14	44	44	43	51	10.5	8.5	11.5
tPHL	A or B	Y (CD74: Y)	MAX	38	12	14	44	44	43	51	10.5	8.5	11.5
tPLH	G	Y (CD74: Y)	MAX	24	8	14	44	41	43	51	10.5	7.9	12
tPHL .	G	Y (CD74: Y)	MAX	32	10	15	44	41	43	51	10.5	7.5	12

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LV 3V	LV 5V	LVC 3V
tplH .	A or B	Y (CD74: Y)	MAX	10.5	10.5	16.5	10.5	6.2
tPHL	A or B	Y (CD74: Y)	MAX	10.5	10.5	16.5	10.5	6.2
tPLH .	G	Y (CD74: Y)	MAX	9.5	9.5	14.5	9.5	4.7
tphl .	G	Y (CD74: Y)	MAX	9.5	9.5	14.5	9.5	4.7

Logic Diagram 1A 1A 1B 1C 1C 1D 1Y 1Y 1Y 1Y 12A 2B 2C 2C 2Y

 $\bullet$  Y =  $\overline{\mathsf{ABCD}}$ 

RECOMMENDED	OPERATING CON	DITION	S			2		avia (Tri	James Alizado	
PARAMETER	MAX or MIN	S	UNIT							
Icc	MAX	44	mA							
Іон	MAX	-40	mA							
lou	MAX	60	mA							

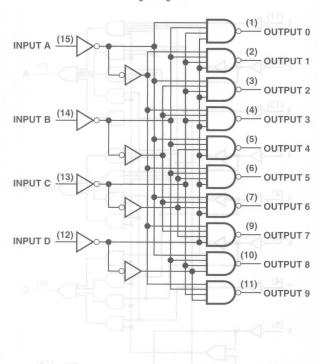
SWITCHING CHARACTERISTICS

SWITCHING CHA	MAGILINGTICS			THE REAL PROPERTY.
PARAMETER	INPUT	OUTPUT	MAX or MIN	S
tPLH	A, B, C, D	V	MAX	6.5
tphl .	A, B, C, D	T	MAX	6.5

# BCD-TO-DECIMAL DECODERS/DRIVERS FOR LAMPS, RELAYS, MOS NO WITH BOUND BALLAGOT AND

- Sink-Current Capability: 80mA
- Low Power Dissipation (SN74LS): 35mW (typ)

# Logic Diagram



# FUNCTION TABLE

No.		INP	UTS						OUT	PUTS	ê				_
NO.	D	C	В	Α	0	1	2	3	4	5	6	7	8	9	
0	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	
1	L	L	L	H	H	L	H	H	H	Н	H	Н	H	Н	
2	L	L	H	L	H	H	L	H	H	Н	Н	Н	Н	Н	
3	L	L	H	H	Н	H	H	L	H	H	Н	Н	H	Н	
4	L	Н	L	L	Н	H	Н	H	L	H	H	Н	H	H	
5	L	Н	L	Н	Н	Н	н	Н	Н	L	Н	Н	Н	Н	
6	L	H	H	L	H	Н	H	Н	H	H	L	Н	H	H	
7	L	Н	H	H	Н	Н	Н	H	Н	Н	Н	L	Н	Н	
8	H	L	L	L	Н	H	Н	Н	H	H	Н	Н	L	н	
9	H	L	L	H	н	H	H	H	H	H	H	H	H	L	
	Н	L	H	L	Н	Н	H	Н	Н	Н	Н	Н	Н	Н	
0	H	L	H	H	H	H	H	H.	H	H	Н	H	н	Н	
INVALID	H	H	L	L	Н	H	Н	Н	Н	Н	Н	Н	Н	Н	
\$	H	Н	L.	Н	Н	Н	Н	Н	Н	Н	Н	Н	н	Н	
Z	Н	H	Н	L	H	Н	Н	Н	н	Н	Н	Н	н	Н	
	Н	H	Н	H	Н	H	Н	Н	Н	Н	Н	Н	Н	Н	

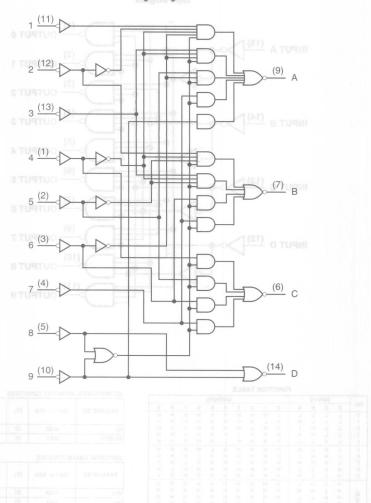
# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
Icc	MAX	70	13	mA
Vo (OFF)	MAX	15	15	mA

## SWITCHING CHARACTERISTICS

PARAMETER	MAX or MIN	TTL	LS
tplH	MAX	50	50
tphl.	MAX	50	50

# Logic Diagram



961

-TO 3-LINE DETAIL PRIORITY ENCODERS

	INPUTS										PUTS	
1	2	3	4	5	6	7	8	9	D	С	В	Α
Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	H	Н	Н
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	Н
X	X	X	X	X	X	L	H	H	Н	L	L	L
X	X	X	X	X	L	H	H	H	Н	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	Н	Н	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	Н	Н	H	H	Н	Н	Н	H	H	L	H
L	H	H	Н	H	H	H	H	Н	Н	H	H	L

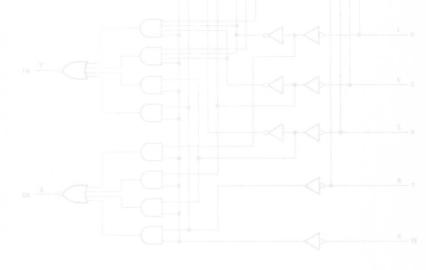
Logic Diagram

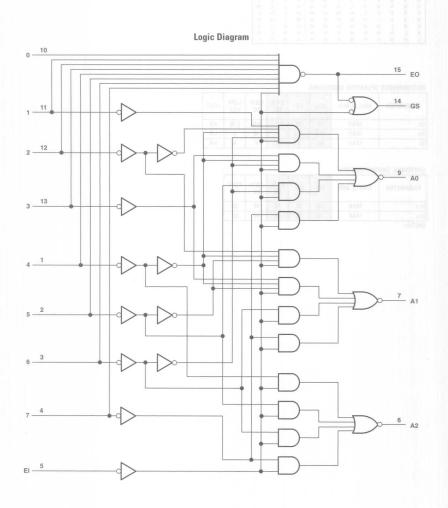
COMMEN	NDED OP	FRATING	CONDITIONS	

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
lcc	MAX	70	20	0.08	0.16	0.16	mA
Іон	MAX	-0.8	-0.4	-4	-4	-4	mA
loL	MAX	16	8	- 4	4	4	mA

# SWITCHING CHARACTERISTICS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	
tPLH	MAX	19	33	48	48	53
tPHL .	MAX	19	23	48	48	53





			11	IPUT:	S					O	UTPU	TS	
El	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
Н	X	X	X	X	X	X	X	X	Н	H	Н	Н	Н
L	Н	H	H	H	H	H	H	H	Н	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	Н
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	Н
L	X	X	X	X	L	H	Н	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	Н	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

1-OF-16 DATA SELECTOR

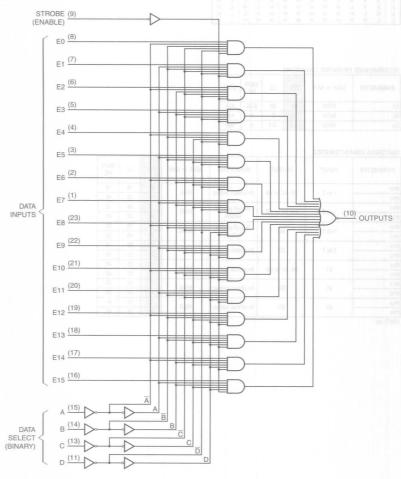
Legic Diagr

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	UNIT
Icc	MAX	60	20	0.08	mA
lou	MAX	16	- 8	4	mA
Іон	MAX	-0.8	-0.4	-4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	WAVEFORM	MAX or MIN	TTL	LS	SN74 HC
tPLH	14-7	40.4140	In advantage of	MAX	15	18	45
tPHL .	1 to 7	A0, A1 or A2	In-phase output	MAX	14	25	45
tPLH	17	A0, A1 or A2	Out-of-phase	MAX	19	36	45
tPHL THE TOTAL OF	1 to 7	AU, AT OF AZ	output	MAX	19	29	45
tPLH	04-7	EO	Out-of-phase	MAX	10	18	38
tPHL	0 to 7	EU	output	IVIAA	25	40	38
tPLH .	0 7	GS	In Continue	MAN	30	55	48
tPHL .	0 to 7	65	In-phase output	MAX	25	21	48
tPLH		40.4140		1447	15	25	49
tPHL .	E1	A0, A1 or A2	In-phase output	MAX	15	25	49
tPLH .		00		MANY	12	17	36
tPHL.	E1	GS	In-phase output	MAX	15	36	36
tPLH .	F1	50	la absentant	MAX	15	21	41
tPHL .	E1	EO	In-phase output	IVIAX	30	35	41



**FUNCTION TABLE** 

		INP	UTS		
	SEL	ECT		STROBE	OUTPUT
D	C	В	Α	G	VV
X	X	X	X	Н	H
L	L	L	L	L	E0
L	L	L	H	L	E1
L	L	H	L	L	E2
L	L	H	H	L	E3
L	H	L	L	L	E4
L	H	L	H	L	E5
L	H	Н	L	L	E6
L	H	H	H	L	E7
H	L	L	L	L	E8
H	L	L	H	L	E9
Н	L	H	L	L	E10
H	L	H	H	L	E11
H	Н	L	· L	L	E12
H	H	L	H	L	E13
Н	H	Н	L	L	E14
H	H	H	H	L	E15

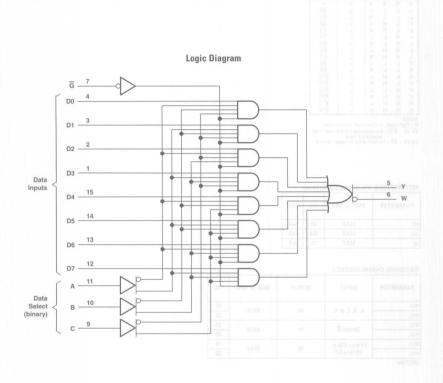
# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
Icc	MAX	48	mA
Іон	MAX	-0.8	mA
lou	MAX	16	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
tplH	A D C D	W	MAX	35
TPHL.	A, B, C or D	VV	WAA	33
tplH	Strobe G	147	2447	24
tphL .	Strone G	W	MAX	30
tPLH	E0 thru E15 or		MANY	14
<b>TPHL</b>	E0 thru D7	W	MAX	20

# 8-TO-1 LINE DATA SELECTORS/MULTIPLEXERS



	INI	PUTS	OUTPUTS				
S	ELEC	Т		0011	PUIS		
C	В	Α	G	Y	W		
X	X	X	Н	L	Н		
L	L	L	L	D0	D0		
L	L	Н	L	D1	D1		
L	H	L	L	D2	D2		
L	Н	Н	L	D3	D3		
H	L	L	L	D4	D4		
Н	L	H	L	D5	D5		
Н	H	L	L	D6	D6		
H	H	н	L	D7	D7		

# 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

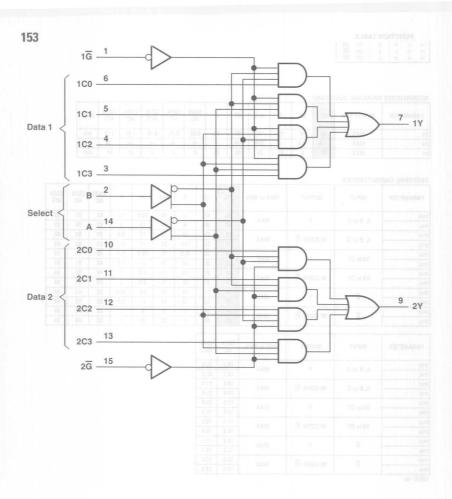
# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
Icc	MAX	48	10	70	12	30	21	0.08	0.16	0.16	0.16	0.16	mA
Іон	MAX	-0.8	-0.4	-1	-2.6	-15	-1	-6	-4	-4	-24	-24	mA
lor	MAX	16	8	20	24	48	24	6	4	4	24	24	mA

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	ОИТРИТ	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT
tplh	A D C	Y	MANY	38	43	18	18	14.5	12	63	56	62
tphl.	A, B or C	τ.	MAX	38	30	18	24	15	9	63	56	62
tplH	A D 0	W (CD74; Y)	1444	26	23	15	24	12	9.5	63	62	65
tpht.	A, B or C	VV (CD74: Y)	MAX	30	32	13.5	23	12	7.5	63	62	65
tPLH	D0 to D7	v	MAX	20	32	16.5	10	10.5	7.5	49	51	57
tPHL .	DU to D7	1		27	26	18	15	11	7.5	49	51	57
tPLH .	D0 to D7	W (CD74: Y)	MANY	14	21	13	15	6.5	7	49	56	54
tphl.	DU to D7	VV (CD/4: Y)	MAX	14	20	12	15	4.5	5	49	56	54
tplH	G	Y	****	33	42	12	18	14	10.5	32	42	44
tPHL .	6	1	MAX	33	32	12	19	11	7.5	32	42	44
tPLH	G	W (0D34 V)	MAN	21	24	7	19	6	7	32	44	54
tPHL	G	W (CD74: Y)	MAX	23	30	7	23	10	6	32	44	54

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 AC	CD74
tPLH .	A D C	Y	MANY	18.2	20.2
tphL .	A, B or C	T T	MAX	18.2	20.2
tplH	A. B or C	W (CD74: Y)	MAX	19.6	21.6
tPHL .	A, B or C	VV (CD/4: Y)	IVIAX	19.6	21.6
tplH	D0 +- D7	Υ	MAN	13.5	15.5
tphl.	D0 to D7	1	MAX	13.5	15.5
tplH .	D0 4- D7	W (CD74: Y)	MAY	14.9	16.9
tphl.	D0 to D7	VV (CD/4: Y)	MAX	14.9	16.9
tplH	G	Y	MAN	12.2	12.1
tPHL .	G	1	MAX	12.2	12.1
tPLH	G	W (CD74: Y)	MAN	13.5	13.5
tPHL .	G	VV (CD/4: Y)	MAX	13.5	13.5



ì	11	6	F	INC.	TION	TARI	F _	
ı	Н	H	X	X	X	L	L	L
ı	Н	Н	X	X	X	H	L	H

RECOMMENDED OPERATING CONDITIONS

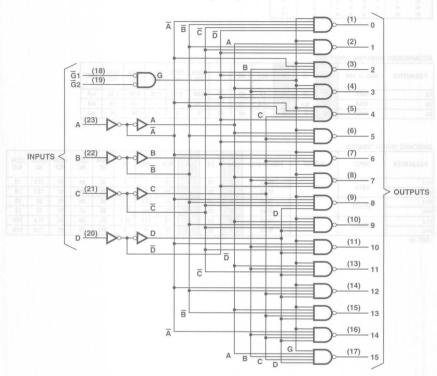
PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
Icc	MAX	60	10	70	14	33	20	0.08	0.16	0.16	0.16	0.16	mA
Іон	MAX	-0.8	-0.4	-1	-2.6	-15	-1	-6	-4	-4	-24	-24	mA
lou	MAX	16	8	20	24	48	20	6	4	4	24	24	mA

### CMUTCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
tplH	DATA		MAX	18	15	9	10	7	8	35	44	51	13.3	18
tPHL .	DATA	4	MAX	23	26	9	15	8	7.5	35	44	51	13.3	18
tPLH .	OFLEGE		MAX	34	29	18	21	12.5	12	38	48	51	20	22
tphl .	SELECT	1	MAX	34	38	18	21	11	10.5	38	48	51	20	22
tPLH	STROBE Y	ATROPE V	MAX	30	24	15	18	11.5	10.5	24	36	41	11.8	12.6
tPHL .		Y	MAX	23	32	13.5	18	- 9	8	24	36	41	11.8	12.6

# 4-LINE TO 16-LINE DECODER/DEMULTIPLEXER

Logic Diagram



		INP	UTS										OUT	PUTS							
G1	G2	D	С	В	Α	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	Н	L	L	L	L	Н	H	Н	Н	Н	H	Н	Н	Н	Н	H	Н	Н	Н	Н
L	L	L.	L	L	н	Н	L	H	Н	Н	H	H	H	H	Н	H	Н	H	H	H	H
L	L	L	L	H	L	Н	H	L	H	H	H	H	H	Н	H	Н	H	H	H	H	H
L	L	L	L	H	H	Н	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	Н	L	L	Н	Н	H	Н	L	Н	H	Н	H	H	H	H	H	Н	Н	Н
L	L	L	H	L	Н	Н	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	Н	L	Н	H	H	H	Н	Н	L	H	H	H	H	H	Н	H	H	Н
L	L	L	H	H	Н	Н	H	H	H	Н	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	н	Н	H	H	H	H	H	H	L	H	H	H	Н	H	Н	Н
L	Ŀ	Н	L	L	H	Н	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	Н	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	Н	L	Н	Н	Н	H	H	H	Н	H	H	H	H	H	H	L	H	Н	H	Н
L	L	Н	H	L	L	Н	H	H	H	H	H	H	H	H	H	H	H	L	H	H	Н
L	L	H	H	L	Н	H	H	H	H	H	Н	H	H	H	H	H	H	H	L	H	Н
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	Н	H	H	H	H	L	H
L	L	H	H	H	Н	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	Н	X	X	X	X	H	H	H	H	H	H	H	Н	H	H	H	H	H	H	Н	H
H	L	X	X	X	X	Н	H	H	H	Н	H	H	Н	H	H	H	Н	H	H	H	H
H	Н	X	X	X	X	н	H	Н	Н	H	H	Н	Н	H	H	H	Н	Н	Н	Н	Н

#### RECOMMENDED OPERATING CONDITIONS

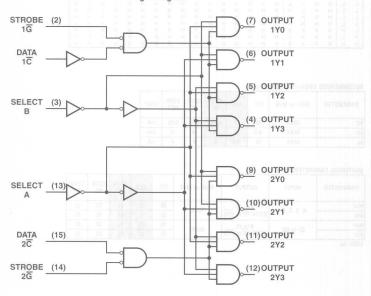
PARAMETER	MAX or MIN	TTL	ALS	SN74 HC	CD74 HC	CD74 HCT	UNIT
lcc	MAX	56	23	0.08	0.16	0.16	mA
Іон	MAX	-0.8	24	-4	-4	-4	mA
lor	MAX	16	-0.4	4	4	4	mA

#### SWITCHING CHARACTERISTICS U.O. (8)

	nvi						1	
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	ALS	SN74 HC	CD74 HC	CD74 HCT
tPLH	ARCD	0 to 15	MAX	36	12	45	53	53
tPHL	A, B, C, D	(CD74: Y0 to Y15)	IVIAA	33	12	45	53	53
tPLH	G1 to G2	0 to 15	MAX	30	12	45	53	51
tPHL .	G1 t0 G2	(CD74: Y0 to Y15)	IVIAA	27	12	45	53	51

UNIT: ns

# Logic Diagram



**FUNCTION TABLES** 

2-LINE	TO	4-LINE	DECODER OR
1-LINE	TO	4-I INF	DEMULTIPLEXER

		INPUTS			OUT	PUTS	
SEL	ECT	STROBE	DATA				
В	Α	1G	1C	110	111	112	173
X	X	Н	X	Н	Н	Н	Н
L	L	L	H	L	H	H	Н
L	H	L	H	H	L	Н	Н
H	L	L	H	H	H	L	Н
H	H	L	H	Н	H	H	L
X	X	X	L	H	H	H	H

#### 2-LINE TO 4-LINE DECODER OR

		INPUTS		OUTPUTS					
SELECT		STROBE	DATA						
В	Α	2G	2C	2Y0	2Y1	2Y2	2Y3		
X	X	Н	X	Н	Н	Н	Н		
L	L	a.L	L	L	H	H	Н		
L	H	O.L	L	H	L	H	Н		
Н	L	L	L	H	H	Ĺ	H		
Н	H	L	L	H	H	H	L		
X	X	X	H	H	H	H	Н		

# 3-LINE TO 8-LINE DECODER OR 1-LINE TO 8-LINE DEMULTIPLEXER

		INPU	rs				OUT	PUTS			
s	ELEC	т	STROBE or DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	В	Α	G‡	2Y0	2Y1	2Y2	2Y3	110	1Y1	1Y2	113
X	X	Х	Н	Н	Н	Н	Н	Н	Н	Н	Н
L	L	L	L	L	H	H	Н	Н	H	H	Н
L	L	H	L	H	L	H	Н	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	Н
H	L	L	L	H	H	H	H	L	H	Н	H
H	L	Η.	L L	H	H	H	H	H	L	Н	Н
Н	H	L	L	H	Н	H	Н	Н	H	L	Н
Н	H	H	L	H	H	H	Н	Н	Н	Н	L

# † C = inputs 1C and 2C connected together ‡ G = inputs 1G and 2G connected together

#### RECOMMENDED OPERATING CONDITIONS

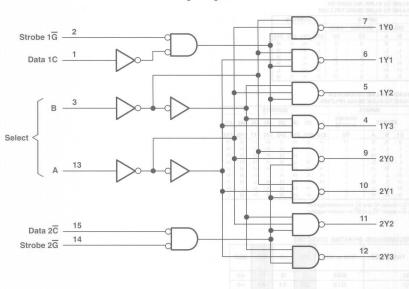
PARAMETER	MAX or MIN	TTL	LS	ALS	UNIT
Icc	MAX	40	10	13	mA
Юн	MAX	-0.8	-0.4	-0.4	mA
lou	MAX	16	8	8	mA

SWITCHING CHAR	ACTERISTICS					
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS
tPLH	A or B	Y	MAX	32	26	14
tPHL .	A or B	1 '	MAX	32	30	12
tPLH .	1C	v	MAN	24	27	12
tPHL .	10	1 '	MAX	30	27	14

# **DECODERS/DEMULTIPLEXERS**

- Individual Strobes Simplify Cascading for Decoding or Demultiplexing Lager Words
- Outputs: Open-Collector

# Logic Diagram



2-LINE TO 4-LINE DECODER OR 1-LINE TO 4-LINE DEMULTIPLEXER

		INPUTS			OUT	PUTS	
SELECT		STROBE	DATA				
В	Α	1G	1C	1Y0	111	112	1Y3
X	X	Н	X	Н	Н	Н	Н
L	L	L	H	L	H	H	Н
L	H	L	H	Н	L	H	Н
H	L	L	H	H	H	L	Н
Н	H	L	H	Н	H	H	L
v	v	V	1	1.1	1.1	1.7	1.2

2-LINE TO 4-LINE DECODER OR

		INPUTS			OUT	PUTS	
SEL	ECT	STROBE	DATA				
В	Α	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	Н	Н	Н
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
Н	L	L	L	H	H	L	H
H	H	L	L	H	H	Н	L
X	X	X	H	H	H	H	Н

3-LINE TO 8-LINE DECODER OR 1-LINE TO 8-LINE DEMULTIPLEXER

		INPU'	rs	1			OUT	PUTS			
S	ELEC	т	STROBE or DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
Ct	В	Α	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	111	1Y2	1Y3
Х	X	X	H	Н	Н	Н	Н	Н	Н	H	Н
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	Н	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	Н	H	H	Н
H	L	L	L	H	H	H	H	L	H	Н	H
H	L	Н	L	Н	H	H	H	H	L	H	H
H	H	L	L	Н	H	H	H	H	H	L	Н
H	H	H	L	H	H	H	H	H	H	H	1

† C = inputs 1C and 2\overline{\overline{C}} connected together ‡ \overline{G} = inputs 1\overline{G} and 2\overline{G} connected together

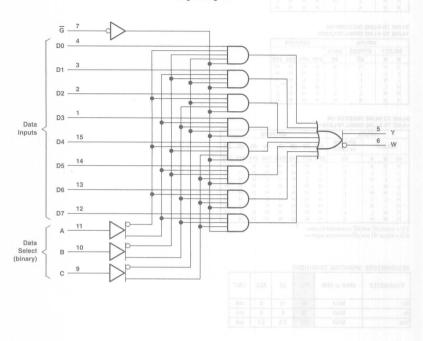
RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	UNIT
Icc	MAX	40	10	9	mA
lou	MAX	16	8	8	mA
Vон	MAX	5.5	5.5	5.5	mA

SWITCHING CHARACTERISTICS

SWITCHING CHAP	RACTERISTICS				_	_
PARAMETER	INPUT	ОИТРИТ	MAX or MIN	TTL	LS	ALS
tPLH	2C	V	MAX	23	40	38
tPHL .	2 <u>C</u> 1 <u>G</u> or 2 <u>G</u>	Ť	IVIAX	30	51	22
tPLH	A or B		DAAW.	34	46	55
TPHL	A or B	Y	MAX	34	51	25
tplH .	1C	v	MAN	27	48	50
PHL	1C	1 ,	MAX	33	48	23

UNIT: ns



	INPUTS	ОИТРИТ		
STROBE	SELECT	Α	В	OUIPUI
Н	X	X	X	L
L	L	L	X	L
L	L	H	×	H
L	H	X	L	L
L	H	X	H	H

#### RECOMMENDED OPERATING CONDITIONS

HECOMINIEMAEN	OFENATING CON	DITIONS	)	_								
PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	UNIT
Icc -	MAX	48	16	78	11	28	23	0.08	0.16	0.08	0.16	mA
Іон	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-6	-4	-6	-4	mA
lor	MAX	16	8	20	8	20	20	6	4	6	4	mA

PARAMETER	MAX or MIN	CD74 AC	CD74 ACT	АНС	AHCT	LV 3V	LV 5V	TAC 3A	UNIT
Icc	MAX	0.16	0.16	0.04	0.02		0.0.2	0.01	mA
Іон	MAX	-24	-24	-8	-8	-6	-12	-24	mA
lou YS	MAX	24	24	8	8	6	12	24	mA

#### SWITCHING CHARACTERISTICS

OTTITO OTTA	MOTERIO	_			_								
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT
tPLH	DATA	V	MAN	14	14	7.5	14	6	6.5	32	38	35	38
tPHL .	DATA	Υ.	MAX	14	14	6.5	12	5.5	7	32	38	35	38
tPLH .	STROBE	v	MAX	20	20	12.5	20	10.5	-11	29	41	33	41
tphl.	STRUBE	1	IVIAA	21	21	12	13	7.5	7	29	41	33	41
tPLH .	SELECT	v	MAN	23	23	15	24	11	11	31	44	40	44
tPHL .	SELECT	1	MAX	27	27	15	17	10	8	31	44	40	44

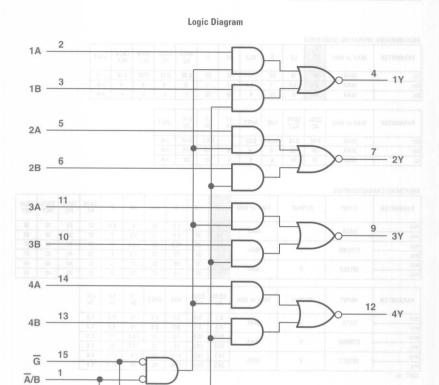
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 AC	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	
tPLH .	DATA	V	MAX	8.5	9.5	9.5	9.8	15	9.5	5.2	
tphl -	DATA	- 1	IVIAA	8.5	9.5	9.5	9.8	15	9.5	5.2	
tPLH	STROBE	V	MAX	13.5	13.5	12	12	19.5	12	6.5	
tPHL.	STRUBE	(1)	IVIAA	13.5	13.5	12	12	19.5	12	6.5	
tPLH .	SELECT	v	MAX	14.5	14.5	11.5	12	19	11.5	6.8	
tPHL .	SELECT	1	IVIAX	14.5	14.5	11.5	12	19	11.5	6.8	

UNIT: ns

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# QUAD 2-TO-1 LINE DATA SLECTORS/MULTIPLEXERS

Buffered Inputs and Outputs



	INPUTS	OUTPUT		
STROBE	SELECT	Α	В	OUTPUT
Н	X	X	X	H
L	L	L.	×	H
L	L	Н	×	L
L	H	X	L	Н
L	H	×	Н	L

#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	UNIT
Icc	MAX	11	81	10	22.5	15	0.08	0.16	0.16	mA
Іон	MAX	-0.4	-1	-0.4	-2	-1	-6	-4	-4	mA
lou	MAX	8	20	8	20	20	6	4	4	mA

PARAMETER	MAX or MIN	CD74 AC	CD74 ACT	AHC	AHCT	UNIT
Icc	MAX	0.16	0.16	0.04	0.02	mA
Іон	MAX	-24	-24	-8	-8	mA
lou	MAX	24	24	8	8	mA

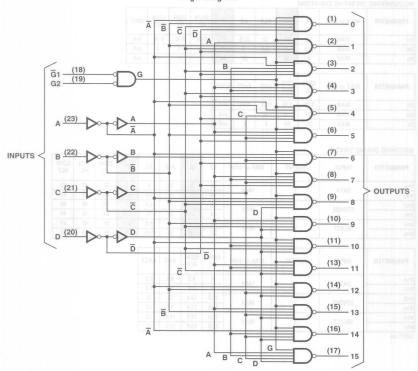
#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	ОИТРИТ	MAX or MIN	LS	s	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT
tPLH	DATA		BAAN.	12	6	15	5	7	32	42	42
tPHL .	DATA	Y	MAX	15	6	8	4.5	4.5	32	42	42
tPLH	OTDODE	1		17	11.5	18	6.5	7	29	48	48
tPHL .	STROBE	Y	MAX	24	12	18	10	6.5	29	48	48
tPLH	0 - 100	o( , )	****	20	12	18	9.5	9.5	31	45	45
tPHL	SELECT	Y	MAX	24	12	18	10.5	7	31	45	45

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 AC	CD74 ACT	AHC	AHCT
tPLH	DATA	v	MAN	8	9.2	9.5	9.8
tphL.	DATA		MAX	8	9.2	9.5	9.8
tPLH .	OTDODE		MANY	11.9	12.4	12	12
tphL .	STROBE	1	MAX	11.9	12.4	12	12
tplh .	OFLEGE		1447	12.9	13.5	11.5	12
tphL .	SELECT	Y	MAX	12.9	13.5	11.5	12

UNIT: ns

# **Logic Diagram**



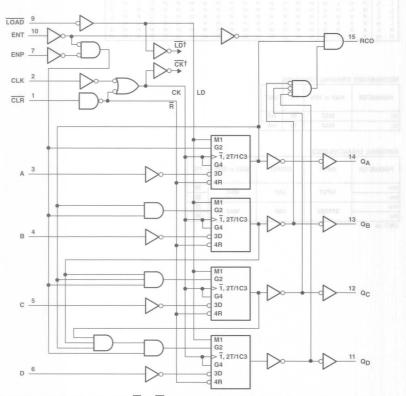
									FUN	CTIC	N T	ABL	E									
			UTS											PUT								
L L	G2 L L L L L L L L L L L L L L H L H	D L L L L L L H H H H H H H H X X X	C L L L H H H H L L L L H H H H X X X	B L L H H L L H H L L H H X X X	A L H L H L H L H L H L H X X X		HHHHH	2		4	5	6 1111111111111111	7	8 H H H H H H H H H H H H H H H H H H H	9 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	10 H H H H H H H H H H H H H H H H H H H	12	13 H H H H H H H H H H H H H H H H H H H	14	15 H H H H H H H H H H H H H H H H H H H	4-BIT BING	
			T		ATING	4	T	E-		7												
PAR	IAM	ETER	1	MA	X or		T	TL	UNI	r												
CC OL			_		MAX		_	16	mA mA													
		ETER	1		INPU	Г		0	TPUT		MA	X or	515 515		TTL 36							
TPHL TPLH			4	_		_	+	-		4			100	1	36 25	-						
PHL		İ	88	S	TROB	E		A	NY		85	MA)	( SB	I.	36							
UNIT:	ns																					
										-0												

Ther simplicity, reuting of complementary signals LD and CK is not shown on the central logic diagram. The uses of these signals are contine topic diagram of the D4 file-dops.

#### **SYNCHRONOUS 4-BIT BINARY COUNTERS**

- Asynchronous Clear Function
- Carry Output for n-Bit Cascading

# Logic Diagram



<sup>†</sup> For simplicity, routing of complementary signals  $\overline{LD}$  and  $\overline{CK}$  is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

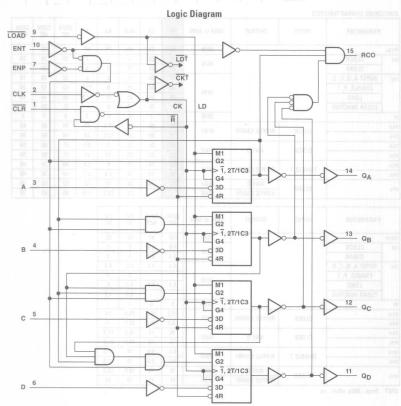
#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	LV 3V	LV 5V	UNIT
Icc	MAX	101	32	21	53	55	0.08	0.16	0.16	0.08	0.08	-	0.02	mA
Іон	MAX	-0.8	-0.4	-0.4	-2	-1	4	-4	-4	-24	-24	-6	-12	mA
lou	MAX	16	8	8	20	20	-4	4	4	24	24	-6	12	mA

#### SWITCHING CHARACTERISTICS

SWIT	CHING CHARACTERIS	TICS		mangeru c	Bind		,			,		_
	PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	AS	<i>E</i> 1	SN74 HC	CD74 HC	CD74 HCT
fmax	81V		00	MIN	25	25	40	75	90	25	20	20
tw	CLOCK			MIN	25	25	-	- /	7	20	24	24
	CLEAR			IVIIN	20	20	15	8	5	20	30	30
tsu	INPUT A, B, C, D			1.3	20	20	15	8	5	38	18	15
	ENABLE, P, T				20	20	15	8	11.5	43	15	20
	LOAD			MIN	25	20	15	8	11.5	34	18	18
	CLEAR INACTIVE				20	25	10	8		31	20	153
th				MIN	0	3	0	0	2	0	3	5
tPLH		OL OOK	DIDDLE CARRY	MAN	35	35	20	16.5	15	54	56	63
tPHL		CLOCK	RIPPLE CARRY	MAX	35	35	20	12.5	15	54	56	63
tPLH		01.001	*****	14437	25	24	15	7	9.5	51	56	59
tPHL		CLOCK	ANY Q	MAX	29	27	20	13	11	51	56	59
tPLH			FALADIE T DIDDLE GADDY	MAX	16	14	13	9	8.5	49	36	48
tPHL	AD -1	ENABLE T	RIPPLE CARRY	MAX	16	14	13	8.5	8.5	49	36	48
tphl CLEAR	OLEAD	ANY Q	MAX	38	28	24	13	13	53	63	75	
	RIPPLE CARRY	MAX		N	23	12.5	11.5	55	63	75		

	PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 AC	CD74 ACT	3V	LV 5V
fmax	> ag	5-10-0	<	MIN	103	91	50	85
tw	CLOCK		4	GE MIN	4.8	5.4	5	5
	CLEAR			MIN	4.4	5.3	5	5
tsu	INPUT A, B, C, D				4.4	4.4	6.5	4.5
	ENABLE, P, T			24121	-	-	9	6
	LOAD			MIN	5.3	5.3	9.5	6
	CLEAR INACTIVE						2.5	1.5
th	20 21		177 C3	MIN	0	0	1	1
tPLH		CLOCK	RIPPLE CARRY	MANY	15.2	15.2	23.5	14
tPHL		CLUCK	RIPPLE CARRY	MAX	15.2	15.2	23.5	14
tPLH		CLOCK	ANNO	MANY	15	15	18.5	11.5
tPHL		CLUCK	ANY Q	MAX	15	15	18.5	11.5
tPLH		FNADIET	RIPPLE CARRY	1444	9.4	9.8	18	11.5
tPHL		ENABLE T	RIPPLE CARRY	MAX	9.4	9.8	18	11.5
		01540	ANYQ	MAX	15	15	19.5	12.5
tPHL.	ds -	CLEAR	RIPPLE CARRY	MAX	15	15	19	12



† For simplicity, routing of complementary signals  $\overline{LD}$  and  $\overline{CK}$  is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

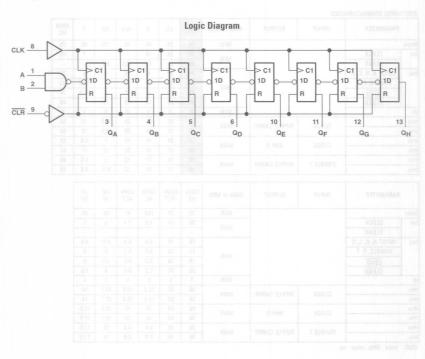
#### SWITCHING CHARACTERISTICS

	PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC
fmax				MIN	25	25	40	40	75	90	25
tw	CLOCK			MIN	25	25	10	- 1	-	7	20
	CLEAR			IVIIN	20	20	10	12.5	6.7	-	-
tsu	INPUT A, B, C, D			10.5	20	20	4	15	8	5	38
	ENABLE, P, T			MIN	20	20	12	15	8	11.5	43
	LOAD			IVIIIN	25	20	.14	15	8	11.5	34
	CLEAR				20	20	14	15	12	-4-	40
th				MIN	0	3	3	0	0	2	0
TPLH	12 13	CLOCK	RIPPLE CARRY	MAX	35	35	25	20	16.5	15	54
tPHL	90	CLUCK	RIPPLE CARRY	IVIAX	35	35	25	20	12.5	15	54
tPLH		CLOCK	ANY O	MAX	25	24	15	15	7	9.5	51
<b>t</b> PHL		CLUCK	AINT U	IVIAA	29	27	15	20	13	11	51
tPLH		CALADIC T	DIDDLE GADDY	MAN	16	14	15	13	9	8.5	49
tPHL		ENABLE T	RIPPLE CARRY	MAX	16	14	15	13	8.5	8.5	49

	PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	LV 3V	LV 5V
fmax				MIN	20	20	103	91	50	85
tw	CLOCK			MINI	24	24	4.8	5.4	5	5
	CLEAR			MIN	-	-	-	-	-	-
tsu	INPUT A, B, C, D				18	15	4.4	4.4	6.5	4.5
	ENABLE, P, T			NAIN!	15	20	4.4	5.3	9	6
	LOAD			MIN	18	18	5.3	6.6	9.5	6
	CLEAR				20	20	5.3	6.6	4	3.5
th				MIN	3	5	0	0	1	1
tPLH		01.001/	DIDDLE GARDY	1447	56	63	15.2	15.2	23.5	14
tPHL.		CLOCK	RIPPLE CARRY	MAX	56	63	15.2	15.2	23.5	14
<b>TPLH</b>		01004	AAUV O		56	59	15	15	18.5	11.5
tPHL.		CLOCK	ANY Q	MAX	56	59	15	15	18.5	11.5
tPLH		FNIADLET	DIDDLE GADDV	MAN	36	48	9.4	9.8	18	11.5
tPHL		ENABLE T	RIPPLE CARRY	MAX	36	48	9.4	9.8	18	11.5

#### 8-BIT PARALLEL OUT SERIAL SHIFT REGISTERS

- AND-Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs



	INPUTS				OUTPL	JTS
CLEAR	CLOCK	Α	В	QA	QB	QH
L	X	X	X	L	L	L
H	L	×	X	QAO	QBO	QHO
H	1	H	H	H	QAn	QGr
Н	1	L	X	L	QAn	QGr
H	1	×	1	L	OAn	000

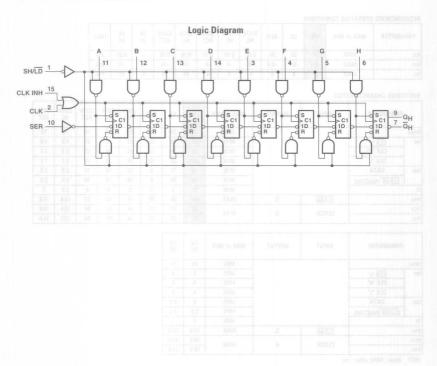
#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	LV 3V	LV 5V	UNIT
lcc	MAX	54	27	24	0.08	0.16	0.16	0.16	0.16	- 0	0.02	mA
Іон	MAX	-0.4	-0.4	-0.4	-4	-4	-4	-24	-24	-6	-12	mA
lor	MAX	8	8	8	4	4	4	24	24	6	12	mA

#### CIANTOLINA CHADACTERICTICS

24411	CHING CHARACTERIS	1165								Y		
	PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
fmax	35-11	Rip.	86- 10	MIN	25	25	50	25	20	18	75	70
tw	CLR "L"			MIN	20	20	16	25	18	27	4.5	4.5
	CLK "H"			MIN	20	20	10	20	24	27	6.7	7.1
	CLK "L"			MIN	20	20	10	20	24	27	6.7	7.1
tsu	DATA			MIN	15	15	6	25	18	18	2.5	2.5
	CLEAR INACTIVE			MIN	20	20	8	25	18	18	2.5	2.5
th				MIN	5	5	2	5	4	4	2.5	3
tPHL		CLEAR	Q	MAX	42	36	20	51	42	57	13.9	15.8
tPLH		CLOCK	0	MANY	30	27	16	44	51	54	12.5	14.9
tPHL		CLUCK	۵	MAX	37	32	17	44	51	54	12.5	14.9

	PARAMETER	INPUT	OUTPUT	MAX or MIN	LV 3V	LV 5V
fmax			1	MIN	45	75
tw	CLR "L"			MIN	5	5
	CLK "H"			MIN	5	5
	CLK "L"			MIN	5	5
tsu	DATA			MIN	6	4.5
	CLEAR INACTIVE			MIN	2.5	2.5
th				MIN	0	1
tPHL.		CLEAR	0	MAX	18.5	12.5
tPLH		CLOCK	Q	MAX	18.5	12.5
tPHL		CLUCK	u	WAX	18.5	12.5



		INPUTS			INTE	RNAL	OUTPUT
SHIFT/	CLOCK	01.001/	OFFILE	PARALLEL	OUT	PUTS	OUTFUT
LOAD	INHIBIT	CLOCK	SERIAL	AH	QA	QB	QH
L	X	X	X	ah	а	b	h
H	L	L	X	X	QAO	Q <sub>B0</sub>	QHO
H	L	1	H	X	Н	QAn	QGn
H	L	1	L	X	L	QAn	QGn
H	Н	X	X	X	QAO	QBO	QHO

RECOMMENDED OPERATING CONDITIONS

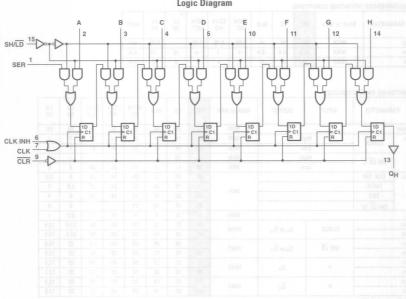
TIEGOTHINETEDED	OI LINATING GOIL	DITTOTAL			_	_	-	_	_	
PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	TA TA	5 LV	UNIT
Icc	MAX	63	30	24	0.08	0.16	0.16	-	0.02	mA
Тон	MAX	-0.8	-0.4	-0.4	-4	-4	-4	-6	-12	mA
lou.	MAX	16	8	8	4	4	4	6	12	mA

SWIT	CHING CHARACT	TERISTICS	plan	pl-sh	14		1		1-1		ph-h	
P/	ARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V
fmax		4.97	7 07	MIN	20	25	45	25	20	18	50	85
tw	OI DON	H	igh	MIN	25	15	11	20	24	27	7	4
	CLOCK	L	ow	MIN	25	25	11	20	24	27	7	4
	SH/ LD "L"	Н	igh	MIN	15	25	-	-	-	-	-	3
	SH/ LD L	L	ow	MIN	15	17	12	20	24	30	9	6
tsu	CLK INH				30	30	11	25	24	30	5	3.5
	DATA			MIN	10	10	10	25	24	30	8.5	5
	SER			IVIIIN	20	20	10	10	24	30	6	4
	SH/ LD "H"				45	45	10	20		-	6	4
th				MIN	0	0	4	5	.11	11	0.5	1
tPLH .		CLOCK	0 0	MAX	24	25	13	38	50	60	21.5	13.5
tPHL		CLUCK	$Q_H$ or $\overline{Q}_H$	IVIAA	31	25	14	38	50	60	21.5	13.5
tPLH		SH/ LD	0 5	MAX	31	35	20	38	53	60	22	13.5
tPHL.		SH/ LU	Q <sub>H</sub> or Q <sub>H</sub>	IVIAA	40	35	22	38	53	60	22	13.5
tPLH		Н	0	MAX	17	25	13	38	45	53	20	12.5
tPHL		п	QH	IVIAX	36	30	16	38	45	53	20	12.5
tPLH	н		Q <sub>H</sub>	MAX	27	30	15	38	45	53	20	12.5
tPHL		ri	Q <sub>H</sub>	IVIAX	27	25	16	38	45	53	20	12.5

#### **8-BIT SHIFT REGISTERS**

- Synchronous Load
- Direct Overriding Clear
- Parallel-to-Serial Conversion

# Logic Diagram



		1	NPUTS			INTE	RNAL	OUTPUT		
	SHIFT/	CLOCK			PARALLEL C		OUTPUTS		OUTPUTS	
CLEAR	LOAD	INHIBIT	CLOCK	SERIAL	AH	QA	QB	QH		
L	X	X	X	X	X	L	L	L		
H	X	L	L	X	X	QAO	Q <sub>B0</sub>	QHO		
H	L	L	1	X	ah	a	b	h		
H	H	L	1	H	X	H	QAn	QGn		
H	H	L	1	L	X	L	QAn	QGn		
H	X	Н	1	X	X	QAO	Q <sub>B</sub> 0	QHO		

4-BIT UP/DOWN SYNCHRONOUS O

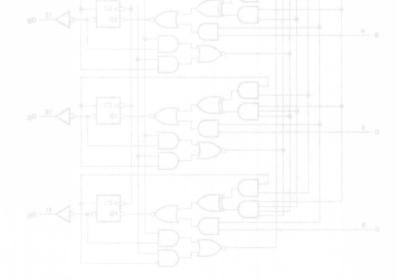
Fully Synchronous Operation for Countin
 Internal Carry Look-Ahead Circuitry for E
 Carry Output for a Pic Secondary

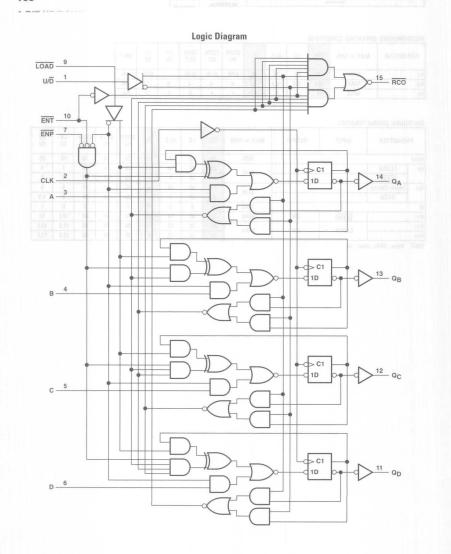
RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	F	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
Icc	MAX	127	32	24	60	0.08	0.16	0.16	-	0.02	mA
Іон Остан	MAX	-0.8	-0.4	-0.4	-1	-4	-4	-4	-6	-12	mA
lou	MAX	16	8	8	20	4	4	4	6	12	mA

SWITCHING CHARACTERISTICS

SWIT	CHING CHARAC	TERISTICS								V	-		1148
Р	ARAMETER	INPUT	OUTPUT	MAX or MIN	ΠL	LS	ALS	F	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V
fmax				MIN	25	25	45	110	25	20	16	50	85
tw	CLOCK		0 < 0 - 6	MIN	20	20	10	3.5	20	24	30	7	4
	CLEAR	The land	01 5	MIN	20	25	9	4	25	30	53	7	5
tsu	Mode Control	A III		MIN	30	30	16	4	36	44	45	6	4
	DATA			IVIII	20	20	7	3	20	24	24	6	4.5
th				MIN	0	0	3	0	0	1	0	0	1
tPHL		CLEAR	ΩН	MAX	35	30	14	9.5	30	48	60	18.5	12
tPHL	PHL CLOCK QH		MAN	30	25	13	14	38	48	60	21.5	13.5	
tPLH			MAX	26	20	12	9	38	48	60	21.5	13.5	





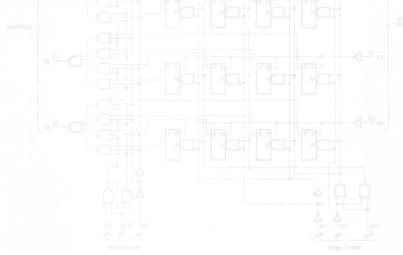
RECOMMENDED	OPERATING	CONDITIONS	
DADAMETED		MAY or MIN	10

HEOOMHILLIAN	20 01 210111110 01		_		_	_	_	_
PARAMETER	R	MAX or MIN	LS	S	ALS	AS	F	UNIT
Icc		MAX	45	160	25	63	52	mA
	RCO	MAX	-0.4	-1	-0.4	-2	nia e	mA
ЮН	Q	MAX	-1.2	-1	-0.4	-2	-1	mA
Іон ВСС	RCO	MAX	8	20	8	20	20	mA
	Q	MAX	24	20	8	20	20	mA

 Fast Access Times: Typically 20ng Expandable to 1024 Words of 4 Bit

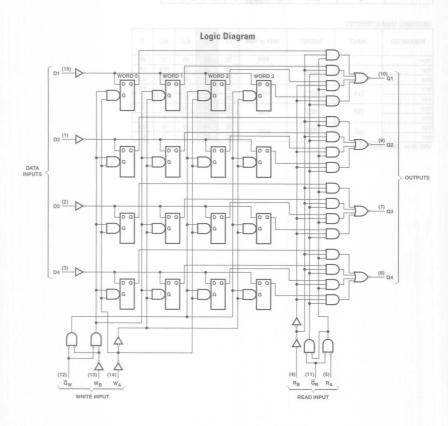
#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F
fmax			MIN	20	40	40	75	90
tPLH	CLK	RCO	MAY	40	21	20	16.5	17
tPHL ID	CLK	nco	MAX	25	28	20	13	12.5
tPLH	0114	4400	1111	25	15	15	13	9.5
tPHL .	CLK	ANY Q	MAX	25	15	20	7	13
tPLH	ENT	RCO	MAN	25	12	13	9	7
tphl.	ENT	RUU	MAX	20	25	16	9	9
tPLH	U/D	RCO	MAX	35	15	19	12	12.5
tPHL .	0/0	KLU	MAX	25	22	19	13	12



#### **4-BY-4 REGISTER FILES**

- Separate Read/Write Addressing Permits Simultaneous Reading and Writing
- Fast Access Times: Typically 20ns
- Expandable to 1024 Words of 4 Bits



#### WRITE FUNCTION TABLE

WRI	WRITE INPUTS		INPUTS OUTPUTS			
WB	WA	G <sub>W</sub>	0	1	2	3
L	L	L	Q = D	00	QO	00
L	Н	L	00	Q = D	00	00
H	L	L	00	90	Q = D	00
H	Н	L	90	00	QO	Q = D
X	×	Н	90	90	90	00

#### READ FUNCTION TABLE

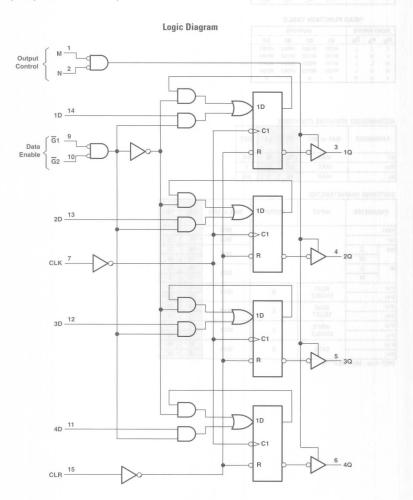
RE/	D INP	UTS		OUT	PUTS	
RB	RA	GR	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	Н	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
Н	Н	L	W3B1	W3B2	W3B3	W3B4
X	×	Н	H	H	H	Н

#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
Icc	MAX	150	40	mA
Vон	MAX	5.5	5.5	V
lou	MAX	16	8	mA

#### SWITCHING CHARACTERISTICS

300110	JIING CHAI	RACTERISTICS				
PAR	RAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
fmax			10<	MIN	3	
tw		-		MIN	25	25
tsu	D	8 19		NAINI	10	10
	W	- O		MIN	15	15
th	D	-		NAINI	15	15
	W			MIN	5	5
tPLH .		READ	0	MAX	15	30
<b>TPHL</b>		ENABLE	u	IVIAX	30	30
tPLH		READ	Ω	MAX	35	40
tPHL.		SELECT	u ar	MAX	40	40
tPLH		WRITE	0	MAX	40	45
tPHL		ENABLE	u	IVIAX	45	40
tPLH.		DATA	0	MAN	30	45
tPHL .		DATA	0	MAX	45	35



	INPUTS  LEAR CLOCK DATA ENABLE DATA  G1 G2  D							
CLEAR	CLOCK	DATA	ENABLE	DATA	OUTPUT			
		G1	G2	D				
H	X	X	×	X	L			
L	L	X	X	X	90			
L	1	H	×	X	90			
L	1	X	Н	X	QO			
L	1	L.	L	L	L			
L	1	L	L	H	H			

HEX D-TYPE FLIP-FLOPS

Buffered Cleak and Disease Class

Fully Buffered Dutauts for Maximum leadation

from External Disturbences

#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
lcc	MAX	72	24	0.08	0.16	0.16	mA
Іон	MAX	-5.2	-2.6	-6	-6	-6	mA
lou	MAX	16	24	6	6	6	mA

#### SWITCHING CHARACTERISTICS

1	PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
fmax			Am   810   81	MIN	25	25	25 25	20	13
tvv				MIN	20	25	20	24	28
tsu	DATA ENABLE			20 05	17	35	25	18	18
	DATA			MIN	10	17	25	18	27
	CLR INACTIVE			MIN	10	10	23	don	100
th	DATA ENABLE			TONG VS	2	0	0	0	0
	DATA			MIN	10	3	0	3	0
tPHL	•	CLEAR	۵	MAX	27	35	38	53	66
tPLH		CLOCK	0	MANY	43	25	38	60	60
tPHL		CLOCK	u	MAX	31	30	38	60	60
tPZH		FALABLE	Q	MAN	30	23	38	45	45
tPZL		ENABLE	и	MAX	30	27	38	45	45
tPHZ	senn senn s	DICABLE	0	1447	14	20	38	45	
tPLZ	T394 398	DISABLE	Ω	MAX	20	17	38	45	

 · · · · · · · · · · · · · · · · · · ·	THE LET US						

# 174

# **HEX D-TYPE FLIP-FLOPS**

- Buffered Clock and Direct Clear Inputs
- Fully Buffered Outputs for Maximum Isolation from External Disturbances

#### **FUNCTION TABLE**

	INPUTS		OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	1	Н	H
H	1	L	L
L	L	X	00

# CLR 1 1D 1D 1D

To Five Other Channels

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	UNIT
Icc	MAX	65	26	144	19	45	55	0.08	0.16	0.16	mA
Іон	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-4	-4	-4	mA
lou	MAX	16	8	20	8	20	20	4	4	4	mA

PARAMETER	MAX or MIN	CD74 AC	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	UNIT
Icc	MAX	0.16	0.16	0.04	0.04		0.02	mA
Іон	MAX	-24	-24	-8	-8	-6	-12	mA
lou	MAX	24	24	8	8	6	12	mA

SWITCHING CHARACTERISTICS

F	PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC
fmax				MIN	25	30	75	50	100	80	25	20	17	95
tw	CLR LOW			MIN	20	20	10	10	5	5	20	24	38	4
	CLK HIGH			MIN	20	20	7	10	4	4	20	24	30	5.2
	CLK LOW			IVIIIV	20	20	7	10	6	6	20	24	30	5.2
tsu	DATA INPUT			MIN	20	20	5	10	4	4.5	25	18	24	2
	CLR INACTIVE			MIN	25	25	5	6	6	5	25	-	-	-
th				MIN	5	5	3	0	1	1	0	5	5	3
tPLH		CLR	ANY Q	MAX	25	-	-	18		-	40	45	66	14.5
TPHL		ULH	ANYU	IVIAX	35	35	22	23	14	15	40	45	66	14.5
tPLH		01.14	ANY Q	MAN	30	30	12	15	8	9	40	50	60	13.5
<b>t</b> PHL		CLK	ANYU	MAX	35	30	17	17	10	11	40	50	60	13.5

1	PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 ACT	AHC	AHCT	SV TV	LV 5V
fmax				MIN	80	80	65	50	80
tw.	CLR LOW			MIN	4	5	5	5	5
	CLK HIGH			24121	6.2	5	5	5	5
	CLK LOW			MIN	6.2	5	5	5	5
tsu	DATA INPUT			MIN	2	4.5	5	6	4.5
	CLR INACTIVE			MIN	-	2.5	3.5	3	2.5
th				MIN	2.5	0.5	0	0	0.5
tPLH		01.0	ANIVO	MANY	15.5	-	-	17	11
tPHL		CLR	ANY Q	MAX	15.5	11	13	17	11
tPLH		OL IV	4100	1111	14	10.5	10	16.5	10.5
tPHL		CLK	ANY Q	MAX	14	10.5	10	16.5	10.5

#### QUAD D-TYPE FLIP-FLOPS

- Complementary Outputs (Q, Q)
   Buffered Clock and Direct Clear Inputs
- Asynchronous Clear Function

# 1D -

Logic Diagram

#### **FUNCTION TABLE**

	INPUTS					
CLEAR	CLOCK	D	Q	Q		
L	X	X	L	Н		
H	1	H	H	L		
H	1	L	L	H		
H	4 11	X	90	Qn		

To Three Other Channels

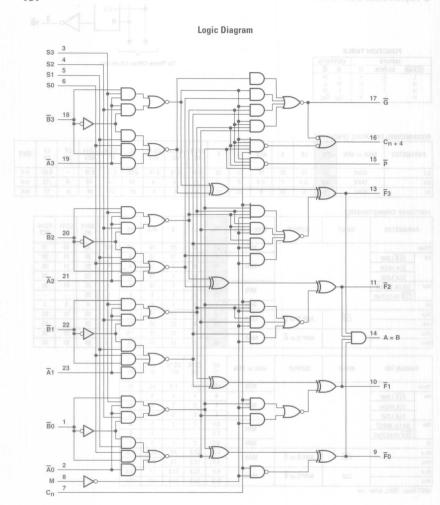
#### RECOMMENDED OPERATING CONDITIONS

9 4 11					1.76											
PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	CD74 AC	CD74 ACT	LV 3V	LV 5V	UNIT
lcc	MAX	45	18	96	14	34	34	0.04	0.16	0.16	0.08	0.16	0.16	-	0.02	mA
Гон	MAX	-0.8	-0.4	-1	-0.4	-2	-1-	-4	-4	-4	-24	-24	-24	-6	-12	mA
lou g	MAX	16	8	20	8	20	20	4	- 4	4	24	24	24	6	12	mA

#### SWITCHING CHARACTERISTICS

SVVII	CHING CHARACTE	HISTICS		1 119			_	-					
1	PARAMETER	INPUT	OUTPUT	MAX or MIN	ΠL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT
fmax				MIN	25	30	75	50	100	100	25	20	16
tw	CLR LOW				20	20	10	10	5	5	20	24	30
	CLK HIGH			MIN	20	20	7	10	4	4	20	24	30
	CLK LOW				20	20	7	10	5	5	20	24	30
tsu	DATA INPUT	(1		MIN	20	20	5	10	3	3	25	24	30
	CLR INACTIVE			IVITIV		25	5	6	6	5	25	-	-
th				MIN	5	5	3	0	-(1	-1	0	5	5
tPLH		CLR	ANY Q or Q	MAX	25	30	15	18	9	9	38	53	53
tPHL.		CLR	ANT U OF U	IVIAX	35	30	22	23	13	13	38	53	53
tPLH	11	CIV	ANV 0 0	MAN	30	25	12	15	7.5	7.5	38	53	50
<b>t</b> PHL		CLK	ANY Q or Q	MAX	35	25	17	17	10	9.5	38	53	50

F	PARAMETER	INPUT	OUTPUT	MAX or MIN	AC 11	CD74 AC	CD74 ACT	LV 3V	LV 5V	
fmax	19 01		(()	MIN	125	100	114	45	75	
tw	CLR LOW				4	4	4	5	5	
	CLK HIGH			MIN	4	5	5	5	5	
	CLK LOW				4	5	5	5	5	
tsu	DATA INPUT			MIN	5.5	2	2	5	4	
	CLR INACTIVE			IVIIIV	5.5	-	¥.	5	5	
th				MIN	0.5	2	2	1	- 1	
tPLH	0 0	CLR	ANY Q or Q	MAX	6.8	12.2	13	15.5	9.5	
<b>TPHL</b>		CEN	AINT U OF U	IVIAX	9.3	12.2	13	15.5	9.5	
tPLH		CLK	ANY Q or Q	MAX	6.9	12.2	11.5	17	10.5	
<b>TPHL</b>		ULK	AINT COLC	WAX	93	12.2	11.5	17	10.5	



#### FUNCTION TABLE (ACTIVE LOW)

SELECTIO			ACTIVE-LOW	DATA				
SELECTIO	IN .	M = L; ARITHMETIC OPERATIONS						
S3 S2 S1	SO F	LOGIC	Cn = L (no carry)	Cn = H (with carry)				
LLL	LF	- Ā	F = A MINUS 1	F = A				
LLL	H F	= AB	F = AB MINUS 1	F = AB				
LLH	L F	= A + B	F = AB MINUS 1	F = AB				
LLH	H F	=1	F = MINUS 1(2's COMP)	F = 0				
LHL	LF	= A + B	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1				
LHL		= B	F = AB PLUS (A + B)	F = AB PLUS (A + B) PLUS 1				
LHH	LF	- A @ B	F = A MINUS B MINUS 1	F = A MINUS B				
LHH	HF	= A + B	F = A + B	F = (A + B) PLUS 1				
HLL	LF	= AB	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1				
HLL	H F	= A ⊕ B	F = A PLUS B	F = A PLUS B PLUS 1				
HLH	LF	= B	F = AB PLUS (A + B)	F = AB PLUS (A + B) PLUS 1				
H L H	H F	= A + B	F = (A + B)	F = (A + B) PLUS 1				
HHL	L F	= 0	F = A PLUS A*	F = A PLUS A PLUS 1				
H H L	H F	= AB	F = AB PLUS A	F = AB PLUS A PLUS 1				
ннн	LF	= AB	F = AB PLUS A	F = AB PLUS A PLUS 1				
21 22 22	11 6		F . A	F ADULE 1				

#### FUNCTION TABLE (ACTIVE HIGH)

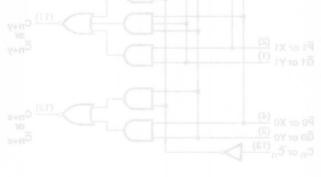
SELECTION		ACTIVE-HIGH DATA						
SELECTION	M = H	M = L; ARITHMETIC OPERATIONS						
S3 S2 S1 S0	LOGIC	Cn = H (no carry)	Cn = L (with carry)					
LLLL	F = A	F = A	F = A PLUS 1					
LLLH	F = A + B	F = A + B	F = (A + B) PLUS 1					
LLHL	F = AB	$F = A + \overline{B}$	$F = (A + \overline{B}) PLUS 1$					
LLHH	F = 0	F = MINUS 1(2's COMPL)	F = 0					
LHLL	F = AB	F = A PLUS AB	F = A PLUS AB PLUS 1					
LHLH	$F = \widetilde{B}$	F = (A + B) PLUS AB	F = (A + B) PLUS AB PLUS 1					
LHHL	F=A@B	F = A MINUS B MINUS 1	F = A MINUS B					
LHHH	F = AB	F = AB MINUS 1	F = AB					
HLLL	$F = \widetilde{A} + B$	F = A PLUS AB	F = A PLUS AB PLUS 1					
HLLH	F = A $\oplus$ B	F = A PLUS B	F = A PLUS B PLUS 1					
HLHL	F = B	$F = (A + \overline{B}) PLUS AB$	F = (A + B) PLUS AB PLUS 1					
HLHH	F = AB	F = AB MINUS 1	F = AB					
HHLL	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1					
HHLH	$F = A + \overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1					
HHHL	F = A + B	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1					
0 0 0 0	E A	E - A MINITE 1	E - A					

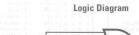
#### RECOMMENDED OPERATING CONDITIONS

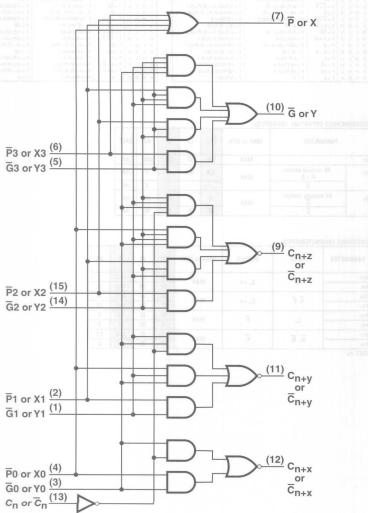
112001111		1				10	_
	PARAMETER	MAX or MIN	TTL	LS	S	AS	UNIT
Icc		MAX	150	37	220	200	mA
Іон	All outputs except A = B	MAX	-0.8	-0.4	-1	-2	mA
	G			-	-	-3	mA
lor	All outputs except	MAX	16	8	20	20	mA
	G		16	8	20	48	mA

SWITCHING CHAP	RACTERISTICS					1	-
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	AS
tPLH	X+C <sub>n</sub>	0	MAX	18	27	10.5	9
tphL .	C <sub>n</sub>	C <sub>n</sub> +4	WAX	19	20	10.5	9
tplh	Ā, B	0.1	MAX	43	38	18.5	12
tPHL .	А, В	C <sub>n</sub> +4	WAX	41	38	18.5	12
tPLH .		Ē	MAN	19	26	12	9
tphl.	Cn	F	MAX	18	20	12	9
tPLH.	$\overline{A}_i, \overline{B}_i$	F <sub>i</sub>	MAN	42	32	16.5	9.5
tPHL .	A <sub>i</sub> , B <sub>i</sub>	F <sub>i</sub>	MAX	32	20	16.5	8

#### UNIT: ns







OUTPUT

#### 0

	INP	UTS	3
P3	P2	P1	PO
L	L	L	L

#### Cn+x OUTPUTS

	INPL	JTS	OUTPUT
GO	Po	Cn	C <sub>n+x</sub>
L	X	X	Н
X	L	H	H
	II oth		L

		IN	PUT	rs			OUTPUT
Ğ3	Ğ2	Ğ1	P3	P2	P1	P0	G
L	X	X	X	Χ	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
7	All of	her	com	bina	ation	s	H

C-+V OUTDUTS

	Un-	-у ч	20	IPU	15
	IN	OUTPUT			
G1	G0	P1	P0	Cn	Cn+y
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	Н	H
	Al	loth			L

Cn+z OUTPUTS

		IN	PU'	TS		-	OUTPUT
32	G1	G0	P2	P1	P0	Cn	C <sub>n+z</sub>
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	V H
A	II ot	her	con	bin	ation	าร	L

RECOMMENDED OPERATING CONDITIONS

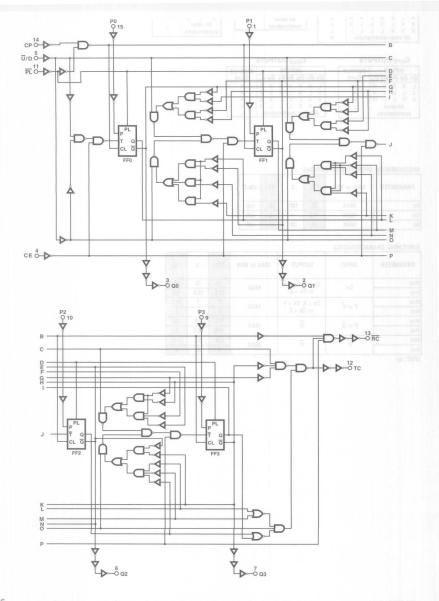
PARAMETER	MAX or MIN	TTL	S	AS	UNIT
Icc	MAX	72	109	36	mA
Іон э	MAX	-0.8	-1	-2	mA
lou	MAX	16	20	20	mA

SWITCHING CHARACTERISTICS

SWITCHING CHAN	ACTENISTICS			1		
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	S	AS
tplH	C-	Cn + X, Cn + Y	MAX	10	10	10
tPHL .	Cn	or Cn + Z	IVIAA	10.5	10.5	9.5
tPLH .	P or G	Cn + X, Cn + Y or Cn + Z MAX	MANY	7	7	10.5
tPHL .			IVIAA	7	7	6
tPLH .	P or G	G	MAX	7.5	7.5	12
tphL .	Poru	U	IVIAX	10.5	10.5	8
tPLH .	P	P	MAN	6.5	6.5	7.5
tPHL .	P	P	MAX	10	10	6

UNIT: ns



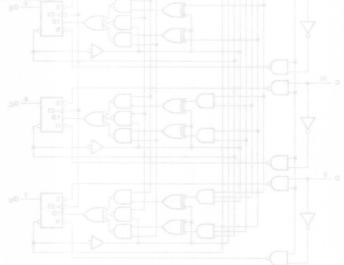


#### RECOMMENDED OPERATING CONDITIONS

TILOUIVIIVILIADE	D OI LIMING	CONTENT	10110				
PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	UNIT
Icc	MAX	105	35	22	0.08	0.16	mA
Іон	MAX	-0.8	-0.4	-0.4	-4	4	mA
Inc	MAX	16	8	8	4	4	mA

#### SWITCHING CHARACTERISTICS

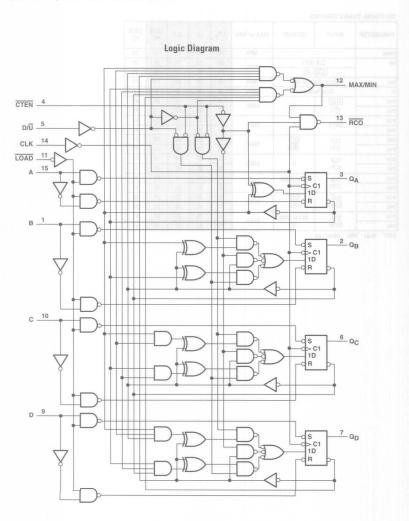
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC
fmax			MIN	20	20	25	17	25
tw	CLK (CP)			25	25	20	30	20
	LOA	D (PL)	MIN	35	35	20	30	25
tsu	Data , high or low		MIN	20	20	20	38	15
th	Data hold time		MIN	0	5	5	5	2
tPLH .	LOAD (PL)	0	MAX	33	33	30	66	49
tphl.		u		50	50	30	66	49
tPLH O	DATA	0	MAY	22	32	21	60	44
tphL .		-u	MAX	50	40	21	60	44
tPLH	CLK (CP)	RCO	MAX	20	20	20	30	31
tPHL .		(RC)	IVIAX	24	24	20	30	31
tPLH	CLK	Q	MAX	24	24	18	48	43
tPHL	(CP)	u	MAX	36	36	18	48	43
tPLH	CLK	MAX/MIN	MAX	42	42	31	63	53
tPHL	(CP)	(TC)	MAX	52	52	31	63	53
tPLH	D/Ū	D/Ū RCO (RC)	MAX	45	45	37	57	38
tPHL				45	45	28	57	38
tplH	D/Ū (Ū/D)	MAX/ MIN	/	33	33	25	48	41
tphl.		(TC)	MAX	33	33	25	48	41



## 191

### SYNCHRONOUS UP/DOWN COUNTERS

- Count Enable Control Input
- Ripple Clock Output for Cascading
- Asynchronously Presentable with Load Control



### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	UNIT
lcc	MAX	105	35	22	0.08	0.16	0.16	mA
Іон	MAX	-0.8	-0.4	-0.4	-4	-4	-4	mA
lor.	MAX	16	8	8	4	4	4	mA

#### SWITCHING CHARACTERISTIC

SWIT	CHING CHA	RACTERISTICS	,	11183	20114	HARM	,			
PAI	RAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT
fmax		(5) (M)		MIN	20	20	30	17	25	25
tw	CLK			MIN	25	25	16.5	30	20	20
	LOAD			IVIIIV	35	35	20	30	25	25
tsu	DATA			MIN	20	20	20	38	15	15
th	DATA			MIN	0	5	5	5	2	2
tPLH	AO TUS	LOAD	QA, QB	MAX	33	33	30	66	49	50
tPHL		LUAD	QC, QD	IVIAX	50	50	30	66	49	50
tPLH		DATA	QA, QB	MAX	22	32	21	60	44	48
tPHL		A, B, C, D	QC, QD	IVIAA	50	40	21	60	44	48
tPLH		CLK	RIPPLE	MAX	20	20	20	30	31	34
tPHL		CLK	CLK	IVIAA	24	24	20	30	31	34
tPLH		CLK	QA, QB	MAX	24	24	18	48	43	44
tPHL		CLK	QC, QD	IVIAX	36	36	18	48	43	44
tPLH		CLK	MAX or MIN	MAX	42	42	31	63	53	53
tPHL	- of the		IVIAX OF IVIIIN	IVIAX	52	52	31	63	53	53
tPLH .		D/Ū	RIPPLE	MAX	45	45	37	57	38	38
tPHL		0/0	CLK	IVIAX	45	45	28	57	38	38
tPLH		D/U	MAN MINI	MAN	33	33	25	48	41	48
tPHL		D/U	MAX or MIN	MAX	33	33	25	48	41	48

UNIT fmax : MHz, other : ns

# Logic Diagram (13) BO (12) CO DATA (15) DOWN (4) (3) OUTPUT QA DATA (1) INPUT B S DATA (10) S (6) OUTPUT QC DATA (9) CLR (14) (7) OUTPUT QD LOAD (11)

CLOCK UP	CLOCK	RESET	PARALLEL LOAD	FANCTION
1	Н	L	Н	Count Up
Н	1	L	Н	Count Down
Х	X	Н	X	Reset
Х	Х	L	L	Load Preset inputs

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care, ↑ = Transition from Low to High Level

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
Icc	MAX	0.16	mA
Іон	MAX	-4	mA
lou	MAX	4	mA

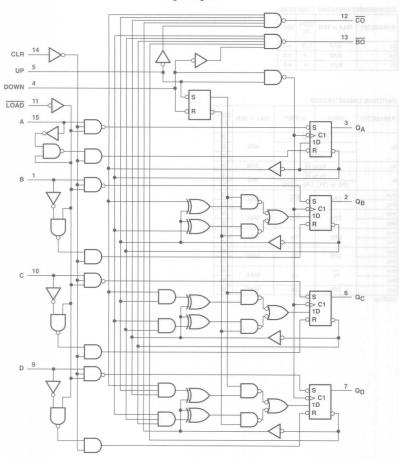
#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
	CPU	, CPD		35
tw		PL	MIN	24
	MR		30	
tsu	Pn	to PL	MIN	24
	Pn	PL MIN		0
th	CPD to CPU	, CPD to CPU	IVIIN	24
tPLH	CPU	TCU	MAX	38
tphl	CPU	100	MAX	38
tPLH .	CPD	TCD	MAX	38
tphl.	CPD	I CD	IVIAX	38
tPLH .	CPD	0-	MAN	65
tphl .	CPD	Qn	MAX	65
tplh	CPD	Qn	MAX	65
tphl .	CPD	un	IVIAX	65
tplH	PL	0-	MAN	66
tPHL	rL.	Qn	MAX	66
tPHL	MR	Qn	MAX	60

### SYNCHRONOUS UP/DOWN DUAL CLOCKCOUNTERS

- Parallel Asynchronous Load for Modulo-N Count Lengths
- Asynchronous Clear

## Logic Diagram

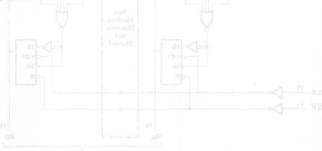


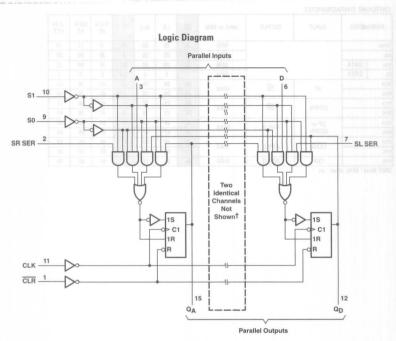
HECOMINIENDED	OI LIMITING CON	DITION	,						
PARAMETER	MAX or MIN	TTL	LS	ALS	F	SN74 HC	CD74 HC	CD74 HCT	UNIT
Icc	MAX	102	34	22	54	0.08	0.16	0.16	mA
Іон	MAX	-0.4	-0.4	-0.4	-1	-4	-4	-4	mA
lou	MAX	16	8	8	20	4	4	4	mA

SWITCHING CHARACTERISTICS

	AMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	F	SN74 HC	CD74 HC	CD74 HCT
fmax				MIN	25	25	30	85	17	17	15
tw				MIN	20	20	20	4	30	30	35
tsu	DATA			MIN	20	20	20	3.5	28	24	22
th	DATA			MIN	0	5	5	2.5	5	0	0
tPLH		LID	8 <u>co</u>	MAY	26	26	16	9	41	38	41
tPHL		UP	CO	MAX	24	24	18	9	41	38	41
tPLH		DOWN	80	MAX	24	24	16	9	41	38	41
tPHL .		DUVVIN	ВО	IVIAX	24	24	18	9	41	38	41
tPLH		UP or	ANY Q	MAX	38	38	19	9	63	65	60
tPHL		DOWN	ANYU	IVIAX	47	47	17	13	63	65	60
tPLH	198.18	LOAD	ANY Q	MAN	40	40	30	11	65	66	69
tPHL		LUAD	ANYU	MAX	40	40	28	13	65	66	69
tPHL.		CLR	ANY Q	MAX	35	35	17	12	60	60	65

UNIT fmax : MHz, other : ns





† I/O ports not shown: QB (14) and QC (13)

	UTS	OUTF	- (						NPUTS	11			
0-	00	0=	QA	L	LLE	ARA	P	RIAL	SEF	CLOCK	DE	MO	CLEAR
чD	QC	αB	чA	D	C	В	Α	RIGHT	LEFT	CLUCK	SO	S1	LEAR
L	L	L	L	X	X	X	X	X	X	X	X	X	L
Q <sub>D0</sub>	QCO	Q <sub>B</sub> 0	QAO	X	X	X	X	X	X	L	X	X	H
d	C	b	a	d	C	b	a	X	X	1	H	Н	H
QCn	QBn	QAn	H	X	X	X	X	H	X	1	H	L	H
	QBn		L	X	X	X	X	L	X	1	H	L	Н
H		Qcn	QBn	X	X	X	X	X	H	1	L	Н	Н
L				X	X	X	X	X	L	1	L	H	Н
QDO		Q <sub>B</sub> 0		X	X	X	X	X	X	X	L	L	H

#### RECOMMENDED OPERATING CONDITIONS

NECOMMENDED	OF ENATING CON	DITION	,						
PARAMETER	MAX or MIN	TTL	LS	S	AS	SN74 HC	CD74 HC	CD74 HCT	UNIT
Icc	MAX	63	23	135	53	0.1	0.16	0.16	mA
Іон	MAX	-0.8	-0.4	-1	-2	-4	-4	-4	mA
lo <sub>L</sub>	MAX	16	8	20	20	4	4	4	mA

### SWITCHING CHARACTERISTICS

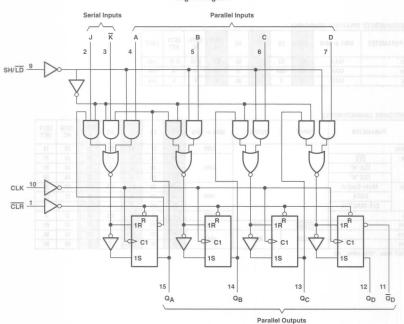
	PARAMETER	INPUT	ОИТРИТ	MAX or MIN	TTL	LS	S	AS	SN74 HC	CD74 HC	CD74 HCT
fmax				MIN	25	25	70	80	25	20	18
tw	CLR				20	20	12	4.5	20	24	24
	CLK "H"			MIN	20	20	7	4	20	24	24
	CLK "H"				20	20	7	7	20	24	24
tsu	Mode Control			-	30	30	11	9.5	25	24	30
	DATA			MIN	20	20	5	4	25	21	21
	CLR INACTIVE			-	25	25	9	6			C-
th	g			MIN	0	0	3	0.5	0	0	0
tPHL	- G 81	CLEAR	ANY	MAX	30	30	18.5	12	38	42	60
tPLH			4 4 104	1111	22	22	12	7	36	53	56
tPHL	12/45	CLOCK	ANY	MAX	28	26	16.5	7/	36	53	56

UNIT fmax : MHz, other : n

### **4-BIT PARALLEL-ACCESS SHIFT REGISTERS**

- Direct Overriding Clear
- Parallel-to-Serial, Serial-to-Parallel Conversions

### Logic Diagram



	INPUTS								OUTPUTS					
CLEAR	SHIFT/	CLOCK	SEF	RIAL	PA	AR/	LLI	EL	QA	QR	QC	QD	Ōρ	
OLLAII	LOAD		J	ĸ	A	В	С	D	-	-		_	_	
L	X	X	X	X	X	X	X	X	L	L	L	L	Н	
H	L	1	X	X	a	b	C	d	a	b	C	d	d	
H	Н	L	X	X	X	X	X	X	QAO	Q <sub>B0</sub>	QCO	Q <sub>D0</sub>	QDO	
H	H	1	L	H	X	X	X	X	QAO			QCn		
H	H	1	L	L	X	X	X	X	L			QCn		
H	H	1	H	H	X	X	X	X	Н	QAn	QBn	QCn	Qcn	
Н	Н	1	Н	L	X	X	X	X	QAn			QCn		

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	AS	SN74 HC	CD74 HC	UNIT
lcc	MAX	63	21	109	57	0.1	0.16	mA
Іон	MAX	-0.8	-0.4	-1	-2	-4	-4	mA
lou	MAX	16	8	20	20	4	4	mA

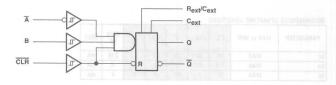
### SWITCHING CHARACTERISTICS

	PARAMETER	INPUT	ОИТРИТ	MAX or MIN	TTL	LS	S	AS	SN74 HC	CD74 HC
fmax				MIN	30	30	70	70	25	20
tw	CLOCK			MIN	16	16	7	4	20	24
	CLEAR			IVIIIV	12	12	12	7.2	20	24
tsu	Shift / Load				25	25	11	8	25	30
	Serial & Pararel Data			MIN	20	15	5	3.5	25	30
	Clear Inactive Data				25	25	9	6	25	30
TRELE	ASE			MAX	10	20	6		NE.	-
th				MIN	0	0	3	1	0	
tPHL		CLEAR		MAX	30	30	18.5	11.5	38	45
tPLH		CLOCK	QA, QD	MAX	22	22	12	8.5	36	53
tPHL.		CLUCK		WAX	26	26	16.5	10.5	36	53

Overriding Clear Terminates Outputs Pulse

UNIT fmax : MHz, other : ns

### Logic Diagram



INF	UTS		OUT	PUTS
CLEAR	A	В	Q	Q
L	X	X	L	Н
X	H	X	Lt	H†
X	X	L	Lt	H†
H	L	1	л	T
H	1	H	17	7.5
4	1 1	L		7.5

See explanation of function table on page
† These lines of the functional tables assume that the indicated
steady-state conditions at the A and B inputs have been
set up long enough to complete any pulse started before the set up.

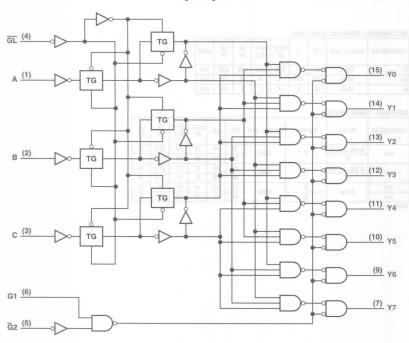
#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ΠL	LS	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
lcc	MAX	80	27	0.16	0.16	0.28	0.65	mA
Іон	MAX	-0.8	-0.4	-4	-4	-6	-12	mA
lou	MAX	16	8	4	4	6	12	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ΠL	LS	CD74 HC	CD74 HCT	LV 3V	LV 5V
describ.	A (HC, LV: A)	0	MAY	70	70	63	63	27.5	16
tPLH	В	Q	MAX	55	55	63	63	27.5	16
(21)	A (HC, LV: A)	ā	MAN	80	80	51	51	27.5	16
TPHL	В	u	MAX	65	65	51	51	27.5	16
tPHL .	01	Q	MAN	27	55	48	57	22	13
tPLH	Clear	ā	MAX	40	65	54	56	22	13

Logic Diagram



		INPUTS							OUT	PUTS				and a sure of the second second second
LE	OE0	OE1	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	BOYSEE DECORESION
X	X	Н	X	X	X	L	L	L	L	L	L	L	L	
X	L	X	X	X	X	L	L	L	L	L	L	L	L	
L	H	L	L	Ĺ	L	H	L	L	L	L	L	L	L	
L	Н	L	L	L	H	L	H	L	L	L	L	L	L	
L	H	L	L	H	L	L	L	H	L	L	L	L	L	
L	H	L	L	H	H	L	L	L	H	L	L	L	L	
L	H	L	Н	L	L	L	L	L	L	H	L	L	L	
L	H	L	H	L	H	L	L	L	L	L	H	L	L	
L	H	L	H	H	L	L	L	L	L	L	L	H	L	
L	H	L	H	Н	H	L	L	L	L	L	L	L	H	
Н	H	L	X	X	X	Depend	s upon th	e address	s previous	sly applied	while LE	was at a	logic low.	

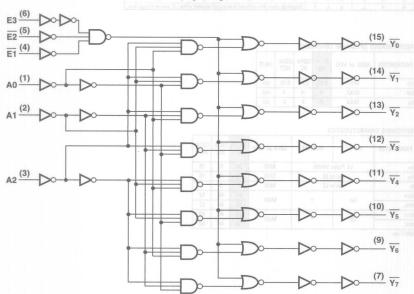
# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
lcc	MAX	0.08	0.16	0.16	mA
Іон	MAX	-4	-4	-4	mA
lou (6)	MAX	4	4	4	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
tw	LE Puls	e Width	MIN	20	15	15
tsu	An	to LE	MIN	19	15	15
th	An	to LE	MIN	5	9	5
tPLH .	An	Y	MAX	48	48	57
tPHL (1)	An	T	WAX	48	48	57
tPLH	0.5	v	MAN	44	44	60
tPHL .	0E	T -	MAX	44	44	60

## Logic Diagram



			DUTO	OUT						UTS	INP		
			2018	OUTI				ss	DDRES	Al	E	NABLE	E
Y7	Y6	Y5	Y4	Y3	Y2	Y1	YO	A0	A1	A2	E1	E2	E3
L	L	L	L	L	L	L	L	X	X	X	Н	X	X
L	L	F	L	auf a	E F	FE	L	X	X	X	X	X	L
L	L	L	L	L	L	L	L	X	X	X	X	Н	X
L	L	L	L	L	L	L	Н	L	L	L	L	L	Н
L	PETA	L	T.	T.	L	Н	L	Н	L	L	L	L	Н
L	L/	L	ankey	1 ba	H	1 L	L	ak n	Н	L	L	L	Н
L	L	L	L	Н	L	L	L	Н	Н	L	L,	L	Н
L	L	L	Н	L	L	L	L	L	L	Н	L	L	Н
L	L.	H	L	L	L	L	L	Н	L	H	L	L	Н
L	Н	L	L	L	L	L	L	L	Н	Н	L	L	Н
Н	og.	L	S LUB	L	L	L	L	Н	Н	Н	L	L	Н

Note: H = High Voltage Level, L = Low Volltage Level, X = Don't Care

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
lcc	MAX	0.16	0.16	0.16	0.16	mA
Іон	MAX	-4	-4	-24	-24	mA
lor	MAX	4	4	24	24	mA

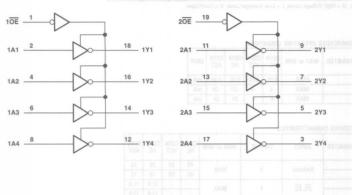
### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
tPLH	Address	y	MAX	45	53	15	15
tPHL	Address	1	IVIAX	45	53	15	15
tPLH .	E1, E2	v	BAAV	-	5=3	11.9	11.9
tPHL .	E1, EZ	,	MAX	-	-	11.9	11.9
tPLH	E3	v	MAX	-	120	16.6	16.6
tphl.	ES	1	IVIAA	2	-	16.6	16.6

### **OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS**

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- PNP Inputs Reduce DC Loading
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

### Logic Diagram



### RECOMMENDED OPERATING CONDITIONS

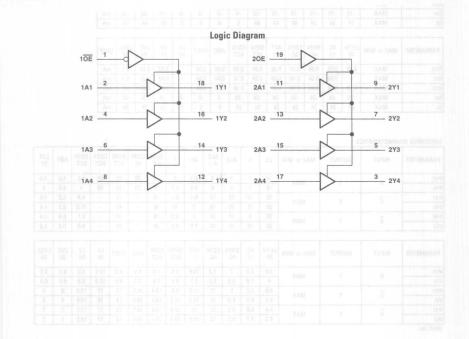
PARAMETER	MAX or MIN	LS	S	ALS	ALS A-1	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVT 3V	UNIT
Іссн	MAX	27	135	11	11	17	29	0.08	0.16	0.08	0.16	31	0.25	0.19	mA
Iccl	MAX	44	150	23	23	75	75	0.08	0.16	0.08	0.16	71	30	5	mA
Iccz	MAX	50	150	25	25	38	63	0.08	0.16	0.08	0.16	9	0.25	0.19	mA
Іон	MAX	-15	-15	-15	-15	-15	-15	-6	-6	-6	-6	-15	-32	-32	mA
lou	MAX	24	64	24	48	64	64	6	6	6	6	64	64	64	mA

PARAMETER	MAX or MIN	LVTH 3V	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	TAC TAC	LVCZ 3V	UNIT
Іссн	MAX	0.19	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-1	0.02	0.01	0.1	mA
ICCL	MAX	5	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.01	0.1	mA
lccz	MAX	0.19	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.01	0.1	mA
Іон	MAX	-32	-24	-24	-24	-24	-24	-24	-8	-8	-8	-16	-24	-24	mA
lou	MAX	64	24	24	24	24	24	24	8	8	8	16	24	24	mA

### SWITCHING CHARACTERISTICS

OTTITOTING OIL		1	_	_		_	-		_		_	_		-		-
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	ALS A-1	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVT 3V
tPLH .	N 2 A	V	MAX	14	7	9	9	6.5	8	25	30	32	33	5.6	4.8	3.8
tphl.	A	1	IVIAX	18	7	9	9	6.5	5.7	25	30	32	33	4	4.8	4
tPZH	G	v	MAX	23	10	13	13	6.4	6.1	38	-	44		8.8	5.2	4.6
tPZL	b	1	IVIAX	30	15	18	18	9	10	38	-	44	-	10.5	6.2	4.4
tPHZ	-	v	MAY	25	9	10	10	5	6.3	38	-	44	-	8.1	6.4	4.4
tPLZ	U	, T	Y MAX		15	12	12	9.5	9.5	38	-	44	-	9.5	5.8	4.3

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	3V LVC	LVCZ 3V
tPLH .		v	MAN	3.8	8.4	7	7.2	10.6	9.5	8.6	8.5	9.5	12.5	8.5	6.5	6.5
tPHL .	А	1	MAX	4	7.2	6.5	7.2	8.7	8.5	8.6	8.5	9.5	12.5	8.5	6.5	6.5
tPZH	G	V	MAX	4.6	9.2	8	12	12.5	9.5	13.4	10.5	13	16	10.5	8	8
tPZL	G	1	IVIAX	4.4	8.7	8.5	12	12.3	10.5	13.4	10.5	13	16	10.5	8	8
tPHZ	G	v	MAX	4.4	6.6	9.5	12	10	10.5	13.4	10.5	13	17	15.5	7	7
tPLZ	U	Υ.	IVIAX	4.3	7.7	9.5	12	10.8	10.5	13.4	10.5	13	17	15.5	7	7



### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 BCT	ABT	LVTH 3V	SN74 AC	UNIT	
СН	MAX	27	160	18	35	60	0.08	0.16	0.16	43	0.25	0.19	0.04	mA	
CCL	MAX	46	180	26	90	90	0.08	0.16	0.16	85	30	5	0.04	mA	
CCZ	MAX	54	180	30	56	90	0.08	0.16	0.16	10	0.25	0.19	0.04	mA	
)H	MAX	-15	-15	-15	-15	-15	-6	-6	-6	-15	-32	-32	-24	mA	
DL	MAX	24	64	24	64	64	6	6	6	64	64	64	24	mA	

PARAMETER	MAX or MIN	SN74 ACT	CD74 ACT	UNIT
Іссн	MAX	0.04	0.16	mA
ICCL	MAX	0.04	0.16	mA
lccz	MAX	0.04	0.16	mA
Іон	MAX	-24	-24	mA
lou	MAX	24	24	mA

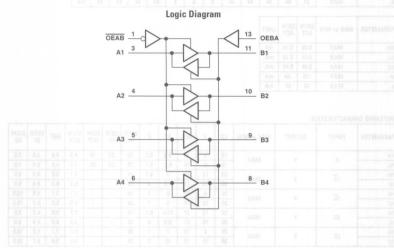
### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74	CD74	CD74	SN74	ABT	LVTH	SN74 AC
			100 100			N			HC	HC	HCT	BCT		3V	
tPLH	Α	Y	MAX	18	9	11	6.2	6.2	29	33	38	4.9	4.6	3.5	7.5
tPHL .	А	'	IVIAA	18	9	10	6.2	6.5	29	33	38	5.9	4.6	3.4	7.5
tPZH	1G	V	MAX	23	12	21	9	6.7	38	-	-	8.7	6.8	4.5	9.5
tPZL	10	,	IVIAA	30	15	21	7.5	8	38	8 .	-	9.4	6.8	4.4	9.5
tPHZ	1G	Y	MAX	25	9	10	6	7	38	-	-	8.1	7.1	4.5	10.5
tPLZ	10	,	IVIAA	20	15	15	9	7	38	-	-	9.9	5.9	4.7	10.5
tPZH	2G	V	MAX	23	12	21	10.5	6.7	38	-	-	8.7	6.8	4.5	9.5
tPZL	20	1	IVIAA	30	15	21	8.5	8	38	-	-	9.4	6.8	4.4	9.5
tPHZ	2G	Y	MAX	25	9	10	7	7	38	-		8.1	7.1	4.5	10.5
tPLZ	20	,	IVIAA	20	15	15	12	7	38	-	-	9.9	5.9	4.7	10.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 ACT	CD74 ACT
tPLH .		-		9.5	9.6
tPHL .	А	Y	MAX	8.5	9.6
tPZH	1G	· ·		9.5	13.4
tPZL	16	Y	MAX	10.5	13.4
tPHZ	1G		MAN	10.5	13.4
tPLZ	16	Y	MAX	10.5	13.4
tPZH	00	Y	MAN	9.5	13.4
tPZL	2G	Y	MAX	10.5	13.4
tPHZ	20	Y	MANY	10.5	13.4
tPLZ	2G	Y	MAX	10.5	13.4

### QUADRUPLE BUS TRANSCEIVERS

- Two-Way Asynchronous Communication Between Data Buses
- PNP Inputs Reduce DC Loading



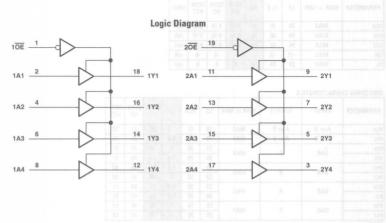
INP	UTS	
GAB	GBA	OPERATION
L	L	A to B
H	H	B to A
H	L	Isolation
L	H	Latch A and B (A = B)

PARAMETER	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	CD74 HCT	UNIT
Іссн	MAX	38	25	44	0.08	0.16	0.16	mA
ICCL	MAX	50	30	74	0.08	0.16	0.16	mA
lccz	MAX	54	32	56	0.08	0.16	0.16	mA
Іон	MAX	-15	-15		19.	-6	-6	mA
lou	MAX	24	24	64	6	6	6	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	CD74 HCT
tPLH .	A or B	A or B	MAX	18	11	7.5	25	27	33
tphL .	A or B	A or B	MAX	18	11	6.5	25	27	33
tPZH	GAB	В	MAX	23	20	9	38	45	51
tPZL	GAB	В	IVIAX	30	20	7.5	38	45	51
tPHZ	GAB	В	MAX	25	14	6.5	38	45	53
tPLZ	UAD	D	IVIAA	20	22	9	38	45	53
tPZH	GAB	А	MAX	23	20	10.5	38	45	51
tPZL	GAD	A	IVIAA	30	20	8.5	38	45	51
tPHZ	CAD		MAX	25	14	7	38	45	53
tPLZ	GAB	A	IVIAX	20	22	11	38	45	53

## 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



RECOMMENDED	

RECOMMENDE	D OPERATING	CONDI	TIONS	10.1			-										_	138	18
PARAMETER	MAX or MIN	LS	S	ALS	ALS C-1	AS	F <sub>FIRE</sub>	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	SN64 BCT	ABT	LVT 3V	LVTH 3V	LVTT	LVTZ 3V	UNIT
Іссн	MAX	27	160	17	17	34	60	0.08	0.16	0.08	0.16	40	40	0.25	0.19	0.19	0.19	0.225	mA
ICCL	MAX	46	180	24	24	90	90	0.08	0.16	0.08	0.16	80	80	30	5	5	12	15	mA
lccz	MAX	54	180	27	27	54	90	0.08	0.16	0.08	0.16	10	10	0.25	0.19	0.19	0.19	0.225	mA
Іон	MAX	-15	-15	-15	-15	-15	-15	-6	-6	-6	-6	-15	-15	-32	-32	-32	-32	-32	mA
lot.	MAX	24	64	24	48	64	64	6	6	6	6	64	64	64	64	64	64	64	mA
												19	pulso	WUU!	17,010	TROUGH	D-D-11	2 1473	
PARAMETER	MAX or MIN	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	LVCH 3V	LVCZ 3V	ALVC 3V	ALVCH 3V	UNIT	1	
Іссн	MAX	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.01	0.01	0.1	0.01	0.01	mA		
lccL	MAX	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.01	0.01	0.1	0.01	0.01	mA		
Iccz	MAX	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.01	0.01	0.1	0.01	0.01	mA	1	

-24 -24 -24 -24 -24 -24 -8 -8 -8 -16 -24 -24 -24 -24 -24 mA

16 24 24 24 24 mA

### SWITCHING CHARACTERISTICS

MAX

MAX

SVIII GIIII G CII	AIIACILIIIOII	00								notified the second sec	desert.					
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	s	ALS	ALS C-1	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	SN64 BCT	ABT
tPLH .	Λ	v	MAX	18	9	10	10	6.2	6.2	29	33	35	38	5	5.3	4.6
tphL .	A		IVIAA	18	9	10	10	6.2	6.5	29	33	35	38	5.5	6	4.6
tPZH	G	HISAVISA	MAN	23	12	20	20	9	6.7	38	IA-	44	DEC 10	8.7	9	5.1
tPZL	W.G. VE	1	MAX	30	15	20	20	7.5	8	38	-	44		8.9	9.4	6.1
tPHZ	0.0	ESD , 200	MAX	25	9	10	10	6	7	38	65 -	44	XA	7.7	8	6.6
tPLZ	8		IVIAX	20	15	13	13	9	7	38	10 -	44	*41	8.9	9.8	5.7

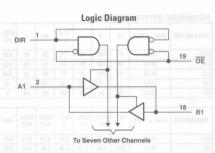
PARAMETER	INPUT	ОИТРИТ	MAX or MIN	LVT 3V	LVTH 3V	LVTT	LVTZ 3V	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V
tPLH	10.4	18 V 18		3.5	3.5	4.1	4.1	7.3	7.5	8.2	9.9	10	9.6	8.5	9.5	13.5
tPHL	A	Y	MAX	3.3	3.3	4.1	4.1	6.9	7.5	8.2	9.2	10	9.6	8.5	9.5	13.5
tPZH	G		MAX	4.5	4.5	5.2	5.2	8.5	8	12	12.5	9.5	13.4	10.5	13	16
tPZL TIME	HEVE MAYER	ZIVI KUVI	IVIAX	4.4	4.4	5.2	5.2	8.5	8.5	12	11.4	10.5	13.4	10.5	13	16
tPHZ	ē	V	MAX	4.4	4.4	5.6	5.6	7.3	9.5	12	10.4	10.5	13.4	10.5	13	18
tPLZ	100 100	1.0 10.0	WIAX	4.4	4.4	5.1	5.1	8.2	9.5	12	11.2	10.5	13.4	10.5	13	18

PARAMETER	INPUT	OUTPUT	MAX or MIN	LV 5V	LVC 3V	LVCH 3V	LVCZ 3V	ALVC 3V	ALVCH 3V
tPLH .	A	15 V 15	I MAN	8.5	5.9	5.9	5.9	2.8	2.8
tPHL .	A	100 100	MAX	8.5	5.9	5.9	5.9	2.8	2.8
tPZH	G	V	AAAV	10.5	7.6	7.6	7.6	4.5	4.5
tPZL	G	1	MAX	10.5	7.6	7.6	7.6	4.5	4.5
tPHZ	G	v	MAN	15.5	6.5	5.8	6.5	4.2	4.2
tPLZ	G	1	MAX	15.5	6.5	5.8	6.5	4.2	4.2

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### OCTAL BUS TRANSCEIVERS

- 3-State Outputs Drive Bus Lines Directly
- PNP Inputs Reduce DC Loading on Bus Lines
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



### FUNCTION TABLE

ENABLE G	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	Y	leolation

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	ALS C-1	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	SN64 BCT	ABT	ABTH	LVT 3V	LVTH 3V	LVTR 3V	UNIT
Іссн	MAX	70	45	45	97	90	0.08	0.16	0.08	0.16	57	57	0.25	0.25	0.19	0.19	0.19	mA
Icci	MAX	90	55	55	143	120	0.08	0.16	0.08	0.16	90	90	30	30	5	5	12	mA
lccz	MAX	95	58	58	123	110	0.08	0.16	0.08	0.16	15	15	0.25	0.25	0.19	0.19	0.19	mA
lon (A port)	MAX	-15	-15	-15	-15	-3	-6	-4	-6	-4	-3	-3	-32	-32	-32	-32	-12	mA
loн (B port)	MAX	-15	-15	-15	-15	-15	6	-4	-6	-4	-15	-15	-32	-32	-32	-32	-32	mA
lot (A port)	MAX	24	24	48	64	24	-6	-4	6	4	24	24	64	64	64	64	32	mA
lot (B port)	MAX	24	24	48	64	64	6	4	6	4	64	64	64	64	64	64	32	mA

PARAMETER	MAX or MIN	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	АНСТ	SV 3V	LV 5V	3V LVC	LVCH 3V	LVCZ 3V	ALVC 3V	ALVCH	UNIT
Іссн	MAX	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	1	0.02	0.01	0.01	0.1	0.01	0.01	mA
lccL	MAX	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	1.0	0.02	0.01	0.01	0.1	0.01	0.01	mA
lccz	MAX	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04		0.02	0.01	0.01	0.1	0.01	0.01	mA
loн (A port)	MAX	-24	-24	-24	-24	-24	-24	-8	-8	-8	-16	-24	-24	-24	-24	-24	mA
loн (В port)	MAX	-24	-24	-24	-24	-24	-24	-8	-8	-8	-16	-24	-24	-24	-24	-24	mA
lot (A port)	MAX	24	24	24	24	24	24	8	8	8	16	24	24	24	24	24	mA
lot (B port)	MAX	24	24	24	24	24	24	8	8	8	16	24	24	24	24	24	mA

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS C-1	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	SN64 BCT	ABT	ABTH
tPLH .	A D	D. A.	MAX	12	10	10	7.5	7	26	33	28	39	7	7	3.6	3.6
tPHL	A, B	B, A	IVIAX	12	10	10	7	7	26	33	28	39	7	7	3.9	3.9
tpzH	G	A D	MAX	40	20	20	9	8	58	45	58	48	10.9	10.9	5.6	5.6
tPZL	G	A, B	IVIAX	40	20	20	8.5	9	58	45	58	48	11.6	11.6	6.2	6.2
tPHZ	G		144V	28	10	10	5.5	7.5	50	45	50	45	9.3	9.3	5.9	5.9
tPLZ	G	A, B	MAX	25	15	15	9.5	7.5	50	45	50	45	9.1	9.1	4.5	4.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVT 3V	LVTH 3V	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V
tPLH	A D	В. А.	MAX	3.5	3.5	9.5	7	8.5	10	8	10	8.5	9.5	13.5	8.5	6.3
tPHL TILL	A, B	B, A	MAX	3.5	3.5	6.9	7	8.5	9.1	9	10	8.5	9.5	13.5	8.5	6.3
tPZH	G	4.0	MAX	5.5	5.5	11.4	9	14	13.2	11	14	12	16	19	12	8.5
tPZL	G	A, B	MAX	5.5	5.5	9.5	9.5	14	12.9	12	14	12	16	19	12	8.5
tphz	G	A D	MAN	5.9	5.9	9.5	10	14	12.9	11	14.4	11	16.5	22	16	7.5
tPLZ	G	A, B	MAX	5	5	10.4	10	14	13.9	11	14.4	11	16.5	22	16	7.5

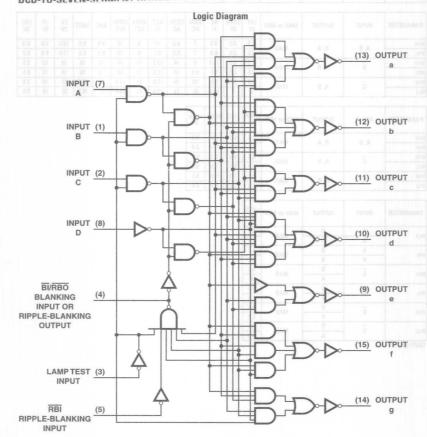
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVCH 3V	LVCZ 3V	ALVC 3V	ALVCH 3V
tPLH .	A, B	B, A	MAX	6.3	6.3	3.4	3.4
tphl.	A, b	В, А	WAX	6.3	6.3	3.4	3.4
tPZH	G	A D	MANY	8.5	8.5	5.5	5.5
tPZL	G	A, B	MAX	8.5	8.5	5.5	5.5
tPHZ	0 (7)	A D	MAX	7.5	7.5	5.5	5.5
tPLZ	d	A, B	IVIAX	7.5	7.5	5.5	5.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTR 3V
tPLH TUST	in An	В	MAY	4.2
UPLH	В	Α	MAX	4.4
terri	Α	В	MAX	4.6
tPHL .	В	A	IVIAX	4.1
in au	G	В	MAY	5.5
tPZH	G	А	MAX	6
tezu	(G)	В	MAX	6.6
IPZL B	G	Α	IVIAX	6.4
ania.	G	В	MAN	6.1
tPHZ	G	A	MAX	5.8
	G	В	MANY	5.2
tPLZ	G	A	MAX	5.2

UNIT: ns

PPLE-BLANKII INPUT

# BCD-TO-SEVEN-SEGMENT DECODEDS/DBIVEDS WITH BUTTO



DECIMAL OR		- 1	NPU	TS			BI/RBO			0	UTPU	rs		
FUNCTION	LT	RBI	D	C	В	Α		a	b	С	d	е	f	g
0	Н	Н	L	L	L	L	Н	ON	ON	ON	ON	ON	ON	OFF
1	H	X	L	L	L	H	н	OFF	ON	ON	OFF	OFF	OFF	OFF
2	H	X	L	L	H	L	Н	ON	ON	OFF	ON	ON	OFF	ON
3	H	X	L	L	H	Н	Н	ON	ON	ON	ON	OFF	OFF	ON
4	Н	X	L	Н	L	L	Н	OFF	ON	ON	OFF	OFF	ON	ON
5	H	X	L	H	L	Н	Н	ON	OFF	ON	ON	OFF	ON	ON
6	H	X	L	H	H	L	Н	ON	OFF	ON	ON	ON	ON	ON
7	H	X	L	Н	H	Н	н	ON	ON	ON	OFF	OFF	OFF	OFF
8	Н	X	Н	L	L	L	Н	ON	ON	ON	ON	ON	ON	ON
9	H	X	H	L	L	Н	H	ON	ON	ON	ON	OFF	ON	ON
10	H	X	H	L	H	L	and Harris	OFF	OFF	OFF	ON	ON	OFF	ON
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON
12	Н	X	Н	Н	L	L	Н	OFF	ON	OFF	OFF	OFF	ON	ON
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON
15	Н	X	Н	Н	H	Н	Н	OFF	OFF	OFF	OFF	OFF	OFF	OFF
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON

### RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	TTL	LS	UNIT
lcc		MAX	103	13	mA
Vo (off)	- 41	MAX	15	15	٧
lo (on)	a thru g	MAX	40	24	mA
Іон	BI/RB0	MAX	-0.2	-0.05	mA
lou	BI/RBU	MAX	8	3.2	mA

### SWITCHING CHARACTERISTICS

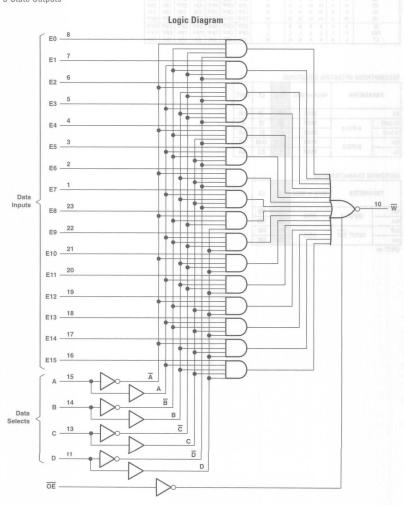
P	ARAMETER	MAX or MIN	TTL	LS
toff	INPUT A	14111	100	100
ton	INPUTA	MIN	100	100
toff	INDUT DO	MIN	100	100
ton	INPUT RBI	MIN	100	100

### 1-OF-16 DATA SELECTOR/MULTIPLEXER

- 4-Line to 1-Line Multiplexers That Can Select 1-of-16 Data Inputs
- Applications:

Boolean Function Generator Parallel-to-Serial Converter Data Source Selector

- Buffered 3-State Bus Driver Inputs Permit Multiplexing From n Lines to One Line
- 3-State Outputs



		INI	PUTS			OUTPUT
G	Α	В	C	D	Ei	W
L	L	L	L	L	E0	E0
L	Н	L	L	L	E1	E1
L	L	H	L	L	E2	E2
L	Н	H	L	L	E3	E3
L	L	L	H	L	E4	E4
L	Н	L	H	L	E5	E5
L	L	Н	Н	L	E6	E6
L	H	H	Н	L	E7	E7
L	L	L	L	Н	E8	E8
L	Н	L	L	Н	E9	E9
L	L	H	L	H	E10	E10
L	Н	H	L	H	E11	E11
L	L	L	H	H	E12	E12
	H	L	H	H	E13	E13
L	L	H	H	Н	E14	E14
L	H	H	H	H	E15	E15
H	X	X	X	X	X	Z

### ECTORS/WHI TIPLEXERS

- 121' in poissol/ etel2-5 4
- 3-State Outguts Interface Directly with System Bu
  - Perform Parallel-to-Serial Conversion
- Complementary Outputs Previde True and Inverted Data

### Logic Diagram

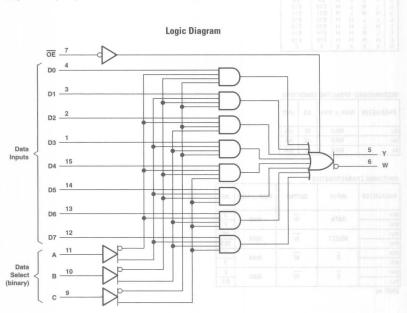
### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	UNIT
Icc	MAX	50	mA
Іон	MAX	-15	mA
IOL	MAX	48	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AS
tPLH .	DATA			8
tphL .	DATA	W	MAX	7
tPLH .	OFLECT	w	MAN	13
tphl.	SELECT	VV	MAX	10.5
tрzн	G	w	MAN	7
tPZL	G	VV	MAX	9
tPHZ	-	w	MAN	6
tPLZ	G	VV	MAX	6.5

Complementary Outputs Provide True and Inverted Data



L	н	н	L	LD3	D3
Н	L	L	L	D4	D4
Н	L	H	L	D5	D4 D5
Н	H	L	L	D6	D6
Н	H	Н	L	D7	D7

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 AC	CD74 AC	UNIT
lcc	MAX	62	12	85	14	24	0.08	0.16	0.16	0.16	0.16	mA
Гон	MAX	-5.2	-2.6	-6.5	-2.6	-3	-6	-4	-4	-24	-24	mA
los.	MAX	16	8	20	24	24	6	4	4	24	24	mA

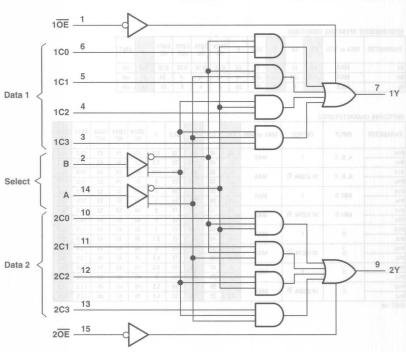
### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TIL	LS	S	ALS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 AC	CD74 AC
tPLH .	ARC	Y	MAX	45	45	18	18	9.5	51	74	63	18.2	18.2
tphl .	A, B, C	1	IVIAA	45	45	19.5	24	7.5	51	74	63	18.2	18.2
tplh	A D C	W (CD74: Y)	MAY	33	33	15	24	12.5	51	74	63	19.6	19.6
tphl.	A, B, C	VV (CD/4: 1)	MAX	33	33	13.5	23	9	51	74	63	19.6	19.6
tPLH	ANY D	Y	MAX	28	28	12	10	7	49	53	53	13.5	13.5
tPHL .	ANT D	1	WAX	28	28	12	15	5	49	53	53	13.5	13.5
tPLH	ANY D	W (CD74: Y)	MAX	15	15	7	15	8	49	53	53	14.9	14.9
tphl .	ANTU	VV (CD/4: 1)	MAX	15	15	7	15	8	49	53	53	14.9	14.9
tpzh	G	Y	MAX	27	45	19.5	15	7	36	42	45	13.5	13.5
tPZL	G	1	IVIAX	40	40	21	15	6.5	36	42	45	13.5	13.5
tPZH	G	W (CD74; Y)	MAX	27	27	19.5	15	6	36	42	45	13.5	13.5
tPZL	G	VV (CD/4. 1)	IVIAA	40	40	21	15	4.5	36	42	45	13.5	13.5
tPHZ	G	Y	MAX	8	45	8.5	10	8.5	49	42	45	13.5	13.5
tPLZ	0	1	IVIAA	23	25	14	10	8	49	42	45	13.5	13.5
tPHZ	G	W (CD74; Y)	MAX	8	55	8.5	10	5.5	49	42	45	13.5	13.5
tPLZ	G	VV (GD74. 1)	IVIAA	23	25	14	10	4.5	49	42	45	13.5	13.5

### **DUAL DATA SELECTORS/MULTIPLEXERS**

- 3-State Version of '153
- Perform Parallel-to-Serial Conversion

### Logic Diagram



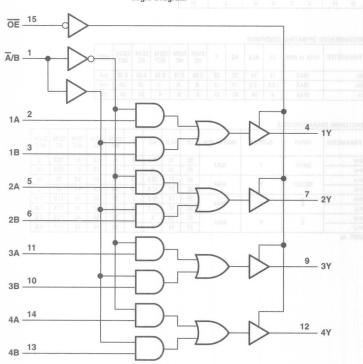
	ECT	1	DATA I	INPUTS	8	OUTPUT	ОИТРИТ
В	Α	CO	C1	C2	C3	G	Υ
X	X	X	X	X	X	Н	Z
L	L	L	X	X	X	L	L
L	L	H	X	×	X	ne Sketein	H
L	H	X	L	X	X	and for any	Len
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L.	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
Icc	MAX	14	14	33	23	0.08	0.16	0.16	0.16	0.16	mA
Іон	MAX	-2.6	-2.6	-15	-3	-6	-6	-4	-24	-24	mA
lou	MAX	8	24	48	24	6	6	4	24	24	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
tPLH	DATA	v	1441/	25	10	7.5	8	35	53	57	13.3	18
tPHL	DATA	Y	MAX	20	14	8	7	35	53	57	13.3	18
tPLH .	SELECT	V	MAX	45	21	13.5	13	38	53	60	20	22
tPHL	SELECT	T T	WAX	32	21	11.5	10	38	53	60	20	22
tPZH	G	V	MAX	28	14	12.5	9	25	33	45	11.5	12.6
tPZL	G	-	IVIAA	23	16	11.5	9	25	33	45	11.5	12.6
tPHZ	G	v	MAX	41	10	6	6	38	45	45	11.5	12.6
tPLZ	G	1	IVIAX	27	14	7	7	38	45	45	11.5	12.6



	INPUTS			OUTDUT
OUTPUT	SELECT	A	В	OUTPUT
Н	X	X	X	Z
L	L	L	X	L
L	L	Н	X	H
L	Н	X	L	L
	1.1	V	1.1	3.1

onio Diegram

### RECOMMENDED OPERATING CONDITIONS

				_	_	_	_	_	_	_	_	_		_	_	_
PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	CD74 AC	ACT 11	CD74 ACT	TAC.	UNIT
lcc	MAX	19	87	14	31.9	23	0.08	0.16	0.08	0.16	0.08	0.16	0.08	0.16	0.01	mA
Іон	MAX	-2.6	-6.5	-2.6	-15	-3	-6	-6	-6	-6	-24	-24	-24	-24	-24	mA
lou	MAX	24	20	24	48	24	6	6	6	6	24	24	24	24	24	mA

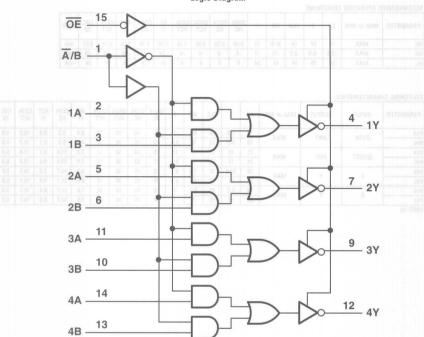
#### SWITCHING CHARACTERISTICS

OTTITION ON	ANAOTEMOTIC	70	_		_		_	_	_	_	-	_	_	_	_	_	_
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	CD74 AC	ACT 11	CD74 ACT	LVC 3V
tPLH .	DATA	ANY	MAX	13	7.5	10	5.5	7	25	45	38	50	6.4	9.3	6.9	10.7	4.6
tphl .				15	6.5	12	6	6.5	25	45	38	50	7.2	9.3	8.7	10.7	4.6
tPLH .	SELECT	ANY	MAX	21	15	18	-11	15	25	53	38	57	7.2	13.4	8.2	15.4	6.4
tphl.				24	15	22	10	9.5	25	53	38	57	7.9	13.4	9.4	15.4	6.4
tрzн	G	Υ	MAX	30	19.5	16	7.5	8.5	38	45	38	45	6.5	14.7	7.3	16.1	5.6
tPZL				30	21	18	9.5	8.5	38	45	38	45	8.6	14.7	9.6	16.1	5.6
tPHZ	G	Υ	MAX	30	8.5	10	6.5	7	38	45	38	45	7.6	14.7	8.4	16.1	4.3
tPLZ				25	14	15	7	7	38	45	38	45	7.6	14.7	8.5	16.1	4.3



#### **QUAD DATA SELECTORS/MULTIPLEXERS**

- 3-State Outputs Interface Directly with System Bus
- Provides Bus Interface from Multiple Sources in High-Performance Systems



	INPUTS			
OUTPUT	SELECT	А	В	OUTPUT
Н	X	X	X	Z
L	L	L	X	H
L	L	H	X	F
L	H	X	L	H
L	H	X	H	L

#### -BIT ADDRESSABLE LATCHES

8-Bit Parallel-Out Storage Register Pa

Asynchronous Parailel Clear

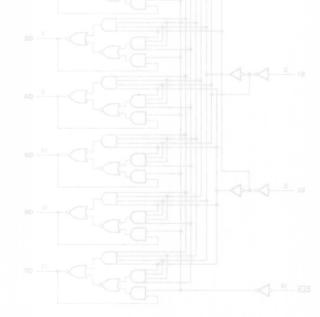
Enable/Disable Input Simplifies Expansio

#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 ACT	UNIT
Icc	MAX	16	87	13	25.2	23	0.08	0.16	0.16	0.16	mA
Іон	MAX	-2.6	-6.5	-2.6	-15	-3	-6	-6	-6	-24	mA
lou	MAX	8	20	24	48	24	6	6	6	24	mA

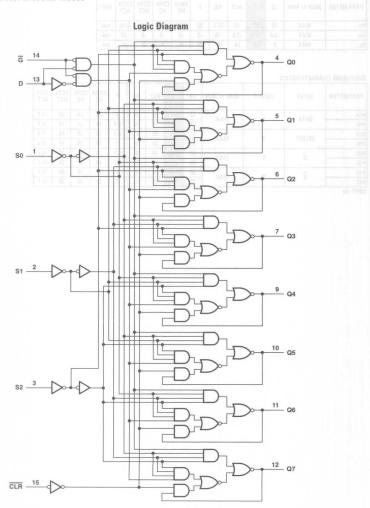
#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74		
tPLH	0.71			12	6	8	5	6	25	24	34	10.7		
tphl.	DATA	Y	MAX	17	6	7	4	5.5	25	24	34	10.7		
tPLH	OFLEGE	Y	V	V	Y MAX	21	12	25	9.5	9.5	29	35	43	15.4
tPHL .	SELECT		MAX	24	12	20	10	11	29	35	43	15.4		
tpzH	G		MAN	30	19.5	18	8	8.5	38	35	35	16.1		
tPZL	G	Y	MAX	30	21	18	10	8.5	38	35	35	16.1		
tPHZ	G	0 v	MANY	30	8.5	10	6	7	38	38	38	16.1		
tPLZ	G 50	-	MAX	25	14	18	6.5	7	38	38	38	16.1		



#### **8-BIT ADDRESSABLE LATCHES**

- 8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion with Storage
- Asynchronous Parallel Clear
- Active-High Decoder
- Enable/Disable Input Simplifies Expansion
- Expandable for n-Bit Applications
- Four Distinct Functional Modes



#### LATCH SELECTION

FUNCTI	ONT	ARIE

	NPUTS		LATCH ADDRESSED
С	В	Α	ADDRESSED
L	L	v.L.	0
L	L	H	1
L	H	L	2 3
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

INPUT	s	OUTPUT OF ADDRESSED	EACH	FUNCTION			
CLEAR	G	LATCH	OUTPUT	FUNCTION			
Н	L	D	QiO	Addressable latch			
Н	Н	QiO	Qi0	Memory			
L	L	D	L	8-line demultiplexer			
L	Н	L	L	Clear			

#### RECOMMENDED OPERATING CONDITIONS

NECOMMENDE	DUFENATING	COMPI	HUNS		,		-	
PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	UNIT
Icc	MAX	90	36	22	0.08	0.16	0.16	mA
Іон	MAX	16	8	8	4	4	4	mA
lor	MAX	-0.8	-0.4	-0.4	-4	-4	-4	mA

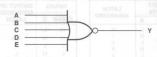
#### SWITCHING CHARACTERISTICS

P.	PARAMETER INPUT OUTPUT		MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	
tw	G			MIN	15	17	15	20	21	27
	CLR	1		IVIIIV	15	10	10	20	21	27
tsu	DATA	1		MIN	15	20	15	19	24	26
	ADDRESS	1		IVIIN	5	17	15	19	24	26
th	DATA	1		NAINI	0	0	0	5	0	0
	ADDRESS	1		MIN		0	0	5	0	0
tPLH .		CLEAR	Any Q	MAX	25	18	12	38	47	59
tPHL .		DATA	A O	1111	24	30	19	33	56	59
tPLH		DATA	Any Q	MAX	20	20	12	33	56	59
tPHL		4000000	4	MAN	28	27	22	50	56	61
tPLH		ADDRESS	Any Q	MAX	28	20	12	50	56	61
tPHL .		FNIADLE	4 0	1444	20	24	20	43	51	57
tPHL .		ENABLE	Any Q	MAX	20	24	13	43	51	57



## DUAL 5-INPUT POSITIVE-NOR GATES

 $Y = \overline{A + B + C + D + E}$ 



Logic Diagram

RECOMMENDED OPERATING CONDITIONS

				T
PARAMETER	MAX or MIN	S	F	UNIT
Icc	MAX	45	9.5	mA
Іон	MAX	-1	-1	mA
lor	MAX	20	20	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	S	F
tPLH .	4 0 0 0 5	ν.	MAX	5.5	6.5
tPHL .	A, B, C, D, E	Y	IVIAX	6	4.5

#### Logic Diagram

#### **QUAD COMPLEMENTARY-OUTPUT ELEMENTS**

- $\bullet$  Y =  $\overline{A}$ , W = A
- Y = AB, W = AB

EL	EM	ENTS	1	and	4

ELEMENTS 2 and 3





RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
Icc	MAX	34	mA
Іон	MAX	-0.8	mA
lou	MAX	16	mA

SWITCHING CHARACTERISTICS

INPUT	OUTPUT	MAX or MIN	TTL
A or B	w	MAX	18
A or B	Υ	MAX	18
A or B	W	MAX	18
A or B	Y	MAX	18
A or B	W with respect Y	MAX	±3
A or B	W with respect Y	MAX	±3
	A or B A or B A or B A or B A or B	A or B W A or B Y A or B W A or B W A or B Y A or B W with respect Y	A or B W MAX A or B Y MAX A or B W MAX A or B Y MAX A or B Y MAX A or B W with respect Y MAX A or B W with

#### OHAD 2 INDUT

#### **FUNCTION TABLE**

INP	UTS	OUTPUT
Α	В	Y
L	L	Н
L	H	L
H	L	L
H	H	H

#### RECOMMENDED OPERATING CONDITIONS

HEODIVINIENDE	D OI LIIATING	COIVE	TIOITO	_
PARAMETER	MAX or MIN	LS	нс	UNIT
lcc	MAX	13	0.02	mA
Vон	MAX	5.5	Vcc	V
lor	MAX	8	4	mA

#### SWITCHING CHARACTERISTICS

			T		T
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	SN74 HC
tРLН	A or B Other Input Low	Υ	MAX	30	31
tphL .	A or B Other Input Low	Υ	MAX	30	25
tplH	A or B Other Input High	Υ	MAX	30	31
tPHL .	A or B Other Input High	Υ	MAX	30	25

#### UNIT: ns

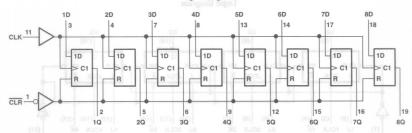
#### **Logic Diagram**

#### ZOLTZINGTOWNAL NO DIMENTINA

#### **OCTAL D-TYPE FLIP-FLOPS**

- Contain Eight Flip-Flops with Single-Rail Outputs
- Buffered Clock and Direct-Clear Inputs

#### Logic Diagram



#### **FUNCTION TABLE**

II	NPUTS		ОИТРИТ
CLEAR	CLOCK	D	Q
L	X	X	L
H	1	Н	H
H	1	L	L
Н	L	X	Q <sub>0</sub>

#### RECOMMENDED OPERATING CONDITIONS

DULLIATING	CONDI	HUNG			_	_					_	_	_		_	-
MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	LVTH 3V	CD74 AC	CD74 ACT	АНС	AHCT	LV 3V	LV 5V	UNIT
MAX	94	27	29	0.08	0.16	0.08	0.16	30	5	0.16	0.16	0.04	0.04	-	0.02	mA
MAX	-0.8	-0.4	-2.6	-4	-4	-4	-4	-32	-32	-24	-24	-8	-8	-6	-12	mA
MAX	16	8	24	4	4	4	4	64	64	24	24	8	8	6	12	mA
	MAX or MIN  MAX  MAX	MAX or MIN TTL  MAX 94  MAX -0.8	MAX 94 27 MAX -0.8 -0.4	MAX or MIN TTL LS ALS  MAX 94 27 29  MAX -0.8 -0.4 -2.6	MAX or MIN TTL LS ALS SN74 HC  MAX 94 27 29 0.08  MAX -0.8 -0.4 -2.6 -4	MAX or MIN TTL LS ALS SN74 CD74 HC HC HC MAX 94 27 29 0.08 0.16 MAX -0.8 -0.4 -2.6 -4 4	MAX or MIN TTL LS ALS SN74 CD74 SN74 HC HCT MAX 94 27 29 0.08 0.16 0.08 MAX -0.8 -0.4 -2.6 -4 -4 -4	MAX or MIN         TTL         LS         ALS         SN74 HC         CD74 HCT         MAZ         CD74 HCT           MAX         94         27         29         0.08         0.16         0.08         0.16           MAX         -0.8         -0.4         -2.6         -4         -4         -4         -4	MAX or MIN         TTL         LS         ALS         SN74 HC         CD74 HCT         CD74 HCT         ABT           MAX         94         27         29         0.08         0.16         0.08         0.16         30           MAX         -0.8         -0.4         -2.6         -4         -4         -4         -4         -32	MAX or MIN TTL LS ALS SN74 CD74 SN74 CD74 ABT LVTH HCT HCT ABT LVTH SV MAX 94 27 29 0.08 0.16 0.08 0.16 30 5 MAX -0.8 -0.4 -2.6 -4 -4 -4 -4 -32 -32	MAX or MIN         TTL         LS         ALS         SN74 HC         CD74 HC         MCD74 HCT         ABT         LVTH LVTH LVTH AR           MAX         94         27         29         0.08         0.16         0.08         0.16         30         5         0.16           MAX         -0.8         -0.4         -2.6         -4         -4         -4         -4         -32         -32         -24	MAX or MIN         TTL         LS         ALS         SN74 HC         CD74 HC         RHC HCT         ABT         LVTH LOT4 SVA ACT         CD74 ACT           MAX         94         27         29         0.08         0.16         0.08         0.16         30         5         0.16         0.16           MAX         -0.8         -0.4         -2.6         -4         -4         -4         -4         -32         -32         -24         -24	MAX or MIN         TTL         LS         ALS         SN74 HC         CD74 HC         RD74 HCT         ABT         LVTH         CD74 ACT         AHC           MAX         94         27         29         0.08         0.16         0.08         0.16         30         5         0.16         0.06         0.08           MAX         -0.8         -0.4         -2.6         -4         -4         -4         -4         -32         -32         -24         -24         -8	MAX or MIN         TTL         LS         ALS         SN74 HC         CD74 HC         NT74 HC         CD74 HCT         ABT         LVTH OT OT AC         CD74 AC         AHC         AHC         AHCT           MAX         94         27         29         0.08         0.16         0.08         0.16         30         5         0.16         0.16         0.04         0.04           MAX         -0.8         -0.4         -2.6         -4         -4         -4         -32         -32         -24         -24         -8         -8	MAX or MIN TTL LS ALS SN74 CD74 SN74 CD74 ABT LVTH CD74 CD74 AHC AHCT LV 3V AC ACT ACT AHC AHCT LV 3V AC ACT ACT AHC AHCT LV 3V ACT ACT ACT ACT ACT ACT ACT ACT ACT ACT	MAX or MIN TTL LS ALS SN74 CD74 SN74 CD74 ABT LVTH CD74 CD74 AHC AHCT LV SV SV ACC ACT AHC AHCT LV SV SV SV SV ACC ACT AHC AHCT LV SV SV SV ACC ACT AHC AHCT LV SV SV SV SV ACC ACT AHC AHCT LV SV SV SV SV ACC ACT AHC AHCT LV SV SV SV SV SV ACC ACT AHC AHCT LV SV SV SV SV SV ACC ACT AHC AHCT LV SV SV SV SV SV ACC ACT AHC AHCT LV SV SV SV SV SV ACC ACT AHC AHCT LV SV SV SV SV SV ACC ACT AHC AHCT LV SV SV SV SV SV ACC ACT AHC AHCT LV SV SV SV SV SV SV ACC ACT AHC AHCT LV SV SV SV SV SV ACC ACT AHC AHCT LV SV SV SV SV SV ACC ACT AHC AHCT LV SV SV SV SV SV ACC ACT AHC AHCT LV SV SV SV SV SV ACC ACT AHC AHCT LV SV SV SV SV SV SV ACC ACT AHC AHCT LV SV SV SV SV SV SV ACC ACT AHC AHCT LV SV SV SV SV SV SV SV ACC ACT AHC AHCT LV SV SV SV SV SV SV SV SV SV SV ACC ACT AHC AHCT LV SV SV SV SV SV SV SV SV SV SV SV SV SV

#### SWITCHING CHARACTERISTICS

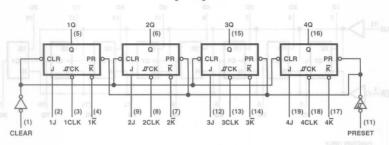
PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	LVTH 3V	CD74 AC	CD74 ACT	AHC	
fma	K	1000		MIN	30	30	35	21	20	16	16	150	150	100	85	70	
tw			NI to XANG	MIN	16.5	20	14	20	24	25	30	3.3	3.3	5	6	5	
tsu	tsu DATA INPUT			MIN	20	20	10	25	18	25	18	2.5	2.3	2	2	4.5	
	CLR INACVIVE		1/1/1/1	MIN	25	25	15	25	-	25		2	2.3	-		2	
th			SHN	MIN	5	5	0	0	3	0	3	1.2	0	2	2	-1	
tPHL .		CLEAR	ANY Q	MAX	27	27	18	40	45	42	48	7.4	4.9	13.5	13.5	12	
tPLH		CLOCK	1004	NAME OF TAXABLE PARTY.	MAX	27	27	12	40	45	42	45	6.5	4.8	13.5	13.5	12.5
tPHL .		CLUCK	ANY Q	IVIAX	27	27	15	40	45	42	45	7.3	4.3	13.5	13.5	12.5	

PARAMETER		INPUT	OUTPUT	MAX or MIN	AHCT	LV 3V	LV 5V
fmax	(		22.58	MIN	45	45	70
tw				MIN	6.5	6.5	5
tsu	DATA INPUT			MIN	5	6.5	4.5
	CLR INACVIVE			MIN	2.5	2.5	2
th				MIN	0	2	1
tPHL		CLEAR	ANY Q	MAX	12.6	19.5	12
tPLH .		CLOCK	ANY Q	MAX	9.8	19.5	12.5
<b>TPHL</b>		CLUCK	ANTU	IVIAX	11	19.5	12.5

#### QUAD J-K FLIP-FLORS

- Separate Negative-Edge-Triggered Clocks
- Fully Buffered Outputs

#### Logic Diagram



#### **FUNCTION TABLE**

COMMON	N INPUTS	INF	OUTPUT		
PRESET	CLEAR	CLOCK	J	K	Q
L	Н	X	X	X	H
H	L	×	X	×	L
L	L	×	X	×	H†
H	Н	1	L	H	Qo
H	H	1	H	H	H
H	THE H	1	L	L	L
H	H	1	H	L	TOGGLE
H	H	H	X	×	Qn

† The output levels in this configuration are not guaranteed to meet the minimum levels for Voys. Furthermore, this configuration is nonstable; that is, it will not persist when either PRE or CLR returns to its inactive (high) level.

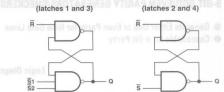
#### RECOMMENDED OPERATING CONDITIONS

NECOMMENDE	DULLIATING	CONDI	110143
PARAMETER	MAX or MIN	TTL	UNIT
Icc	MAX	81	mA
Іон	MAX	-0.8	mA
lou	MAX	16	mA

SWITCHING CHARACTERISTICS

_	CHING CHARAC	TERISTICS		_		
P P	ARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	
fmax		C	1010A	MIN	35	
tw CLOCK high CLOCK low tsu J, K				AMINI	13.5	
				MIN	15	
				****	3	
	CLD DD =			MIN	10	
th				MIN	10	
tPLH		PRESET	Q	MAX	25	
tPHL VI		CLEAR	Q	MAX	30	
tPLH tPHL				MAX	30	
		CLOC K	Q (2) (A)	MAX	30	

QUAD S-R LATCHES

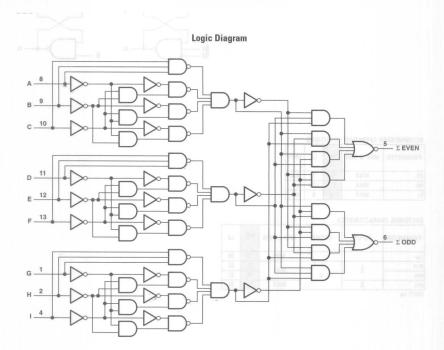


RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
Icc	MAX	30	7	mA
Іон	MAX	-0.8	-0.4	mA
lou	MAX	16	8	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
tw	-		MIN	20	20
tPLH	-		MANY	22	22
tphL .	5	a	MAX	15	21
tphL .	R		MAX	27	27



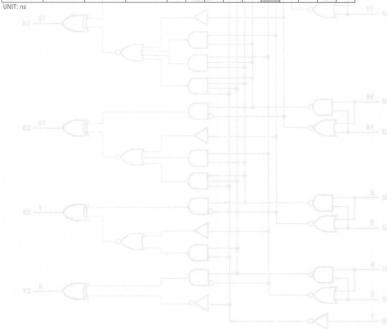
NO. OF INPUTS	OUTF	UTS
THAT ARE HIGH	ΣEVEN	ΣODD
0, 2, 4, 6, 8	Н	L
1, 3, 5, 7, 9	L	H

#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	s	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
Icc	MAX	27	105	16	35	35	0.08	0.16	0.16	0.16	0.16	mA
1он	MAX	-0.4	-1	-2.6	-2	-1	-4	-4	-4	-24	-24	mA
lor.	MAX	8	20	24	20	20	4	4	4	24	24	mA

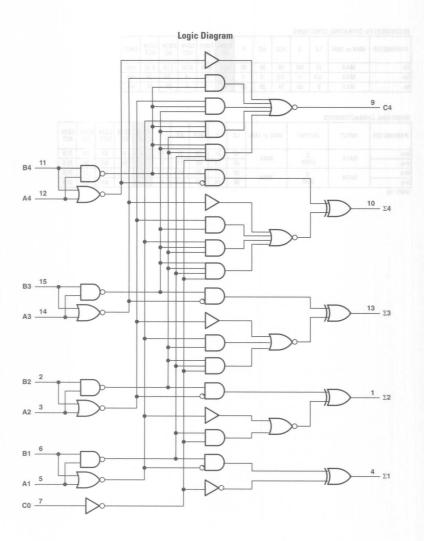
#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
tPLH	DATA	S EVEN	MAN	50	21	20	12	10	52	60	63	20	21.6
tphl .	DATA		MAX	45	18	20	11	11	52	60	63	20	21.6
tPLH	DATA	S	MAY	35	21	20	12	10	52	60	68	21	21.6
tphL -	DATA	ODD	MAX	50	18	22	11.5	11	52	60	68	21	21.6



#### **4-BIT BINARY FULL ADDERS**

Full-Carry Look-Ahead Across the Four Bits



#### CUNCTION TARI

			FUN	ICTIO	N TA	BLE				
						OUT	PUTS			
	INP	UTS		WH	IEN CO	= L	WH	IEN C	) = H	BIT PARITY GENERATOR/CHECKER WITH BUS DRIVE
				WH	IEN C2	= L	WH	IEN C	2 = H	
A1	B1	A2	B2	Σ1	Σ2	C2	Σ1	Σ2	C2	Generate Either Odd or Even Parity for Nine Bata Lines
A3	В3	A4	B4	Σ3	Σ4	C4	Σ3	Σ4	C4	Cascadable for n-Bit Parity
L	L	L	L	L	L	L	Н	L	L	
Н	L	L	L	H	C.L.	L	L	H	L	Direct Bus Connection for Parity Ganeration or Checking by
L	H	L	L	H	L	L		H	L	The second secon
н	H	L	L	L	H	9 Lo	H	H	L	ZARC 10000 Product Available in Reduced-Neise Advanced
L	L	H	L	L	H	L	Н	H	L	ZAACTITXXXC Product Available in Reduced-Noise Advanced
Н	L	H	L	H		mis.	L	E	Н	as our action recorded in arrelease for boild boxet in Assist
L	H	H	L	H	H	L	L	L	H	
Н	H	H	L	L	L	H	H	L	H	
L	L	L	H	L	Н	L	H	Н	L	
Н	L	L	Н	H	Н	L	L	L	Н	
L	Н	L	Н	H	Н	L	L	L	Н	
Н	Н	L	Н	-	L .	H	Н	L	H	
L	L	H	H	L	L	Н	Н	L	H	mineral (Amine I
Н	L	H	H	H	L	H	-	H	H	Logic Diagram
L	Н	H	H	Н	H	H	H	H	H	
Н	H	Н	Н	L	н	Н	H	н	Н	

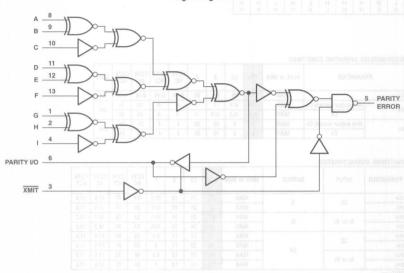
#### RECOMMENDED OPERATING CONDITIONS

	PARAMETER	MAX or MIN	TTL	TTL LS	S	F	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
Icc		MAX	110	39	160	55	0.16	0.16	0.16	0.16	mA
. BORR	Any output except C4	MAX	-0.8	-0.4	-1	-1	-4	-4	-24	-24	
Юн	C4	MAX	-0.4	-0.4	-0.5	-1	-4	-4	-24	-24	mA
i.	Any output except C4	MAX	16	8	20	20	4	4	24	24	
IOL	C4	MAX	8	8	10	20	4	4	24	24	mA

#### SWITCHING CHARACTERISTICS

ANACIENISTIC	)				-0-					
INPUT	OUTPUT	MAX or MIN	ΠL	LS	S	F	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
00	0	MAX	21	24	18	10.5	69	47	17.6	17.6
CU	5	MAX	21	24	18	10.5	69	47	17.6	17.6
Al Di	C:	MAX	24	24	18	10.5	63	69	18.2	18.2
AI OF BI	51	MAX	24	24	18	10.5	63	69	18.2	18.2
00		MAX	14	17	11	8.5	59	80	17.6	17.6
CO	04	MAX	16	22	11	8	59	80	17.6	17.6
A1 D1	L4	MAX	14	17	12	8.5	59	72	17.6	17.6
Ai or Bi		MAX	16	17	12	8	59	72	17.6	17.6
		INPUT	INPUT	INPUT	INPUT   OUTPUT   MAX or MIN   TTL   LS	INPUT   OUTPUT   MAX or MIN   TTL   LS   S	INPUT   OUTPUT   MAX or MIN   TTL   LS   S   F	INPUT OUTPUT MAX or MIN TTL LS S F CD74 HC  CO S MAX 21 24 18 10.5 69 MAX 21 24 18 10.5 69 MAX 21 24 18 10.5 69 MAX 24 24 18 10.5 63 MAX 24 24 18 10.5 63 MAX 24 24 18 10.5 63 MAX 24 24 18 10.5 63 MAX 24 24 18 10.5 63 MAX 14 17 11 8.5 59 MAX 16 22 11 8 59 MAX 16 12 21 11 8 59 MAX 16 17 12 8.5 59	INPUT   OUTPUT   MAX or MIN   TTL   LS   S   F   CD74   HCT   CD74   HCT	INPUT OUTPUT MAX or MIN TTL LS S F CD74 HC CD74 AC CD74 AC CD74 AC CD74 HC CD74 HC AC CD74 HC CD74 AC CD74 HC

• 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



(A-I) THAT ARE HIGH	XMIT	PARITY I/O	PARITY	
0, 2, 4, 6, 8	1	Н	Н	
1, 3, 5, 7, 9	Ī	L	Н	
0, 2, 4, 6, 8	h h	h I	H L	
1, 3, 5, 7, 9	h h	h	L H	

h = high input level I = low input level H = high output level L = low output level

#### RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	AS	AC 11	ACT 11	UNIT
Icc		MAX	50	0.08	0.08	mA
	Parity error	MAX	-2	-24	-24	mA
Іон	Parity I/0	MAX	-15	-24	-24	mA
	Parity error	MAX	20	24	24	mA
lor.	Parity I/O	MAX	48	24	24	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AS	AC 11	ACT 11
tPLH		MANY	15	9	10.4	
tPHL .	A to I	Parity I/O	MAX	14	107	12
tPLH .	A to i	Danita anna	MAX	16.5	10	11.3
tphl .		Parity error	IVIAA	16.5	12	12.9
tPLH	Parity I/O Parity error	Darita	MAN	9	6.2	7.7
tphl .		MAX	9	7.9	9.1	
tPZH			- do - d	13	5.3	7.3
tPZL	XMIT	Davis 110	MAX	16	8.9	11.4
tPHZ		Parity I/0	MAX	11.5	6.5	8.5
tPLZ				10	6.3	7.8

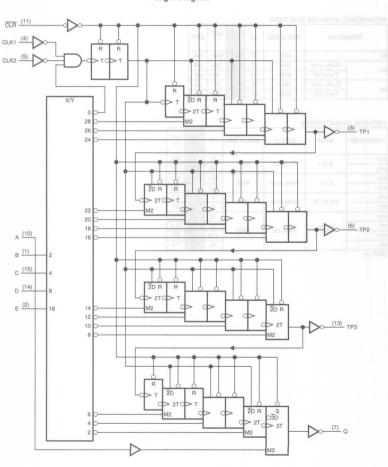
UNIT: ns



#### PROGRAMMABLE FREQUENCY DIVIDER/DIGITAL TIMER

- Digitally Programmable from 2<sup>2</sup> to 2<sup>31</sup>
- Easily Expandable
- Applications:

Frequency Division
Digital Timing



CLEAR	CLK 1	CLK 2	Q OUTPUT MODE
L	X	X	Cleared to L
H	#	L	Count
H	L	*	Count
Н	Н	X	Inhibit
Н	X	H	Inhibit

#### BIT BINARY COUNTERS

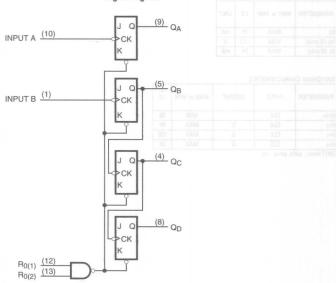
#### RECOMMENDED OPERATING CONDITIONS

112001111121102		001101	1
PARAMETER	MAX or MIN	LS	UNIT
Icc	MAX	75	mA
Iон (Q only)	MAX	-1.2	٧
IoL (Q only)	MAX	24	mA

#### mediann siber

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
fmax	CLK		MIN	30
tPLH	CLK	Q	MAX	90
tPHL	CLK	Q	MAX	120
tPHL	CLR	ā	MAX	65



#### COUNT SECUENCE

0011117	OUTPUTS				
COUNT	QD	QC	QB	QA	
0	L	L	L	H	
1	L	L	L	H	
2	L	L	H	L	
3	L	L	H	H	
4	L	H	L	L	
5	L	H	L	L	
6	L	HHH	H	L	
7	L	H	H	H	
8	H	L	L	L	
9	H	L	L	H	
10	HHHHH	L	L H H	L	
11	H	L	Н	H	
12	H	H	L	L	
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14	Н	Н	L	LHLHLHL	
14	H	Н	H	L	
15	H	H	Н	H	

NOTE: Output QA is connected to input B.

#### RESET/COUNT FUNCTION TABLE

RESET	INPUTS		OUTF	UTS	
R <sub>0</sub> (1)	R <sub>0</sub> (2)	QD	QC	QB	QA
H	Н	L	L	L	L
L	×	COUNT			
X	L		COL	INT	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
lcc	MAX	39	15	mA
Іон	MAX	-0.8	-0.4	mA
lou	MAX	16	8	mA

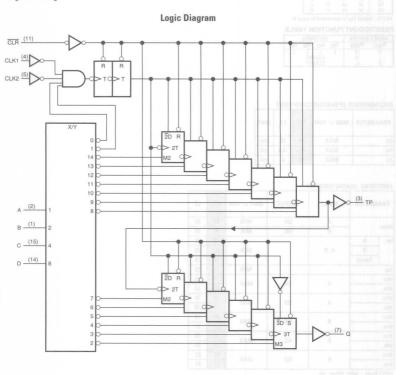
SWITCHING CHARACTERISTICS

PAF	RAMETER	INPUT OUTPUT MAX or MIN		TTL	LS	
		A	QA	MIN	32	32
fmax		В	QB	MIN	16	16
tw	A				15	15
	В	A, B		MIN	MIN 30	
	Reset		7	15	15	
tsu				MIN	25	
tPLH .			QA	144V	16	16
tPHL		Α	UA	MAX	18	18
tPLH		Α.	0.0	MAY	70	70
tPHL		Α	QB	MAX	70	70
tPLH		D.	0.0	MAN	16	16
tPHL .		В	QB	MAX	21	21
tPLH		0	00	MAN	32	32
tphl.		В	ac	MAX	35	35
tPLH	1		00	1111	51	51
tPHL		В	QD	MAX	51	51

#### PROGRAMMABLE FREQUENCY DIVIDER/DIGITAL TIMER

- Digitally Programmable from 2<sup>2</sup> to 2<sup>15</sup>
- Easily Expandable
- Applications

Frequency Division Digital Timing



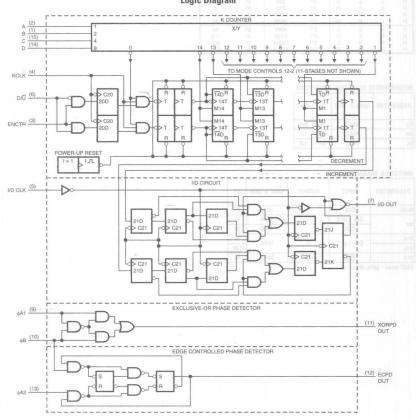
		III O INID	LITO		Y DIVISION		
PROGRAMMING INPUTS				Q	1	TP .	
D	С	В	Α	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	Н	Inhibit	Inhibit	Inhibit	Inhibit
L	L	H	L	22	4	29	512
L	L	H	H	23	8	29	512
L	Н	L	L	24	16	29	512
L	Н	L	Н	25	32	29	512
L	H	H	L	26	64	29	512
L	H	Н	H	27	128	Disab	led Low
Н	L	L	L	28	256	22	4
Н	L	L	H	29	512	23	8
Н	- L -	- H	L	210	1024	24	16
H	L	Н	Н	211	2048	25	32
H	H	L	L	212	4096	26	64
H	H	L	H	213	8192	27	128
H	H	H	L	214	16384	28	256
Н	H	H	H	215	32768	29	512

#### RECOMMENDED OPERATING CONDITIONS

	-	1
MAX or MIN	LS	UNIT
MAX	50	mA
MAX	-1.2	V
MAX	24	mA
	MAX MAX	MAX 50 MAX -1.2

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
fmax	CLK	1-4-	MIN	30
	CLK 1 or 2		MIN	16
tw	CLR	8 4	MIN	35
tPLH .	01111		MAN	90
tPHL .	CLK 1 or 2	u	MAX	120
tPLH .	CLR	ā	MAX	65



K COUNTER FUNCTION TABLE

EXCLUSIVE OR PHASE DETECTOR

D	С	В	Α	MODULO (K)
L	L	L	L	Inhibited
L	L	L	Н	22
L	L	Н	L	24
L	L	Н	Н	25
L	Н	L	L	26
L	H	L	Н	27
L	H	Н	L	28
L	H	Н	H	29
Н	L	L	L	210
Н	L	L	Н	211
H	L	Н	L	212
Н	L	Н	Н	213
Н	Н	L	L	214
Н	Н	L	н	215
Н	H-	H.	L	216
н	H	н	н	217

ØA1	φB	XORPD OUT
L	L	L
L	H	H
Н	L	H
H	Н	L

EDGE-CONTROLLED PHASE DETECTOR

Ø A2	ØΒ	ECPD OUT
HorL	1	Н
1	HorL	L
HorL	1	No change
1	HorL	No change

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	CD74 HC	CD74 HCT	CD74 ACT	UNIT
Icc	MAX	120	0.16	0.16	0.08	mA
Ioн (I/D OUT)	MAX	-1	-6	-4	-24	mA
IOH (XOR, ECPD)	MAX	-0.4	-6	-4	-24	mA
IoL (I/D OUT)	MAX	24	6	4	24	mA
IoL (XOR, ECPD)	MAX	8	6	4	24	mA

SWITCHING CHARACTERISTICS

PAR	RAMETER	IN	PUT	OUTPUT	MAX or MIN	LS	CD74 HC	CD74 HCT	CD74 ACT
		K	CLK	I/D OUT		32	20	20	45
fmax		-1/D	CLK	I/D OUT	MIN	16	13		35
tw	K CLK	100	7-10-4			16	24	24	8
	I/D CLK				MIN	33	38	38	9
tsu	D/Ū					30	30	30	17
	ENCLR				MIN	31	30	30	16
th	D/Ū					0	0	0	7
	ENCLR				MIN	0	0	0	6
tPLH				LID OUT	MAN	25	53	53	24
tPHL		1/D 1	CLK ↑	I/D OUT	MAX	35	53	53	24
			other input low	X or OUT		15	45	45	22
tpl.H		φA1 or φB	other input high	X 01 001		25	45	45	22
			other input low	V 0117	MAX	25	45	45	22
tPHL.		φA1 or φB	other input high	X or OUT		25	45	45	22
tPLH		ф	BŢ	ECPD OUT		30	60	60	30
tPHL			A2 ↓	ECPD OUT	MAX	30	60	60	30

#### QUAD 2-INPUT MULTIPLEXERS WITH STORAGE

Outputs Storage Register

# Logic Diagram A1 -3 ws \_\_10 A2 \_2 B1 \_\_4 B2 \_\_1 1R C1 \_\_9 13 QC C2 \_\_5 12 QD D2 \_\_6

INP	UTS		OUT	PUTS	
WORD SELECT	CLOCK	QA	QB	QC	QD
L	1	A1	B1	C1	D1
H	1	A2	B2	C2	D2
X	H	QAO	QBO	Qcn	Qnn

† a1, a2, etc. = the level of steady-state input at A1, A2, etc. QA0, QB0, etc. = the level of QA, QB, etc. entered on the most recent O transition of CLK

#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	AS	SN74 HC	UNIT
Icc	MAX	65	21	36	0.08	mA
lou	MAX	16	8	20	4	mA
Іон	MAX	-0.8	-0.4	-2	-4	mA

ogic Disgram

#### SWITCHING CHARACTERISTICS

P	ARAMETER	INPUT	OUTPUT	MAX or MIN	ΠL	LS	AS	SN74 HC
tw	8.5			MIN	20	20	8	27
	Data			MIN	15	15	4.5	21
Word Select				IVIIN	25	25	13	21
al-	Data			AMINI	5	5	3.5	0
th	Word Select			MIN	0	0	1	0
tPLH		OLIV	0400	MANY .	27	27	9	31
tPHL.		CLK	GA to GD	MAX	32	32	11	31

#### 8-BIT BIDIRECTIONAL UNIVERSAL SHIFT/STORAGE REGISTERS

- Multiplexed I/O Ports Provide Improved Bit Density
- Four Modes of Operation:

Hold (Store)

Shift Right

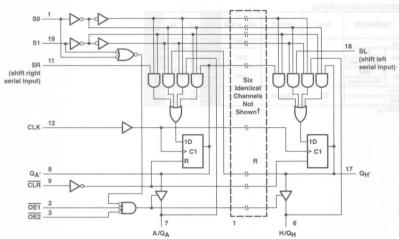
Shift Left

Load Data

- Operate with Outputs Enabled or at High Impedance
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for n-Bit Word Lengths

# | MAX or MIV | 1.5 | AS | 1.5 | LNUT | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX | MAX

#### **Logic Diagram**



† I/O ports not shown: B/QB (13), C/QC (6), D/QD (14), E/QE (5), F/QF (15), and G/QG (4).

									ONOTH	MA IND	las bes							
				INP	JTS				I/O PORTS								OUTPUTS	
MODE	CLR	S1	S0	OE1†	OE2†	CLK	SL	SR	A/Q A	B/Q B	C/Q C	D/Q D	E/Q E	F/Q F	G/Q G	H/Q H	QA'	QH
Clear	L	X L H	X	L	L	X X	X X	X	L	L	L	L	L	L	L L X	L X	L	L
Hold	H	L	L	L	L	X	X	X	Q AO Q AO	Q B0 Q B0	Q C0 Q C0	Q D0 Q D0	Q E0 Q E0	QF0 QF0	Q G0 Q G0	Q <sub>H0</sub> Q <sub>H0</sub>	Q AO Q AO	Q H
Shift Right	H	L	H	L	Ł	Ť	X	H	H	Q An Q An	Q <sub>Bn</sub> Q <sub>Bn</sub>	Q Cn Q Cn	Q Dn Q Dn	Q En Q En	QFn QFn	Q Gn Q Gn	e de H	QG
Shift Left	H	H	L	L	L	<b>†</b>	H	X	Q Bn Q Bn	Q Cn Q Cn	Q Dn Q Dn	Q En Q En	Q Fn Q Fn	Q Gn Q Gn	Q Hn Q Hn	H	Q <sub>Bn</sub> Q <sub>Bn</sub>	L
Load	H	H	H	×	X	1	X	X	a	h	C	d	e	f	0	h	а	h

NOTE: a...h=the level of the steady-state input at inputs A through H, respectively. This data is loaded into the flip-flops while the flip-flop outputsare isolated from the I/O terminals.

† When one or both output-enable inputs are high, the eight I/O terminals are disabled to the high-impedance state; however, sequential operationor clearing of the register is not affected.

#### RECOMMENDED OPERATING CONDITIONS

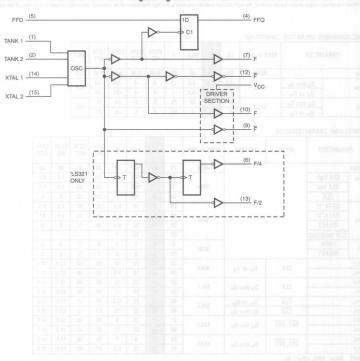
F	PARAMETER	MAX or MIN	LS	S	ALS	F	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
lec		MAX	53	225	40	95	0.16	0.16	0.16	0.16	mA
la	Q <sub>A</sub> thru Q <sub>H</sub>	MAX	-2.6	-6.5	-2.6	-3	-6	-4	-24	-24	
Іон	QA or QH	MAX	-0.4	-0.5	-0.4	1	-4	-4	-24	-24	mA
lou	Q <sub>A</sub> thru Q <sub>H</sub>	MAX	24	20	24	- 24	6	4	24	24	A
IOL	QA' or QH'	IVIAX	8	6	8	- 20	4	4-	24	24	mA

#### SWITCHING CHARACTERISTICS

F	PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	- F	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
fma)	(		- 60	MIN	20	50	30	70	20	16	95	90
tw	CLK high			74	30	10	16.5	7	24	30	5.2	5.5
	CLK low			MIN	10	10	16.5	7	24	30	5.2	5.5
	CLR DATA "H" -DATA "L" SELECT CLR INACTIVE DATA SELECT				20	10	10	7	15	22	5	5
	DATA "H"			M	20	7	16	5.5	36	30	4.5	4.5
tsu	-DATA "L"			MIN	20	5	6	5.5	36	- 30	4.5	4.5
tsu	SELECT			IVIIN	35	15	20	8.5	36	41	9	9
	CLR INACTIVE				20	10	15	7		-	-	-
th	DATA			MIN	0	5	0	2	0	0	0	0
LI I	SELECT			IVIIIV	10	5	- 0	0	0	0	0	0
tPLH		CLV	00	MAX	33	20 -	-15	10	60	68	12.9	12.9
tPHL.		CLK	QA. or QB.	IVIAA	39	20	- 18	9.5	60	68	12.9	12.9
tPLH		CLV	0 1 0	MAX	25	21	13	10	60	68	13.5	14.5
tPHL		CLK	Q <sub>A</sub> thru Q <sub>H</sub>	IVIAX	39	21	19	12	60	68	13.5	14.5
tPHL	5	CLR	QA or QH	MAX	40	21	22	10.5	60	69	11.2	12.2
tPHL.		CLR	Q <sub>A</sub> thru Q <sub>H</sub>	MAX	40	24	22	15	60	69	13.9	18.6
tPZH	->:	051 050	0 11 0	MAX	21	18	16	9	47	48	14.9	14.9
tPZL		UET, UEZ	Q <sub>A</sub> thru Q <sub>H</sub>	IVIAA	30	18	22	11	39	45	14.9	14.9
tPHZ		0E1 0E2	0. 45 0	MAX	20	12	8	7	56	-56 -	14.9	14.9
tPLZ		UE1, UE2	Q <sub>A</sub> thru Q <sub>H</sub>	IVIAX	15	12	15	6.5	47	-48	14.9	14.9

#### CRYSTAL-CONTROLLED OSCILLATOR

- Crystal-Controlled Oscillator Operation from 1MHz to 20MHz
- Complementary Outputs

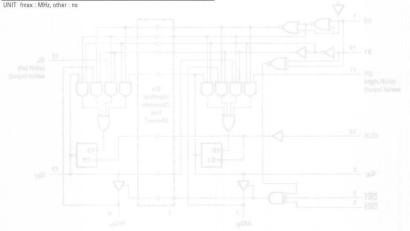


#### RECOMMENDED OPERATING CONDITIONS

TEOO!	ADED OF EINTERING GOT		***************************************	
-	PARAMETER	MAX or MIN	LS	UNIT
lcc		MAX	75	mA
	F' or F'	MAX	-24	mA
Іон	F, F, F/2, F/4	MAX	-0.4	mA
	F' or F'	MAX	24	mA
lor	F F F/2 F/4	MAX	8	mA

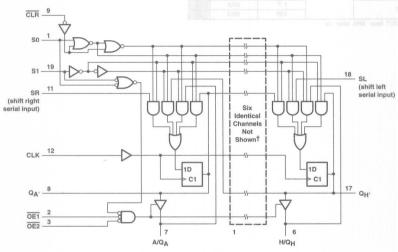
#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
		F/2	MIN	10
fmax		F/4	MAX	5
		ANY	MIN	20
		F',F'	MAX	14
tr		ANY	MAX	40
		F',F'	MAX	10
tf		ANY	MAX	20



- Hold (Store) Shift Right Shift Left Load Data
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for n-Bit Word Lengths

### **Logic Diagram**



† I/O ports not shown: B/QB (13), C/QC (6), D/QD (14), E/QE (5), F/QF (15), and G/QG (4).

				INF	UTS				VO BORD								OUTPUTS	
MODE	CLR	SEL	ECT		TROL	CLK	SEREAL	A/Q <sub>A</sub>	B/QB	C/QC	c/QD	C/QE	C/QF	C/QG	H/QH	Q <sub>A</sub> ·	QH'	
		SR																
Clear	L	X	L	L	L	1	X	X	L	L	L	L	a L	an El o	wit[]	et Lahr	) des	L
Clear	L	L	X	L	L	1	X	X	L	L	L	L	L	L	L	L	L	L
*****	Н	L	L	L	L	X	X	X	QAO	QAO	QCO	QDO	QE0	QFO	QG0	QHO	QAO	QHO
Hold	H	X	×	L	L	L	X	X	QAO	Q <sub>B0</sub>	QCO	Q <sub>D0</sub>	QE0	QF0	Q <sub>G</sub> 0	QHO	QAO	QHO
Shift	Н	L	H	L	L	1	X	н	Н	QAn	QBn	QCn	Qpn	QEn	QFn	QGn	Н	QGn
Right	H	L	H	L	L	Ť.	X	L	L	QAn	QBn	QCn	QDn	QEn	QFn	QGn	L	QGn
Shift	Н	Н	L	L	L	<b>†</b>	H	X	QBn	QCn	QDn	QEn	QFn	QGn	QHn	Н	QBn	Н
Left	Н	H	L	L	L	1	L	X	QBn	QCn	QDn	QEn	QFn	QGn	QHn	L	QBn	L
Load	Н	Н	. Н	X	X	1	X	X	a	b	C	d	е	f	q	h	а	h

<sup>†</sup> a ...h=the level of the steady-state input at inputs A through H, respectively. This data is loaded into the flip-flops while the flip-flop outputsare isolated from the I/O terminals.

#### RECOMMENDED OPERATING CONDITIONS

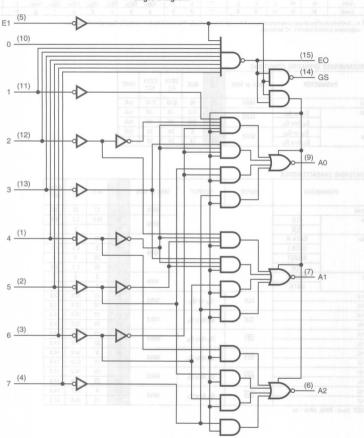
PARAMETER		MAX or MIN	LS	ALS	CD74 AC	CD74 ACT	UNIT
Icc		MAX	225	40	0.16	0.16	mA
1он	QA or QH	MAX	-0.5	-0.4	-24	-24	mA
	Q <sub>A</sub> thru Q <sub>H</sub>	IVIAA	-6.5	-2.6	-24	-24	mA
lor.	QA' or QH'	MAY	6	8	24	24	mA
IUL	Q <sub>A</sub> thru Q <sub>H</sub>	MAX	20	24	24	24	mA

#### SWITCHING CHARACTERISTICS

P.A	ARAMETER	INPUT	INPUT OUTPUT		LS	ALS	CD74 AC	CD74 ACT
fmax			-1.0	MIN	25	17	95	90
tw	CLK			MIN	30	16.5	5.2	5.5
	CLR			IVITIV	20	-	5	5
tsu	DATA H				20	16	4.5	4.5
	DATA L			14141	20	6	4.5	4.5
	SELECT			MIN		20	9	9
	CLR			-0		20	5.5	5.5
th	SELECT			MIN		0	0	0
	DATA			MIN	0	0	0	0
tPLH		CLK		1444	33	15	12.9	12.9
tPHL		CLK	Q <sup>A,</sup> or Q <sup>B,</sup>	MAX	39	18	12.9	12.9
tPLH .		CLK	0 1 0	MAX	25	13	13.5	14.5
<b>TPHL</b>		CEK	Q <sub>A</sub> thru Q <sub>H</sub>	MAX	39	19	13.5	14.5
tPZH		0E1		MAN	21	16	14.9	14.9
tPZL.		UEI	Q <sub>A</sub> thru Q <sub>H</sub>	MAX	30	22	14.9	14.9
tPHZ		0E1	0 11 0	EARY	20	8	14.9	14.9
tPLZ		UEI	Q <sub>A</sub> thru Q <sub>H</sub>	MAX	15	15	14.9	14.9
PZH		050		MANY	21	16	14.9	14.9
tPZL	(9)	0E2	Q <sub>A</sub> thru Q <sub>H</sub>	MAX	30	22	14.9	14.9
tPHZ	SA	0E2	0 1 0	MANY	20	8	14.9	14.9
tPLZ		UE2	Q <sub>A</sub> thru Q <sub>H</sub>	MAX	15	15	14.9	14.9

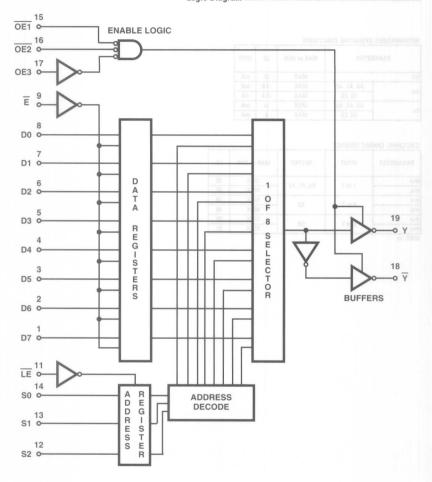
#### **8-LINE TO 3-LINE PRIORITY ENCODER**

- 3-State Outputs Drive Bus Lines Directly
- Encodes 8 Data Lines to 3-Line Binary (Octal)



			IN	PUT	S					0	UTPL	JTS	
E1	0	1	2	3	4	5	6	7	A2	A1	A0	GS	E0
Н	X	X	X	X	X	X	X	X	Z	Z	Z	H	Н
L	H	H	H	H	H	H	Н	H	Z	Z	Z	Н	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	Н
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	Н	H	H	L	L	L	H
L	X	X	L	Н	Н	Н	Н	H	H	L	H	L	Н
L	X	L	Н	Н	H	Н	H	H	H	Н	L	L	H
L	L	Н	Н	Н	Н	Н	H	Н	H	H	Н	L	Н

#### RECOMMENDED OPERATING CONDITIONS PARAMETER MAX or MIN LS UNIT MAX 25 mA MAX A0, A1, A2 -2.6 mA Іон MAX EO, ES -0.4 mA A0, A1, A2 MAX 24 mA EO, ES MAX mA SWITCHING CHARACTERISTICS PARAMETER OUTPUT LS INPUT MAX or MIN tPLH MAX 35 1 to 7 A0, A1, A2 tPHL MAX 35 tPLH MAX 18 0 to 7 E0 tPHL MAX 40 tPLH MAX 55 0 to 7 GS tPHL. MAX 21 UNIT: ns



#### **FUNCTION TABLE (SN74)**

JTH	

		- 1	NPUTS	6				
SELECT		DC		UTPI	OUTPUTS			
S2	S1	S0		G1	G2	G3	W	Υ
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	Н	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	L	L	L	H	D0	D0
L	L	L	H	L	L	Н	D0n	D0n
L	L	Н	L	L	L	H	D1	D1
L	L	H	H	L	L	Н	D1 <sub>n</sub>	D1 <sub>n</sub>
L	H	L	L	L	L	H	D2	D2
L	H	L.	H	L	L	H	D2 <sub>n</sub>	D2n
L	H	H	L	L	L	H	D3	D3
L	Н	H	H	L	L	H	D3 <sub>n</sub>	D3 <sub>n</sub>
H	L	L	L	L	L	H	D4	D4
H	L	L	H	L	L	H	D4 <sub>n</sub>	D4 <sub>n</sub>
H	L	H	L	L	L	H	D5	D5
Н	L	H	H	L	L	H	D5 <sub>n</sub>	D5 <sub>n</sub>
Н	H	L	L	L	L	H	D6	D6
Н	H	L	H	L	L	H	D6 <sub>n</sub>	D6 <sub>n</sub>
Н	H	H	L	L	L	H	D7	D7
Н	Н	Н	Н	L	L	Н	D7n	D7 <sub>n</sub>

			INPUTS					
SE	LECT (NOT	E 3)	ENABLE DATA	оит		ARRIVE	OUT	PUTS
S2	S1	S0	Ē	OE1	OE2	OE3	Ÿ	Y
X	X	X	X	Н	×	Х	Z	Z
Х	X	Х	X	X	Н	×	Z	Z
Х	X	X	×	X	×	L	Z	Z
L	III FIRE	ill bib	L	L	L	Н	D0	D0
L	L	L	Н	L	L	Н	D0n	D0n
L	L	Н	L	L	L	Н	D1	D1
L	L	Н	н	ndn:	L	н	D1n	D1 <sub>r</sub>
L	Н	L	L	L	L	Н	D2	D2
L	Н	L	Н	L	L	Н	D2 <sub>n</sub>	D2 <sub>n</sub>
L	Н	Н	L	L	L	н	D3	D3
L	Н	Н	Н	L	L	Н	D3 <sub>n</sub>	D3 <sub>r</sub>
Н	L	L	L	L	L	Н	D4	D4
Н	L	L	Н	L	L	Н	D4n	D4r
Н	L	Н	L	L	L	н	D5	D5
Н	L	Н	Н	L	L	Н	D5 <sub>n</sub>	DnS
н	Н	L	L	L	L	Н	D6	D6
						- 11	=	-

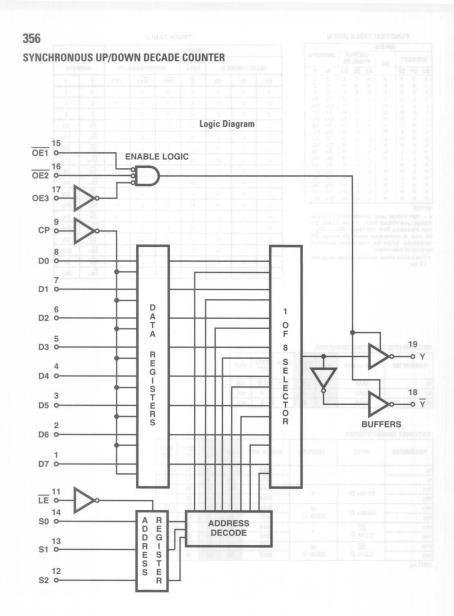
† This column shows the input address setup with LE low.

RECOMMENDED OPERATING CONDITIONS

			-	_		_
PARAMETER	MAX or MIN	LS	SN74 HC	CD74 HC	SN74 HCT	UNIT
Icc	MAX	46	0.08	0.16	0.16	mA
Іон В	MAX	-2.6	-6	-6	-4	mA
lou	MAX	24	6	6	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	SN74 HC	CD74 HC	SN74 HCT
tsu			MAX	15	19	15	15
th			MAX	15	5	14	14
tPLH	D0.45 D7	Υ	MAX	36	59	63	71
tPHL .	D0 thru D7	4	MAX	35	59	63	71
tPLH .	D0 45 D7	W	MAX	27	59	63	71
tPHL .	D0 thru D7	(CD74: Y)	MAX	44	59	63	71
tPLH	DC	γ	MAX	42	68	75	81
tphl.	(CD74: E)	1	MAX	39	68	75	81
tPLH	DC	W	MAX	33	68	75	81
tPHL	(CD74: E)	(CD74: Y)	MAX	50	68	75	81



# FUNCTION TABLE (SN74)

			INPUTS				
SE	SELECT		CLK	OUTPUT			OUTPUTS
C2	C1	CO		G1	G2	G3	WY
X	X	X	X	Н	X	X	Z Z
X	X	X	X	X	H	X	Z Z
X	X	X	X ↑	X	X	L	Z Z
L	L	L	1	L	L	Н	D0 D0
L	L	L	HorL	L	L	H	Don Don
L	L	H	1	L	L	H	D1 D1
L	L	Н	HorL	L	L	H	D1 <sub>n</sub> D1 <sub>n</sub>
L	H	L	1	L	L	H	D2 D2
L	H	L	HorL	L	an Line	H	D2 <sub>n</sub> D2 <sub>n</sub>
L	H	H	1	L	L	H	D3 D3
L	H	H	HorL	L	L	H	D3 <sub>n</sub> D3 <sub>n</sub>
Н	L	L	1	L	L	H	D4 D4
H	L	L	HorL	L	L	H	D4n D4n
Н	L	H	1	L	L	Н	D5 D5
H	L	H	HorL	L	L.	Н	D5 <sub>n</sub> D5 <sub>n</sub>
H	H	L	1	L	L	H	D6 D6
H	H	L	HorL	L	L	H	D6 <sub>n</sub> D6 <sub>n</sub>
H	H	Н	1	L	L	Н	D7 D7
Н	H	Н	HorL	L	L	H	D7 <sub>n</sub> D7 <sub>n</sub>

NOTIES: H= High Voltage Level (Steady State), L = Low Voltage Level (Steady State),  $\tilde{T}$  = Transition form Low to High Level, X = Dornt Care, Z = High Impedance State (Off State),  $Do_1$ , ...  $Dr_1$  = the level of steady-state inputs D0 through D7, respectively, before the most recent low-to-high transition of data control.

† This column shows the input address setup with LE low.

# TRUTH TABLE

			INPUT	S			0.000		
SELI	ECT (NOT	E 3)	сьоск	OUTP	UT ENABL	.ES	OUTPUTS		
52	S1	S0	CP	OE1	OE2	OE3	Ÿ	Υ	
X	Х	Х	×	Н	X	Х	Z	Z	
X	Х	X	×	Х	н	×	Z	Z	
X	X	X	×	Х	×	L	Z	Z	
L	L	L	1	L	L	Н	D0	D0	
L	L	L	HorL	L	L	Н	D0n	D0 <sub>f</sub>	
L	L	H	1	L	L	H	D1	D1	
L	L	Н	H or L	L	L	Н	D1 <sub>n</sub>	D1	
L	Н	L	Ť	L	L	Н	D2	D2	
L	Н	L	H or L	L	L	Н	D2 <sub>n</sub>	D2	
L	Н	Н	2510	anyae.	L	Н	D3	DS	
L	Н	Н	H or L	JH L	L	Н	D3 <sub>n</sub>	D3	
н	LAm	L	0110	30 L	IS L	Н	D4	D4	
Н	L	L	HorL	ō L	L	Н	D <sub>4</sub> n	D4	
Н	L	Н	1	° L	L	Н	D5	DS	
Н	L	Н	H or L	L	L	Н	D5 <sub>n</sub>	D5	
Н	Н	L	1	L	L	Н ,	D6	De	
Н	н	L	HorL	L	L	Н	D6n	D6	

# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	SN74 HC	CD74 HCT	UNIT
lcc	MAX	46	0.08	0.16	mA
Іон	MAX	-2.6	-6	-4	mA
lou	MAX	24	6	4	mA

# SWITCHING CHARACTERISTICS

OTTITO OTTA	IIAGTEMOTIO				1	
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	SN74 HC	CD74 HCT
tsu	D0 th	ru D7	MIN	15	19	11
th	D0 th	ru D7	MIN	0	5	14
tPLH .	CLK	Υ	MAX	27	64	77
tPHL .	CLK	Y.	WAX	50	64	77
tPLH	OLK	W	MAN	36	64	77
tphl .	CLK	(CD74: Y)	MAX	27	64	77
tPLH .	00 01 00	Y	MAX	45	71	89
tphl .	S0, S1, S2	4	IVIAX	48	71	89
tPLH	00 04 00	W	MANY	54	71	89
tPHL .	S0, S1, S2	(CD74: Y)	MAX	45	71	89



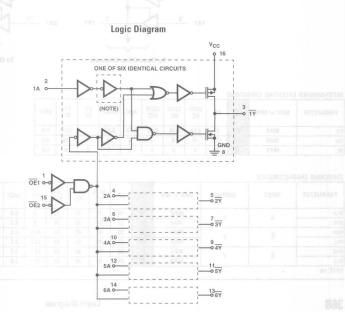
RECOMMENDED OPERATING CONDITIONS

	511-10000000000000000000000000000000000			_	_	_	
PARAMETER	MAX or MIN	ΠL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
lcc so	MAX	85	24	0.08	0.16	0.16	mA
Тон	MAX	-5.2	-2.6	-6	-6	-4	mA
lou	MAX	32	24	6	6	4	mA

SWITCHING CHARACTERISTICS

SWITCHING CHAR								
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
tPLH .		- v	MAX	16	15	24	32	38
tPHL .	A	1	MAX	22	18	24	32	38
tPZH	G	V	MAX	35	35	48	45	53
tPZL	G	Y	MAX	37	45	48	45	53
tPHZ	-	v	MAX	11	32	48	45	53
tPLZ	G	Y	MAX	27	35	48	45	53

# HEX BUS DRIVERS HEX BUFFERS/LINE DRIVERS 3-STATE



NOTE: Inverter not included in HC/HCT365.

FIGURE 1. LOGIC DIAGRAM FOR THE HC/HCT365 AND HC366 (OUTPUTS FOR HC/HCT365 ARE COMPLEMENTS OF THOSE SHOWN, i.e., 1Y, 2Y, ETC.)

# **FUNCTION TABLE**

	INPUTS		OUTPUT
G1	G2	A	Y
L	L	L	Н
L	L	H	L
X	H	X	Z
Н	X	X	Z

NOTES: H = High Voltage Level L = Low Voltage Level X = Don't Care

Z = High Ompedance (OFF) State

# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	UNIT
Icc	MAX	77	21	0.08	160	mA
Іон	MAX	-5.2	-2.6	-6	-6	mA
loL	MAX	32	24	6	6	mA

# SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC
tPLH III	A	Mary You Market	MAX	17	15	24	33
tPHL .	A	(CD74: Y)	MAX	16	18	24	33
tPZH	G	Y	MAX	35	35	48	45
tPZL E	(CD74: OE)	(CD74: Y)	MAX	37	45	48	45
PHZ	G	Y	MAX	11	32	48	45
tPLZ III	(CD74: OE)	(CD74: Y)	MAX	27	35	48	45

# **HEX BUS DRIVERS**



# To Three Other Channels

To One Other Channel

# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	AHC	AHCT	LV 3V	LV 5V	UNIT
Icc	MAX	85	24	0.08	0.16	0.16	0.04	0.04	- 3	0.02	mA
Іон	MAX	-5.2	-2.6	-6	-6	-4	-8	-8	-8	-16	mA
lou	MAX	32	24	6	6	4	8	8	8	16	mA

# SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	AHC	AHCT	LV 3V	LV 5V
tPLH .		V	MAX	16	16	24	32	38	9	6.5	13.5	9
tphl.	A	YE o	MAX	22	22	24	32	38	9	6.5	13.5	9
tPZH	G	.,	MAX	35	35	48	45	53	10.5	9.5	16	10.5
tPZL	G	Y	MAX	47	40	48	45	53	10.5	8.5	16	10.5
tPHZ	G	v	MAX	11	30	48	45	53	10.5	9.5	15.5	10.5
tPLZ	G	Y	MAX	27	35	48	45	53	10.5	8.5	15.5	10.5

# 368

# Logic Diagram

# **HEX BUS DRIVERS**



# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
Icc	MAX	77	21	0.08	0.16	0.16	mA
Іон	MAX	-5.2	-2.6	-6	-6	-4	mA
lou	MAX	32	24	6	6	4	mA

# SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
tPLH C	THE THE	2 KAM	MAX	17	15	24	32	45
tPHL .	А	200	MAX	16	18	24	32	45
tPZH	G	V	MAX	35	35	48	45	53
tPZL	G	AAM.	MAX	37	45	48	45	53
tPHZ	=		MAX	11	32	48	45	53
tPLZ	G	Y	MAX	27	35	48	45	53

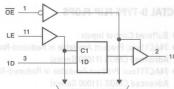
# **OCTAL D-TYPE LATCHES**

- 3-State Bus-Driving True Outputs
- Buffered Control Inputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

# **FUNCTION TABLE**

OUTPUT	INPL	JTS	OUTPUT
CONTROL	LE	D	Q
L	Н	Н	Н
L	H	L	L
L	L	X	QO
H	X	X	Z

# Logic Diagram



To Seven Other Channels

#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH	UNIT
Icc	MAX	40	190	27	100	55	0.08	0.16	0.08	0.16	60	30	5	mA
Іон	MAX	-2.6	-6.5	-2.6	-15	-3	-6	-6	-6	-6	-15	-32	-32	mA
lor	MAX	24	20	24	48	24	6	6	6	6	64	64	64	mA

PARAMETER	MAX or MIN	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	SV TVC	ALVCH 3V	UNIT
Icc	MAX	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	200	0.02	0.01	0.02	mA
Іон	MAX	-24	-24	-24	-24	-24	-24	-8	-8	-8	-16	-24	-24	mA
lou	MAX	24	24	24	24	24	24	8	8	8	16	24	24	mA

#### SWITCHING CHARACTERISTICS

PAF	AMETER	INPUT	ОИТРИТ	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTF
tw	High	20 24	25 05	MIN	15	6	10	4.5	6	20	24	25	24	7.5	3.3	3
	Low			MIN	15	7.3	-	105.1	-	- 3			-	12.0		-
tsu	40			MIN	5	0	10	2	2	13	15	13	20	2	1.9	1.1
th				MIN	20	10	7	3	3	12	5	10	15	5.5	1	1.4
tPLH .	100	D.	0	MAX	18	12	12	6	8	38	45	44	48	9.3	5.9	3.9
tPHL.		U	u	MAX	18	12	16	6	- 6	38	45	44	48	9.5	6.2	3.9
tPLH .	100	LE	0	MAX	30	14	22	11.5	13	44	53	44	53	9.3	6.6	4.2
tPHL .	1000	LE	u	MAX	30	18	23	7.5	- 8	44	53	44	53	8.8	7.2	4.2
tPZH		ŌĒ	0	MAX	28	15	18	6.5	12	38	45	44	53	11.8	5.2	4.8
tPZL		UE	u	MAX	36	18	20	9.5	8.5	38	45	44	53	12	6.7	4.8
tPHZ		ŌĒ	0	MAX	25	9	10	6.5	7.5	38	45	44	53	7	6.9	4.6
tPLZ		UE	u	MAX	20	12	12	7	6	38	45	44	53	7.4	6.5	4.5

PAR	RAMETER	INPUT	OUTPUT	MAX or MIN	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC:
tw	High	27 1 12	1 10	MIN	4	4.5	4	5	8	4	5	6.5	5	5	3.3	3.3
1.0	Low			MIN			4	MAN	-	4		-	-	2 33	ч.	-
tsu				MIN	3.5	4.5	2	3.5	8	2	4	1.5	4	4	2	0.5
th	5 1			MIN	2	1	3	3.5	1	3	1	3.5	1	1	1.5	1.2
tPLH		D		MAX	10.3	10.5	8.5	11.8	11.5	10.4	10.5	10.5	17	10.5	6.8	3.6
tPHL	611	CHI DE LY	0 0	MAX	8.4	10.5	8.5	10	11.5	10.4	10.5	10.5	17	10.5	6.8	3.6
tPLH .		LE	Q	MAX	11.3	10.5	12	13	11.5	12.5	10.5	14.5	16.5	10.5	7.6	3.3
tPHL .		all real	u.	MAX	10.2	10.5	12	12.2	11.5	12.5	10.5	14.5	16.5	10.5	7.6	3.3
tPZH	41	ŌĒ	0	MAX	10.8	9.5	10.5	12.5	10.5	13.5	11.5	13.5	17	11.5	7.7	4.8
tPZL	91	UE	u u	MAX	9.7	9.5	10.5	12	10.5	13.5	11.5	13.5	17	11.5	7.7	4.8
tPHZ		ŌĒ	0	MAX	11.1	12.5	11.5	12.2	12.5	12.5	10.5	12	15	10.5	7	4.4
tPLZ		UE	u	MAX	8.7	10	11.5	10.1	10	12.5	10.5	12	15	10.5	7	4.4

UNIT fmax : MHz, other : ns

 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



#### **FUNCTION TABLE**

OUTPUT	INPL	JTS	OUTPUT
CONTROL	CLK	D	Q
L	1	Н	H
L	1	L	L
L	L	×	Q0
H	X	X	Z

#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH 3V	UNIT
Icc	MAX	40	160	31	128	86	0.08	0.16	0.08	0.16	60	30	5	mA
Іон	MAX	-2.6	-6.5	-2.6	-15	-3	-6	-6	-6	-6	-15	-32	-32	mA
lou.	MAX	24	20	24	48	24	6	6	6	6	64	64	64	mA

PARAMETER	MAX or MIN	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVCH 3V	UNIT
lcc	MAX	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.01	0.01	mA
Іон	MAX	-24	-24	-24	-24	-24	-24	-8	-8	-8	-16	-24	-24	mA
lou	MAX	24	24	24	24	24	24	8	8	8	16	24	24	mA

# SWITCHING CHARACTERISTICS

PAF	RAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH 3V
fmax				MIN	35	75	35	125	70	24	20	25	20	70	150	150
tw	High			MIN	15	6	14	4	7	20	24	20	24	7	3.3	3.3
-	Low			MIN	15	7.3	14	3	6	20	24	20	24	9703	3.3	3.3
tsu	11 2			MIN	20	5	10	2	2	25	18	25	18	6.5	1.9	1.5
th	1 1 00	10 01		MIN	0	2	0	2	2	5	- 5	10	5	0	2.1	0.8
tPLH		CLK	0	MAX	28	15	12	8	10	45	50	45	50	10.6	6.2	4.5
tPHL		CLK	5 U S.	MAX	28	17	16	9	10	45	50	45	50	10	7.1	4.2
tPZH	0.6	OF	0	MAX	26	15	17	6	12.5	38	45	38	42	12.3	5.2	4.7
tPZL	7.4	OE 4	u u	MAX	28	18	18	10	8.5	38	45	38	42	12.7	6.7	4.7
tPHZ	1.6	OF.	88 0.88	MAX	28	9	10	6	8	38	41	38	45	6.8	6.7	4.6
tPLZ		OE H	u u	MAX	20	12	18	6	6.5	38	41	38	45	6.8	6.5	4.5

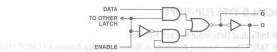
PAF	RAMETER	INPUT	OU	TPUT	MAX or MIN	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	3V	ALVCH 3V
fmax	VIII VE	T WE		FRA	MIN	95	100	12.5	55	90	110	75	75	50	75	100	150
tw	High				MIN	5	4.5	4	9	5	4.5	5	6.5	5.5	5	3.3	3.3
	Low				MIN	5	4.5	4	9	5	4.5	5	6.5	5.5	5	3.3	3.3
tsu	8 8				MIN	2.5	4.5	2	3	5.5	2	3	2.5	4.5	3	2	1.8
th	21111	1 25			MIN	3.5	1.5	2	5.5	1.5	3	2	2.5	2	2	1.5	0.5
tPLH	8.9 8.01	CLK	10.5	03.01	MAX	10.2	10.5	10.8	12.4	11.5	11.2	11.5	11.5	18.5	11.5	7	3.6
TPHL	88 200	CLK	10.5	KIT	MAX	10.1	10	10.8	13	11	11.2	11.5	11.5	18.5	11.5	7	3.6
tPZH	8.5   5.01	ŌĒ	101	0	MAX	9.1	9.5	14.5	12.3	10.5	14.5	11	12.5	16.5	11	7.5	5.2
tPZL	11.6 7.6	231 231		2.51	MAX	9.4	9.5	14.5	12.3	10.5	14.5	11	12.5	16.5	11	7.5	5.2
tPHZ	115 177	0E 281 2.17	217	0.2.87	MAX	11.2	12.5	14.5	13.2	12.5	14.5	10	12	16	10	6.5	4.5
tPLZ	TT BET			U.S.	MAX	9.2	10	14.5	10.8	10	14.5	10	12	16	10	6.5	4.5

# 375

# 4-BIT BISTABLE LATCHES

• Complementary Outputs  $(0, \overline{0})$ 

# Logic Diagram



# **FUNCTION TABLE**

INP	UTS	OUT	PUTS
D	С	(	3
L	H	L	Н
H	H	H	L
X	L	Qo	Q <sub>0</sub>

ogic Diagram

# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	SN74 HC	UNIT
Icc	MAX	12	0.04	mA
Гон	MAX	-0.4	-4	mA
lou	MAX	8	4	mA

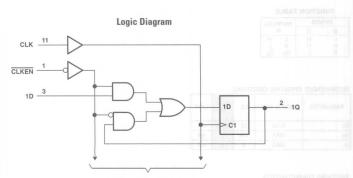
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# SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	SN74
tw			MIN	20	20
tsu			MIN	20	25
th			MIN	0	5
tplH	D	Q	MAX	27	30
tphL	D	u	MAX	17	30
tPLH .	D	ā	MAX	20	30
tphL .	U	u	MAX	15	30
tPLH .	0	0	MAX	27	33
tPHL .	С	Q	MAX	25	33
tPLH .	С	ā	MAX	30	33
tphL .	U	u	MAX	15	33

# OCTAL D-TYPE FLIP-FLOPS

- Individual Data Input to Each Flip-Flop
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



To Seven Other Channels

**FUNCTION TABLE** 

	INPUTS		OUTI	PUTS
CLKEN	CLOCK	DATA	Q	ā
Н	X	X	Qn	Qn
L	1	H	H	L
L	1	L	L	H
X	L	X	Q <sub>0</sub>	Qo

RECOMMENDED OPERATING CONDITIONS

RECOMMENDED	OPERATING CON	DITIONS		_	_		,		,	
PARAMETER	MAX or MIN	LS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	AC 11	UNIT
Icc	MAX	28	90	0.08	0.16	0.08	0.16	30	0.08	mA
Іон	MAX	-0.4	-1	-4	-4	-4	-4	-32	-24	mA
Ini	MAX	8	20	4	4	4	4	64	24	mΔ

SWITCHING CHARACTERISTICS

	PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	AC 11
fmax				MIN	30	110	20	20	17	16	150	100
tw				MIN	20	5	25	24	25	30	3.3	5
tsu	DATA			MIN	20	2	25	18	15	18	2.5	4
	CLKEN ACTIVE			MIN	25	2.5	25		15	-	3	6
	CLKEN INACTIVE			MIN	10	4.5	25	18	15	18	3	6
th				MIN	5	1	5	3	3	3	1.8	0
tPLH		CLK	Q	MAX	27	10	40	53	45	57	6.5	11.3
tPHL		CLK	u u	MAX	27	10.5	40	53	45	57	7.3	12.9

UNIT fmax: MHz, other: ns

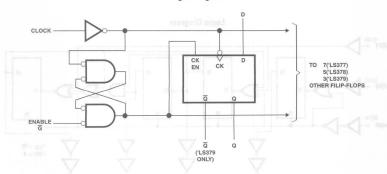


All Have Direct Clear for Each 4-Bit Counter

W WILLIAMS DIEGL CISSLES FOR ESCHAPER COUNTS!

Buffured Outputs Reduce Possibility of Collect

Logic Diagram



**FUNCTION TABLE** 

	INPUTS		OUT	PUTS
G	CLOCK	DATA	Q	Q
Н	X	X	Qo	Qo
L	1	H	H	L
L	1	L	L L	H
X	L	X	Qn	Q

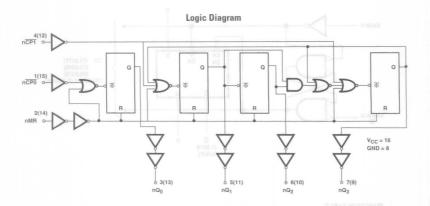
RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	F	SN74 HC	UNIT
Icc	MAX	22	45	0.08	mA
Іон	MAX	-0.4	-1	-4	mA
lou	MAX	8	20	4	mA

SWITCHING CHARACTERISTICS

	PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	F	SN74 HC
fmax	W 110	05 20	2010	MIN	30	110	20
tw	CLK H			MIN	20	4	25
Ter.	CLK L			MIN	20	6	25
tsu	DATA			MIN	20	5	25
88	G ACTIVE			MIN	25	3.5	25
51	G INACTIVE			MIN	10	5	25
th	74			MIN	5 ↑	0	5
tPLH	To part of the same	CLK	XAM o	MAX	27	6.7	40
tPHL	12 7 6 6	ULK	u u	MAX	27	6.1	40
UNIT	fmax : MHz, other : r	IS	XAW	0	HERY	A	***************************************

- Typical maximum Count Frequency: 35MHz
- Buffered Outputs Reduce Possibility of Collector Commutation



FUNCTION TABLE
BCD COUNT SEQUENCE

COUNT	OUTPUTS								
COUNT	QD	QC	QB	QA					
0	L	L	L	L					
1	L	L	L	H					
2	L	L	Н	L					
3	L	L	H	H					
4	L	H	L	L					
5	E	H	L	H					
6	L	H	H	L					
7	L	H	H	H					
8	Н	L	L	L					
9	H	L	L	H					

DI GUINA DV

	1-00	HAMI		
COLUNIT		OUT	PUTS	
COUNT	QA	QD	QC	QB
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
2 3 4 5 6	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	Н	H	L	L

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
Icc	MAX	69	26	0.08	0.16	0.16	mA
Іон	MAX	-0.8	-0.4	-4	-4	-4	mA
lou	MAX	16	8	4	4	4	mA

# SWITCHING CHARACTERISTICS

PAF	RAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
		А	QA	MIN	25	25	25	20	18
fmax		В	QB	MIN	20	12.5	25	20	18
tw	A			MIN	20	20	20	24	29
	В			MIN	25	40	20	24	29
	CLR H			MIN	20	20	20	15	20
tsu				MIN	25	25	5	31/2/11	
tPLH			0.4	MAX	20	20	30	53	60
tphL.		A	AD MA	MAX	20	20	30	53	60
tPLH .			0.0	MAX	60	60	72		126
tPHL.		A	oc.	MAX	60	60	72	W.,	126
tPLH			OB	MAX	21	21	33	56	65
tPHL		В	QB	MAX	21	21	33	56	65
tPLH .			0.0	MAX	39	39	46	74	83
tPHL .		В	30 1	MAX	39	39	46	74	83
tPLH		n .	AAM	MAX	21	21	33	54	63
tPHL		В	XAM QD	MAX	21	21	33	54	63
tPHL		CLR	Q	MAX	39	39	41	57	63

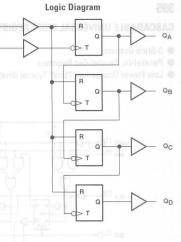
UNIT fmax : MHz, other : ns

# DUAL 4-BIT BINARY COUNTERS

- Dual 4-Bit Binary Counter with Individual Clock
- All Have Direct Clear for Each 4-Bit Counter
- Typical maximum Count Frequency: 35MHz
- Buffered Outputs Reduce Possibility of Collector Commutation

# FUNCTION TABLE

COUNT		INP	UTS	
COUNT	QD	QC	QB	QA
0	L	L	L	L
-1	L	L	L.	H
1 2	L	L	H	L
3	L	L	H	H
4	L	Н	L	L
5	L	Н	L	H
6 7	L	Н	H	L
7	L	Н	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	Н	Н	H	H



RECOMMENDED OPERATING CONDITIONS

NECOMMENDED	OF ENATING CON	DITIONS							
PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
Icc	MAX	64	26	0.08	0.16	0.16		0.02	mA
Іон	MAX	-0.8	-0.4	-4	-4	-4	-6	-12	mA
lor.	MAX	16	8	4	4	4	6	12	mA

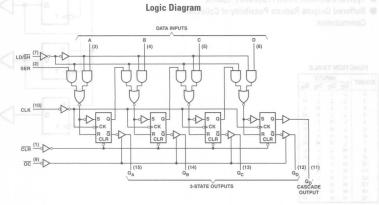
SWITCHING CHARACTERISTICS

PAI	RAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V
fmax			-	MIN	25	25	25	20	18	35	75
tw	Α			MIN	20	20	20	24	29	5	5
	В			MIN	25	40	20	24	29	5	5
	CLR H			MIN	20	20	20	24	24	- 5	5
tsu				MIN	25	25	5	-	-	5	4
tPLH			0.4	MAX	20	20	30	59	48	19	12
tPHL .		А	QΑ	MAX	20	20	30	59	48	19	12
tPLH			0.0	MAX	60	60	72	86	93	26.5	16.5
tPHL		В	QD	MAX	60	60	72	86	93	26.5	16.5
tPHL		CLR	Q	MAX	39	39	41	41	48	18	11.5

UNIT fmax : MHz, other : ns

# **CASCADABLE UNIVERSAL SHIFT REGISTERS**

- 3-State Outputs
- Parallel-In, Parallel-Out Registers
- Low Power Dissipation: 75mW Typical (Enable)



# **FUNCTION TABLE**

	INPUTS									3-STATE OUTPUTS				
CLEAR	LOAD/SHIFT	CLOCK	SERIAL	P	ARA	LLE	L	QA	QB	QC	QD	OUTPUT		
OLLAIT	CONTROL	OLOOK	OLITIAL	Α	В	C	D			-0		QD		
L	X	X	X	X	X	X	X	L	L	L	L	E.		
H	H	H	X	X	X	X	X	QAO	Q <sub>B0</sub>	QCO	Q <sub>D0</sub>	Q <sub>D0</sub>		
H	H	1	X	a	b	C	d	a	b	C	d	d		
H	L	H	X	X	X	X	X	QAO	QBn	Qcn	QDn	QDO		
H	L	1	H	X	X	X	X	H	QAn	QBn	QCn	QCn		
H	L	1	L	X	X	X	X	L	QAn	QBn	QCn	QCn		

Logic Disprom

# RECOMMENDED OPERATING CONDITIONS

	PARAMETER	MAX or MIN	LS	UNIT
Icc		MAX	34	mA
	QA, QB, QC, QD	MAX	-2.6	mA
Іон	OD,	MAX	-0.4	mA
le:	QA, QB, QC, QD	MAX	24	mA
lor	QD'	MAX	8	mA

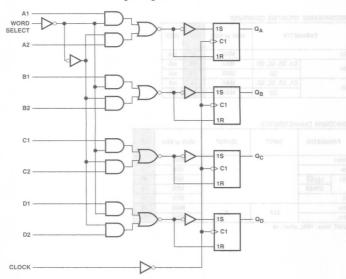
SWITCHING CHARACTERISTICS

PAI	PARAMETER INPUT OUTPUT		MAX or MIN	LS	
fmax		507	- 81	MIN	30
tw				MIN	16
tsu LD/SH				MIN	40
	OTHER			MIN	20
th				MIN	10
tplH	auv o			MAX	30
tPHL		CLK	0	MAX	30

UNIT fmax: MHz, other: ns

WENTS CLOCK OA OB T

# Logic Diagram



FUNCTION TABLE

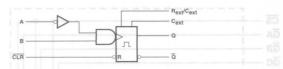
INP		OUT	PUTS		
WORD SELECT	сьоск	QA	QB	QC	QD
L	1	A1	B1	C1	D1
H	1	A2	B2	C2	D2
X	L	QAO	Q <sub>B</sub> 0	QCD	QDO

RECOMMENDED OPERATING CONDITIONS

RECOMMENDED	OPERATING CON	DITION	S
PARAMETER	MAX or MIN	LS	UNIT
Icc	MAX	13	mA
Іон	MAX	-0.4	mA
lou	MAX	8	mA

SWITCHING CHARACTERISTICS

SVVI	TCHING CHARACTER	1131103					
PARAMETER		INPUT	OUTPUT	MAX or MIN	LS		
tw				MIN	20		
tsu	DATA			MIN	25		
	WORD SELECT			MIN	45		
th	DATA			MIN	0		
WORD SELECT				MIN	0		
tPLH tPHL		tPLH .		CLV	0	MAX	27
		CLK	Q.	MAX	32		



COMMON

# **FUNCTION TABLE**

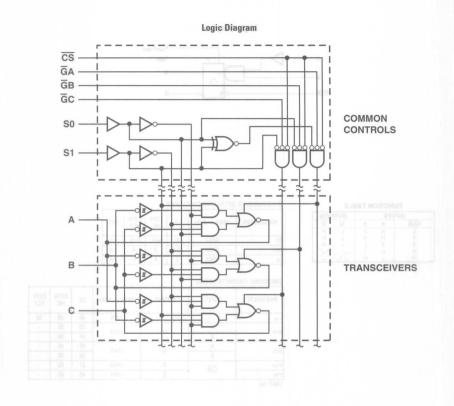
INF	INPUTS			PUTS
CLR	A	В	Q	Q
L	X	X	L	Н
X	H	X	L	H
X	X	L	L	Н
Н	L	1	п	
H	Ī	H	I.L.	7.5

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	CD74 HC	CD74 HCT	UNIT
Icc	MAX	20	0.16	0.16	mA
Іон	MAX	-0.4	-4	-4	mA
lou	MAX	8	4	4	mA

SWITCHING CHARACTERISTICS

SWITCHING CHAN	ACTENISTICS					
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	CD74 HC	CD74 HCT
tw	VE	11111	MIN	40	30	30
tPLH -	Α	0	MAX	33	90	-
	В	u u	IVIAX	44	90	-
	A		MANY	45	96	
tPHL -	В	u	MAX	56	96	-
tPLH	CLR	Q	MAX	27	65	-
tPHL .	CLN	ā	MAX	45	65	



# **FUNCTION TABLE**

			TRANSFERS			
cs	S1	SO	GA	GB	GC	BUSES
Н	X	X	X	X	X	None
X	Н	H	X	X	X	None
X	X	X	Н	H	H	None
X	L	L	X	Н	Н	None
X	L	H	H	X	H	None
X	H	L	Н	H	X	None
L	L	L	X	L	L	$A \rightarrow B, A \rightarrow C$
L	L	H	L	X	L	$B \rightarrow C, B \rightarrow A$
L	H	L	L	L	X	$C \rightarrow A, C \rightarrow B$
L	L	L	X	L	Н	$A \rightarrow B$
L	L	H	H	X	L	$B \rightarrow C$
L	H	L	L	H	X	$C \rightarrow A$
L	L	L	X	H	L	$A \rightarrow C$
L	L	H	L	×	Н	$B \rightarrow A$
L	H	L	H	L	X	$C \rightarrow B$

# RECOMMENDED OPERATING CONDITIONS

TIE O O ITITILE TO C	D OI LIBITINO	00110	T
PARAMETER	MAX or MIN	LS	UNIT
Icc	MAX	95	mA
Іон	MAX	-15	mA
lou	MAX	24	mA

# SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
	A	B or C		
tPLH .	В	A or C	MAX	14
	С	A or B		
	A	B or C		
tPHL	В	A or C	MAX	20
	С	A or B		
	Any G			33
tPZL	S0, S1	A, B, C	MAX	42
	CS			36
tPZH	G, S, CS	A, B, C	MAX	32
tPLZ	G, S, CS	A, B, C	MAX	35
tPHZ	G, S, CS	A, B, C	MAX	25

OCTAL BUFFERS 3-STATE OUTDUTS

IT 62	7 /
A1 2	3 Y1
A2 4	5 Y2
A3 6	7 Y3
A4 8	9 Y4
A5 12	11 Y5
A6 14	13 Y6
A7 16	15 Y7
A8 18	17 Y8

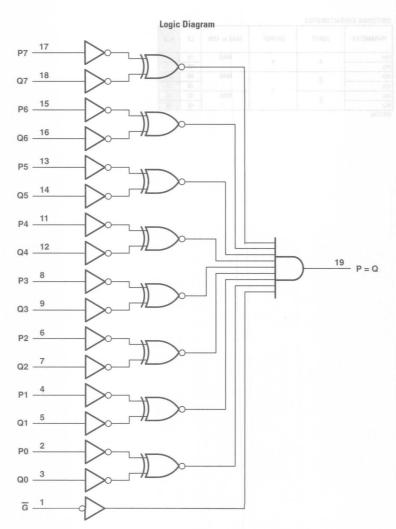
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PARAMETER	MAX or MIN	LS	ALS	UNIT
Icc	MAX	37	33	mA
Іон	MAX	-2.6	-15	mA
lou	MAX	24	24	mA

SWITCHING CHARACTERISTICS PARAMETER INPUT OUTPUT MAX or MIN LS ALS MAX 15 Α Υ 18 12 23 25 10 18 MAX 40 45 40 45 G Υ MAX  $\overline{\mathsf{G}}$ UNIT:ns

# **8-BIT IDENTITY COMPARATOR**

- Open-Collector Outputs
- 20-kΩ Pullup Resistors on Q Inputs



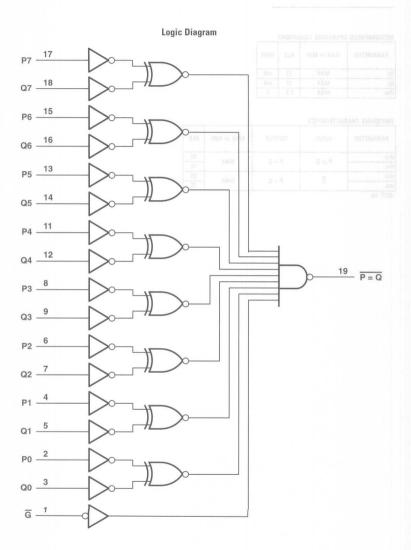
FU					

Т	INF	PUTS	OUTPUT
	DATA P, Q	ENABLE G	P = Q
	P = Q	L	Н
	P > Q	L	L
	P < Q	L	L
	Y	н	Rane

# SOUTH INSULTED COMPARATOR

ZB-KL2 Pullup Hesistors on Ulinputs
 MACT type: Product Available in Reduce

RECOMMENDED	OFENATING CON	T T							
PARAMETER	MAX or MIN	ALS	UNIT						
cc	MAX	17	mA						
DL	MAX	24	mA						
/он	MAX	5.5	V						
WITCHING CHA	RACTERISTICS								
PARAMETER	INPUT	OUT	ГРИТ	MAX or MIN	ALS				
PLH	P or Q	D	= Q	MAX	33				
PHL	roid	E	- u	IVIAA	15				
PLH	G	P	= 0	MAX	33	-			
PHL	, and the second			III.	15				
JNIT: ns									

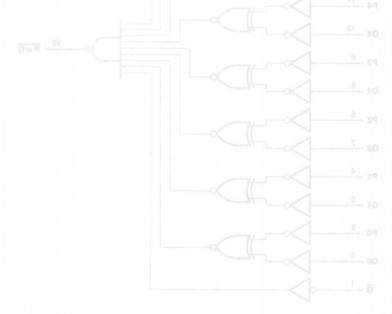


RECOMMENDED	OPERATING CON	DITION	S	
PARAMETER	MAX or MIN	ΔΙς	r.	AC

PARAMETER	MAX or MIN	ALS	F	AC 11	UNIT
Icc	MAX	19	32	8	mA
Іон	MAX	-2.6	-1	-24	mA
lou	MAX	24	20	24	mA

#### SWITCHING CHARACTERISTICS

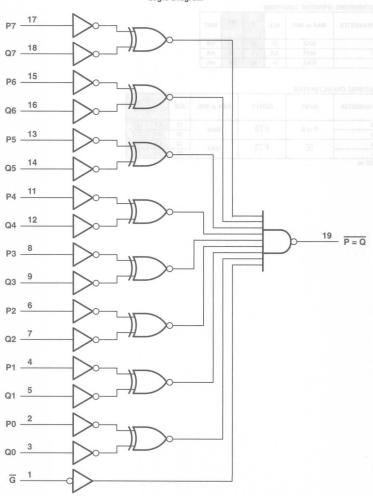
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	F	AC 11
tPLH	P or Q		MAY	12	8.7	12.6
tPHL .	Poru	P = 0.	MAX	20	10.3	11.3
tPLH .	ŌĒ	D 0	MAN	12	6.4	7.4
tPHL .	UE	P = Q	MAX	22	10.4	7.8



# **8-BIT IDENTITY COMPARATOR**

• 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

# Logic Diagram



#### FUNCTION TABLE

OUTPUT	UTS	INP
$\overline{P} = \overline{Q}$	ENABLE G	DATA P, Q
L	L	P = Q
Н	-Luca	P > Q
H	lan L	P < Q
H	K H	X

#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	rest <sub>F</sub> ort	AC 11	UNIT
Icc	MAX	19	32	0.08	mA
Іон	MAX	-2.6	-1	-24	mA
lou	MAX	24	20	24	mA

# CTAL D-TYPE TRANSPARENT

3-State Bus-Driving Inverting Outgets

Functionally Equivalent to '373, Except for Havin

Inverted Outputs

ARCT Door: Product Available in Reduced-Not

MACETTIXXX Product Available in Reduced-Nots

# 320K1 FK

SWITCHING CHAP	RACTERIST	ICS										
PARAMETER	INPUT	r	OUT	PUT	MAX	or MIN	ALS	F	AC 11			
tPLH .			_	_		441/	12	11	13			
tPHL .	PorC	1	P =	u	I.	ЛАХ	20	11	11.4			
tPLH	G		-	_		447	12	7.5	7.9			
tPHL .	G		P =	u	I N	ΛAX	22	10	8.1			
UNIT: ns	TIMU	ATM: TUA	WA			184	HITT TIM	1011	ACGS OH	The Self-		

- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

# Logic Diagram To Seven Other Channels

# **FUNCTION TABLE**

	INPUTS		OUTPUT
oc	ENABLE	D	Q
L	Н	Н	L
L	Н	L	Н
L	L	X	Q <sub>0</sub>
H	X	X	Z

# RECOMMENDED OPERATING CONDITIONS

RECOMMENDED	OPERATING CON	DITIONS				-	- 64	XA	M	. 0	+ 9		9
PARAMETER	MAX or MIN	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	AC 11	SN74 AC	ACT 11	SN74 ACT	UNIT
Icc	MAX	28	110	0.08	0.16	0.08	0.16	30	0.08	0.04	0.08	0.04	mA
Іон	MAX	-2.6	-15	-6	-6	-6	-6	-32	-24	-24	-24	-24	mA
lor	MAX	24	48	6	6	6	6	64	24	24	24	24	mA

# SWITCHING CHARACTERISTICS

SWITCHING CHA	NACTERIOTICS			T										
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	AC 11	SN74 AC	ACT 11	SN74 ACT
tw			MIN	15	2	20	24	25	24	3.3	4	5	5	6
tsu			MIN	15	2	13	15	13	15	2.1	3.5	4.5	3.5	4
th			MIN	7	3	5	-11	5	12	2.1	2	1	3.5	2.5
tPLH .	D	ā	MAX	19	7.5	38	50	44	51	6.4	9.8	11	11.3	11.5
tPHL .	D	u	IVIAA	13	7	38	50	44	51	6.6	8	10.5	9.5	11
tPLH	LE _	ā	MAX	23	9	44	53	44	57	7.3	11.3	11.5	13	11.5
tPHL .	(CD74: LE)	u	MAX	18	8	44	53	44	57	7.3	10.3	11	12.2	11.5
tPZH	0E	ā	MAX	17	6.5	38	45	44	53	5.7	10.8	10.5	12.5	11
tPZL	ÜE	u	MAX	18	9.5	38	45	44	53	6.7	9.7	10.5	12	11
tPHZ	ŌE	ā	MANY	10	6.5	38	45	44	45	6.9	11.4	11	12.8	11
tPLZ	UE	u	MAX	16	7	38	45	44	45	6.5	8.9	11	10.3	11

Functionally Equivalent to '374

- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



To Seven Other Channels

# **FUNCTION TABLE**

	INPUTS		OUTPUT
OC	CLK	D	Q
L	Ť	Н	L
L	1	L	Н
L	L	X	Qo
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

	24 28	Hō			1 3		0	0		1 48	1 85		XAM	
PARAMETER	MAX or MIN	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	UNIT
Icc	MAX	31	128	0.08	0.16	0.08	0.16	30	0.08	0.04	0.16	0.08	0.04	mA
Іон	MAX	-2.6	-15	-6	-6	-6	-6	-32	-24	-24	-24	-24	-24	mA
lor.	MAX	24	48	6	6	6	6	64	24	24	24	24	24	mA

SWITCHING CHARACTERISTICS

PAR	AMETER	IN	IPUT	0	UTPUT	MAX or MIN	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	AC 11	SN74 AC	CD74
fmax		SMAN	1000	RMS	4500	MIN	35	125	25	20	25	16	125	75	140	125
tw	CLK "H"					MIN	14	4	20	24	20	30	3.5	6.5	4	4
	CLK "L"					IVIIIN	14	3	20	24	20	30	3.5	6.5	4	4
tsu	9.7	6.9				2 3 9	10	2	25	18	25	30	1.6	3.5	4	2
h	6.0					MIN	0	2	5	5	5	5	2	4.5	1.5	2
PLH	1.014	(	CLK	0.	-	MAX	12	8	45	50	45	53	6.7	11.7	12	11.3
PHL	9.9	(CD)	4: CP)	E	ā	IVIAX	16	9	45	50	45	53	7.6	12.1	11	11.3
PZH	1.3	R.	0E	0%	=	MAX	17	6	38	45	37	53	5	10.4	11.5	14.5
PZL	[ 5.8 ]		UE 30	86	0	MAX	18	10	38	45	37	53	6.8	10.4	11.5	14.5
PHZ			0E		ā	MAX	10	6	38	45	37	45	7.3	11.6	12.5	14.5
PLZ			UE		u	WAX	. 14	6	38	45	37	45	6.5	9.2	11	14.5

PA	RAMETER	INPUT	OUTPUT	MAX or MIN	ACT 11	SN74 ACT
fmax		8.8	ls 10.5	MIN	55	120
tw	CLK "H"			MIN	9	3.5
	CLK "L"			IVIIIN	9	3.5
tsu				MIN	3	4
th				IVIIN	5.5	1.5
tPLH.		CLK	ā	MAX	14.5	12.5
<b>TPHL</b>		(CD74: CP)	u u	IVIAA	15	12
tPZH		ŌE	ā	MAX	13.3	12.5
tPZL		JE.	l u	WAX	13.5	11.5
tPHZ		ŌE	ā	MAN	13.5	13.5
tPLZ		UE	u	MAX	12	10.5

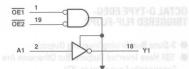
UNIT fmax: MHz, other: ns

# 540

# OCTAL BUFFERS AND LINE DRIVERS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Schmitt-Triggered Inputs (SN74LS540)

# **Logic Diagram**



To Seven Other Channels

# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	ALS A-1	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH 3V	CD74 AC	CD74 ACT	AHC	AHCT	UNIT
Icc	MAX	52	22	22	0.08	0.16	0.08	0.16	71	30	5	0.16	0.16	0.04	0.04	mA
Іон	MAX	-15	-15	-15	-6	-6	-6	-6	-15	-32	-32	-24	-24	-8	-8	mA
lor	MAX	24	24	48	6	6	6	6	64	64	64	24	24	8	8	mA

PARAMETER	MAX or MIN	LV 3V	LV 5V	LVC 3V	UNIT
Icc	MAX	1 - 10	0.02	0.01	mA
Іон	MAX	-8	-16	-24	mA
lou	MAX	8	16	24	mA

#### SWITCHING CHARACTERISTICS

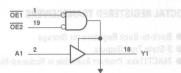
SWITCHING CHAR	ACTERISTICS												
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS A-1	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH 3V
tPLH .		Y	MAX	15	12	12	25	33	25	36	6.9	4.8	3.8
tPHL .	A	(CD74: Y)	IVIAX	15	9	9	25	33	25	36	4	4.8	3.8
tPZH	ŌE	Y	MAX	25	15	15	38	48	38	53	10.1	5.9	5.2
tPZL	UE	(CD74: Y)	IVIAX	38	20	20	38	48	38	53	11.3	6.4	5.3
tPHZ	ŌE	Y	MAN	25	10	10	38	48	38 .	53	9	7.3	5.6
tPLZ	UE	(CD74: Y)	MAX	18	12	12	38	48	38	53	8.5	6.2	5

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 AC	CD74 ACT	AHC	AHCT	3V	LV 5V	3V LVC
tplH		Y	MANY N	68	7.2	8	10	12	8	5.3
tPHL .	А	(CD74: Y)	MAX	68	7.2	8	10	12	8	5.3
tPZH	ŌĒ	Y	MAY	12	13.4	10.5	12	16	10.5	6.6
tPZL	UE	(CD74: Y)	MAX	12	13.4	10.5	12	16	10.5	6.6
tPHZ	<u> </u>	Y	MAN	12	13.4	10	12	17.5	10	7.4
tPLZ	0E	(CD74: Y)	MAX	12	13.4	10	12	17.5	10	7.4

# OCTAL BUFFERS AND LINE DRIVERS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Schmitt-Triggered Inputs (SN74LS541)

# Logic Diagram



To Seven Other Channels

#### ECOMMENDED OPERATING CONDITIONS

RECUMINENDED	UPERATING CON	DITIONS	)													
PARAMETER	MAX or MIN	LS	ALS	ALS A-1	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH 3V	CD74 AC	CD74 ACT	AHC	UNIT
Icc	MAX	55	25	25	75	0.08	0.16	0.08	0.16	72	30	5	0.16	0.16	0.04	mA
Іон	MAX	-15	-15	-15	-15	-6	-6	-6	-6	-15	-32	-32	-24	-24	-8	mA
lou	MAX	24	24	48	64	6	6	6	6	64	64	64	24	24	8	mA

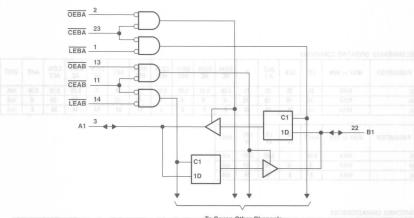
PARAMETER	MAX or MIN	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
Icc	MAX	0.04	-	0.02	0.01	mA
Іон	MAX	-8	-8	-16	-24	mA
lou	MAX	8	8	16	24	mA

# SWITCHING CHARACTERISTICS

OTTTOTHING OTTO			THE PROPERTY OF THE PARTY OF TH	FEED U			_	т —					
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS A-1	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT
tPLH .	Δ.	v	MAN	15	14	14	6	29	35	29	42	6	3.6
tPHL .	А	1	MAX	18	10	10	6	29	35	29	42	8.2	3.9
tPZH	ŌE	v	1447	32	15	15	9.5	38	48	38	53	10.7	4
tPZL	UE	T	MAX	38	20	20	9.5	38	48	38	53	11.5	5.9
tPHZ	ŌE	v	MAN	29	10	10	6.5	38	48	38	53	8.6	5.8
tPLZ	UE	Y	MAX	18	12	12	6	38	48	38	53	8.6	4.4

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	CD74 AC	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V
tPLH			1447	3.5	7.8	8.2	8	9.5	12	8	5.1
tphL .	A	Y	MAX	3.5	7.8	8.2	8	9.5	12	8	5.1
tpzH	ŌE		MANY	5.2	12	13.4	10.5	12	16	10.5	7
tPZL	UE	Υ.	MAX	5.3	12	13.4	10.5	12	16	10.5	7
tPHZ	ŌE	.,	MAN	5.6	12	13.4	10	12	17.5	10	7
tPLZ	UE	Y	MAX	5	12	13.4	10	12	17.5	10	7

# Logic Diagram



				To Sev	en Other Channe	els	

**FUNCTION TABLE†** 

	1 0110			
	INPL	JTS		OUTPUT
CEAB	LEAB	OEAB	Α	В
Н	X	X	X	Z
X	X	Н	X	Z
L	H	L	X	B <sub>0</sub> ‡
L	L	L	L	L
1.	L	L	Н	н

# RECOMMENDED OPERATING CONDITIONS

PARA	METER	MAX or MIN	F	SN74 BCT	ABT	LVTH 3V	ACT 11	SV TVC	UNIT
Іссн		MAX	100	8	0.25	0.19	0.08	0.01	mA
ICCL		MAX	125	71	30	5	0.08	0.01	mA
lccz		MAX	125	15	0.25	0.19	0.08	0.01	mA
Іон	A	MAX	-3	-15	-32	-32	-24	-24	mA
ЮН	В	MAX	-15	-15	-32	-32	-24	-24	mA
la:	A	MAX	24	64	64	64	24	24	mA
lor	В	MAX	64	64	64	64	24	24	mA

	PARAMETER		INPUT	OUTPUT	MAX or MIN	F	SN74 BCT	ABT	LVTH 3V	ACT 11	SV.
tw	4D 01	2	d ar-		MIN	5	7	3.5	3.3	4	3.3
tsu	LE ↑ before	"H"	-			3.5	4.5	3.5	0.4	2.5	1.6
	LE ↑ before	"L"	1		MIN	3.5	4.5	3	_1	2.5	1.6
	CE ↑ before	"H"		-	191114	-	-	3.5	0.2	3	1.6
	CE † before	"L"	1				-	3	0.7	3	1.6
th	LE ↑ after	"H"	]	100		3.5	1.5	0.5	1.5	2	2.1
	LE ↑ after	"Ľ.			MIN	3.5	1.5	0.5	1.3	2	2.1
	CE ↑ after	"H"	1		IVIIIV	0 -	-	0.5	1.6	1.5	2.1
	CE ↑ after	T	d of			-		0.5	1.4	1.5	2.1
tPLH	TILL		A or B	B or A	MAX	8.5	8.8	6.9	3.7	10.2	7
tPHL			AUID	DUIA	IVIAA	7.5	9.6	6.9	3.7	12.1	7
tPLH			LEBA	A	MAX	12.5	12.9	6.6	4.7	11.2	8.5
tPHL.			LEDA	A	IVIAA	12.5	12.7	7.1	4.7	13.2	8.5
tPLH			LEAB	В	MAX	12.5	12.9	6.6	4.7	11.2	8.5
tPHL			LEAD	D .	IVIAA	12.5	12.7	7.1	4.7	13.2	8.5
tPZH			OE	A or B	MAX	10	10.7	6.4	4.9	11.5	7.7
tPZL	ACT PT	27.	UE	A OF B	IVIAX	12	12.3	7.5	4.9	15.3	7.7
tPHZ			OE	A or B	MAX	9	8.1	8.4	5.3	10.4	7
tPLZ			UE	A OF B	IVIAX	8.5	7.2	8	5.3	10.5	7
tPZH			CE	A or B	MAX	10	12	6.4	5.3	12.2	8
tPZL			LE.	A OF B	IVIAA	12	13.5	7.5	5.3	16	8
tPHZ			CE	A or B	MAX	9	8.5	8.4	5.4	11	7
tPLZ			CE	M OF B	IVIAX	8.5	7.6	8	5.4	11.1	7

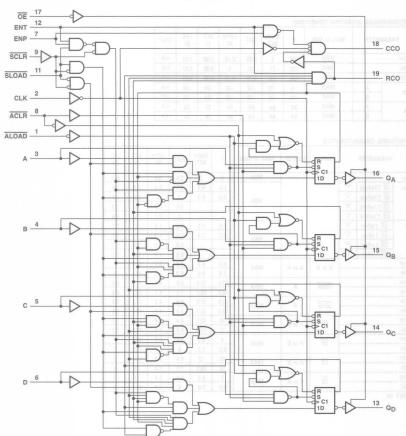
<sup>†</sup> A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA. ‡ Output level before the indicated steady-state input conditions were established

# 561

# **SYNCHRONOUS 4-BIT COUNTER**

- 3-State Outputs
- Choice of Asynchronous or Synchronous Clearing and Loading
- Internal Look-Ahead Circuitry for Fast Cascading

# Logic Diagram



# FUNCTION TABLE

			INP	UTS				OPERATION
OE	ACLR	ALOAD	SCLR	SLOAD	ENT	ENP	CLK	OPERATION
Н	X	X	X	X	X	X	X	Q outputs disabled
L	L	X	X	X	X	X	X	Asynchronous clear
L	H	L	X	X	X	X	X	Asynchronous load
L	Н	H	L	X	X	X	1	Synchronous clear
L	Н	H	H	L	X	X	1	Synchronous load
L	H	H	H	H	Н	H	1	Count
L	Н	Н	H	H	L	X	X	Inhibit counting
L	Н	H	H	H	X	L	X	Inhibit counting

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	MAX or MIN	ALS	UNIT
lcc		MAX	36	mA
	OUTPUT Q	MAX	-2.6	mA
Іон	CCO & RCO	MAX	-0.4	mA
lou	OUTPUT Q	MAX	24	mA
	CCO & RCO	MAX	8	mA

SWITC	HING CHAR	ACTERIS	STICS				
	PARAMETE	R	INPUT	Tipl	OUTPUT	MAX or MIN	ALS
fmax				1	100	MIN	30
tw	CLK	"H"	1			MIN	16.5
	CLK	.r.	1			MIN	16.5
tsu	ENP or	Н					20
	ENT L		1				20
	A, B,	C, D	1				20
	0010	L	1			MIN	15
	SCLR	H.	DUENO SUMBI			3904 400	30
		PL	DA DA			HC OH BAR	15
	SLOAD	Н	i 8			is in ar	30
th		711	7 33			MIN	0
tPLH		0	CIK		0	MAY	12
tPHL.		3.61	CLK	- 8	u	MAX	18
tPLH		100 01	CIV		RCO	MAX	29
tPHL.		arril	CLK		nco	MAX	24
<b>TPLH</b>		2.01	11000				35
tPHL .		101	ALOAD		Q	MAX	23
tPLH		20				MAY	55
tPHL.		an I	ALOAD		CCO	MAX	33
tPLH			FAIT	- '	DOO	MAY	16
tPHL.			ENT		RCO	MAX	14
tPHL.			ACLR		Q	MAX	22

UNIT fmax: MHz, other: ns

# OCTAL D-TYPE TRANSPARENT LATCHES WITH INVERTED OUTPUTS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout

# Logic Diagram DE 1 LE 11 D 2 1D 2

FUN			

	INPUTS	INPUTS			
ŌĒ	ENABLE LE	D	OUTPUT		
L	Н	Н	L		
L	Н	L	H		
L	L	X	Qo		
Н	X	X	Z		



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 AC	CD74 AC	SN74 ACT	UNIT
Icc	MAX	29	0.08	0.16	0.08	0.16	0.08	0.16	0.04	mA
Іон	MAX	-2.6	-6	-6	-6	-6	-24	-24	-24	mA
lou	MAX	24	6	6	6	6	24	24	24	mA

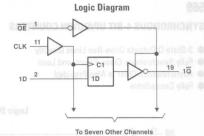
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 AC	CD74 AC	SN74 ACT
tw			UL	15	20	24	25	24	5	4	3
tsu			MIN	10	13	15	13	15	2.5	2	4.5
th			(2)	10	5	4	10	5	2	3	0
tPLH	D	ā	MAX	18	44	45	44	45	11.5	10.5	12.5
tphl .		ų IVIA.	MAX	14	44	45	44	45	11	10.5	11
tPLH	LE	ā	MAX	22	44	50	44	53	11	12	11.5
tphl.	(CD74: LE)	u	MAX	21	44	50	44	53	9.5	12	10.5
tPZH	ŌĒ	ā	MAX	18	38	45	44	53	10	10.5	10
tPZL	UE	u	MAX	18	38	45	44	53	9.5	10.5	9.5
tPHZ	05	OE Q MAX -	MAN	10	38	45	44	53	12	11.5	11.5
tPLZ	UE		15	38	45	44	53	9	11.5	8.5	

# 564

# OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

- 3-State Buffer-Type Inverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout



# **FUNCTION TABLE**

	INPUTS		OUTPUT
OE	CLK	D	Q
L	1	Н	L
L	1	a-L	Н
L	0.00	X	Q <sub>0</sub>
Н	X	X	Z

# RECOMMENDED OPERATING CONDITIONS

NECOMMENDED	UFENATING CON	DITION	2		_				
PARAMETER	MAX or MIN	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 AC	SN74 ACT	UNIT
Icc	MAX	30	0.08	0.16	0.08	0.16	0.04	0.04	mA
Гон	MAX	-2.6	-6	-6	-6	-6	-24	-24	mA
lor	MAX	24	6	6	6	6	24	24	mA

# SWITCHING CHARACTERISTICS

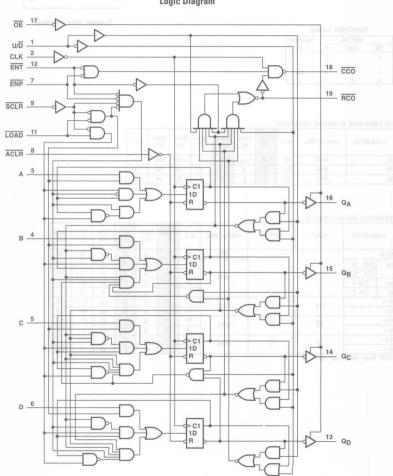
SAALI	CHING CHAN	ACTEMISTICS							_		_
PARAMETER		INPUT	OUTPUT	MAX or MIN	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 AC	SN74 ACT
fmax				MIN	30	25	20	25	16	85	75
tw	CLK "H"				14	20	24	20	30	5	3.5
	CLK "L"			MIN	14	20	24	20	30	5	3.5
tsu	CLK ↑				15	25	18	25	30	2.5	3
th	CLK ↑				0	5	5	5	3	2	1
tPLH		CLK	ā	MAX	14	45	50	45	53	11.5	11.5
tPHL.		ULK	u	WIAA	14	45	50	45	53	10.5	10.5
tPZH		ŌE	ā	MAX	18	38	45	38	53	9.5	9.5
tPZL	ZL		u	IVIAA	18	38	45	38	53	9.5	9.5
tPHZ tPLZ		ŌE	ā	MAX	10	38	41	38	45	11.5	11.5
		UE Q		WAX	15	38	41	38	45	9	8.5

UNIT fmax : MHz, other : ns

## SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

- 3-State Q Outputs Drive Bus Lines Directly
- Fully Synchronous Clear, Count, and Load
- Asynchronous Clear Is Also Provided
- Fully Cascadable

## Logic Diagram



#### FUNCTION TABLE

			INP	OPERATION				
ŌĒ	ACLR	SCLR	LOAD	ENT	ENP	U/D	CLK	OPERATION
Н	X	X	X	X	X	X	X	Q outputs disabled
L	L	X	X	×	X	X	X	Asynchronous clear
L	Н	L	X	×	X	X	1	Synchronous clear
L	Н	H	L	X	X	X	1	Load
L	H	Н	H	L	L	H	1	Count up
- L	Н	H	Н	L	L	L	1	Count down
L	Н	H	H	H	X	X	X	Inhibit count
L	Н	H	H	X	H	X	X	Inhibit count

# OCTAL O-TYPE TRANSPARENT

3-State Buffer-Type Outputs Drive Bus Lines
 The contract of the Contr

Bus-Structured Pinout

# RECOMMENDED OPERATING CONDITIONS

F	PARAMETER	MAX or MIN	ALS	UNIT
lcc		MAX	32	mA
Іон	OUTPUT Q	MAX	-2.6	mA
	CCO & RCO	IVIAX	-0.4	mA
lou	OUTPUT Q	MAX	24	mA
	CCO & RCO	IVIAX	8	mA

#### FUNCTION TABLE

#### SWITCHING CHARACTERISTICS

SVVII	CHING CHAP	ACTENIA	1163	5	100	9 9	1			
	PARAMETE	3 16	INPUT	OUTPUT	M	AX or MIN	ALS			
fmax						MIN	30			
tw	ACLR, L	OAD			11975	V6 V	15	TURA:		
	CLK '	H"				MIN	16.5			
	CLK	L*			AMI		16.5	90.0		
tsu	Data at A,	B, C, D			100	100	20	8		
	ENP, ENT	High			AUR		30	8		
	ENP, ENI	Low					20			
	0010	High					15			
	SCLR	Low				MIN	30	-		
	TOAD	High			2.0		15	560		
	LOAD	Low			1		30			
	UĒ	121			8.5		30			
	ACL	R			2		10			
th	61 13	77 24			3	MIN	0			
tPLH	22 18	168	CLK	ANY Q	8	MAX	13			
tPHL	Ea L 38	63	CLK	ANYU		WAX	16			
tPLH	8.8	1 88	CLK	RCO	tt	MAX	28			
tPHL.	3.5 3.5	53	ULK Ed	RLU	5.5	IVIAA	19			
tPLH	ta Live	2.3	ENT	RCO	100	MAX	15			
tPHL	14 1 10	1 68	EN I	HUU	0.5	IVIAA	13			
tPHL	Int I i	88	ACLR	ac 0 at	6.5	MAX	20			
tPZH	88 BB	63	ŌĒ	18 a 8	15	MAX	18			
tPZL			UE	u		IVIAX	24			
tPHZ			ŌĒ	0		MAX	10			
tPLZ	301 1	V.	TOHA OHA	Sign D Corn	egra	IVIAA	13	10.0		

UNIT fmax: MHz, other: ns

## **OCTAL D-TYPE TRANSPARENT** LATCHES

- 3-State Buffer-Type Outputs Drive Bus Lines
- Bus-Structured Pinout

# Logic Diagram OE 1 C1 1D To Seven Other Channels

#### **FUNCTION TABLE**

	INPUTS		
ŌĒ	ENABLE	D	OUTPUT
L	Н	Н	Н
L	Н	L	L
L	L	X	Qo
Н	X	X	Z

#### RECOMMENDED OPERATING CONDITIONS

RECOMMENDED O	PERATING CONDI	TIONS													
PARAMETER	MAX or MIN	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH 3V	SN74 AC	CD74 AC	SN74 ACT	UNIT
Icc	MAX	27	106	55	0.08	0.16	0.08	0.16	62	30	5	0.04	0.16	0.04	mA
Іон	MAX	-2.6	-15	-3	-6	-6	-6	-6	-15	-32	-32	-24	-24	-24	mA
lou	MAX	24	48	24	6	6	6	6	64	64	64	24	24	24	mA

PARAMETER	MAX or MIN	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	TAC 3A	UNIT
lcc	MAX	0.16	0.04	0.04		0.02	0.01	mA
Іон	MAX	-24	-8	-8	-8	-16	-24	mA
lou	MAX	24	8	8	8	16	24	mA

#### SWITCHING CHARACTERISTICS

PARA	AMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH 3V
tw	LE			06	10	4.5	6	20	24	25	24	4	3.3	3.3
tsu	LE ↓			MIN	10	2	2	13	15	13	20	1	1.9	0.7
th	LE ↓			5	7	3	3	5	12	5	15	4	1.8	1.5
tPLH		D	0	MAX	14	8	8	44	53	44	53	8.4	5.9	3.9
tPHL .		U	u	IVIAX	14	7	6	44	53	44	53	9.6	6.2	3.9
tPLH		LE	0	MAX	20	13	13	44	53	- 44	53	8.1	6.6	4.2
tPHL.		LE	0	IVIAA	19	7.5	8	44	53	44	53	7.8	7.2	4.2
tPZH		ŌĒ	0	MAN	18	6.5	12	38	45	44	53	10.4	5.2	5.1
tPZL		UE	۵	MAX	18	9.5	8.5	38	45	44	53	11	6.7	5.1
tPHZ		ŌĒ	0	MAN	10	6.5	7.5	38	45	44	53	6	7.1	4.9
tPLZ.		UE	Q	MAX	15	7	6	38	45	44	53	6	6.5	4.6

PARA	AMETER	INPUT	OUTPUT	MAX or MIN	SN74 AC	CD74 AC	SN74 ACT	CD74 ACT	AHC	AHCT	LV 5V	LV 3V	3V LVC
tw	LE				5	4	4	4	5	5	5	5	3.3
tsu	LE Ţ			MIN	3.5	2	3.5	2	3.5	3.5	3.5	3.5	2
th	LE ↓				2	3	0	3	1.5	1.5	1.5	1.5	1.5
tPLH		D	Q	MAX	11.5	8.5	12	10.4	10	7.5	10	16.5	6.9
tphL.			u	IVIAX	11	8.5	12	10.4	10	10	10	16.5	6.9
tPLH .		LE	Q	MAX	11	12	12	12.5	11	8.5	11	17.5	7.7
tphl.		(CD74AC/ACT: LE)	u	IVIAA	10	12	10.5	12.5	11	10	11	17.5	7.7
tPZH		- ŌE	Д	MAX	10	10.5	11	13.5	11	8	11	17	7.5
tPZL		UE I	и	WAX	9.5	10.5	10.5	13.5	11	11	11	17	7.5
tPHZ		ŌĒ	0	MAX	12	11.5	12.5	12.5	11	12	11	16.5	6.5
tPLZ		UE	u	WAX	9	11.5	9.5	12.5	11	10.5	11	16.5	6.5

## OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

- 3-State Buffer-Type Noninverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout

# OE 1 CLK 11 1D 2 To Seven Other Channels

Logic Diagram

#### **FUNCTION TABLE**

	INPUTS		OUTPUT
OE	CLK	D	Q
L	1	н	Hamil
L	1	L	L
L	L	×	Q <sub>0</sub>
Н	X	X	Z

#### ECOMMENDED OPERATING CONDITION:

PARAMETER	MAX or MIN	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH 3V	SN74 AC	CD74 AC	SN74 ACT	UNIT
lcc	MAX	28	134	86	0.08	0.16	0.08	0.16	62	30	5	0.04	0.16	0.04	mA
Іон	MAX	-2.6	-15	-3	-6	-6	-6	-6	-15	-32	-24	-24	-24	-24	mA
lor	MAX	24	48	24	6	6	6	6	64	64	24	24	24	24	mA

PARAMETER	MAX or MIN	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
Icc	MAX	0.16	0.04	0.04	-	0.02	0.01	mA
Іон	MAX	-24	-8	-8	-8	-16	-24	mA
lou	MAX	24	8	8	8	16	24	mA

#### SWITCHING CHARACTERISTICS

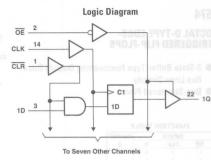
SWITCHING CHARA	CTERISTICS								231	SHEE	ARAM?	SWIND	SVE
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	jų F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH 3V
fmax			MIN	35	125	100	24	20	24	20	77	150	150
tw			MIN	14	5.5	7	20	24	20	24	6.5	3.3	3.3
tsu			MIN	15	5.5	2	25	18	25	18	6	1.5	2
th			MIN	0	0	2	5	5	5	5	0	1.8	0.3
tPLH	CLK	0	MAY	14	8	10	45	50	45	50	10	6.8	4.5
tPHL .	ULN	۵	MAX	14	9	10	45	50	45	50	8.9	7.1	4.5
tPZH	ŌE	Q	MAX	18	6	12.5	38	45	38	45	10.4	5.1	4.8
tPZL.	UE	OE U		18	10	8.5	38	45	38	45	10.9	6.7	4.8
tPHZ	ŌE	<u></u>		10	6	8	38	41	38	42	7.5	7	4.8
tPLZ	UE	Q	MAX	12	6	6.5	38	41	38	42	6.4	6.5	4.4

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 AC	CD74 AC	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	3V LVC
fmax			MIN	85	125	85	110	75	75	45	75	100
tw			MIN	5	4	4	4.5	5	5.5	5	5	3.3
tsu			MIN	2	2	2.5	2	3	3.5	3.5	3.5	2
th			MIN	1.5	2	0	3	1.5	1.5	1.5	1.5	1.5
tplH	CLK	014	MANY	11	10.8	12	11.2	12	12	19	12	7
tрнL	CLK	ū	MAX	9.5	10.8	11	11.2	12	12	19	12	7
tpzH	ŌE	Q	MANY	9	14.5	10	14.5	12.5	12.5	18.5	12.5	7.5
tPZL	OE U		MAX	9	14.5	10	14.5	12.5	12.5	18.5	12.5	7.5
tPHZ	ŌE	0	MAN	10.5	14.5	11.5	14.5	11.5	11.5	17	11.5	6.4
tPLZ	UE	OE Q MAX	MAX	8.5	14.5	9	14.5	11.5	11.5	17	11.5	6.4

UNIT fmax : MHz, other : ns

## OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

- 3-State Buffer-Type Noninverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Synchronous Clear



#### **FUNCTION TABLE**

	INP	OUTPUT		
ŌĒ	CLR	CLK	D	Q
L	L	1	X	L
L	Н	1	Н	H
L	H	1	L	L
L	H	L	X	Qo
H	X	X	X	Z

RECOMMENDED OPERATING CONDITIONS

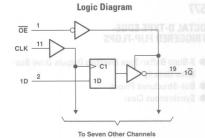
PARAMETER	MAX or MIN	ALS	AS	UNIT
lcc	MAX	30	142	mA
Іон	MAX	-2.6	-15	mA
lou	MAX	24	48	mA

SWITCHING CHARACTERISTICS

PA	RAMET	ER	IN	PUT	0	UTPUT	MAX or MIN	ALS	AS
fmax		17	100 145		00 10		MIN	30	90
tw	CLK	Н	95	THE.	18	Title	5.8		
		L					5 35 2	16.5	5.5
tsu	DA	TA	1.6	15:	5	E	S MINI	15	5.5
CLR	CLR	L					MIN	15	6.5
th DATA		TA	68	15	08	19	M H P		3
	CI	CLR					21 6 0	0	0
tPLH	TEL	P04	0	w III	80		MAN	14	8
tPHL .		C	LK	19	Q	MAX	14	9	
tРZH		-	C	16	0	MAX	18	6	
tPZL			16	0		WAX	18	10	
tPHZ			C	0 MHC		MAX	10	6	
tpi 7			16			MAX	13	6	

## OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

- 3-State Buffer-Type Inverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Functionally Equivalent to '576, Except for Having Inverted Outputs



#### **FUNCTION TABLE**

Γ		INPUTS		OUTPUT
	ŌE	CLK	D	Q
Г	L	1	Н	L
П	L	1	L	H
ı	L	L	X	$\bar{Q}_0$
ı	Н	X	X	Z



#### RECOMMENDED OPERATING CONDITIONS

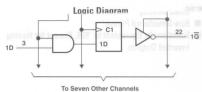
PARAMETER	MAX or MIN	ALS	AS	UNIT
Icc	MAX	30	135	mA
Іон	MAX	-2.6	-15	mA
lor.	MAX	24	48	mA

#### SWITCHING CHARACTERISTICS

SAALL	JIIING CHANA	CIENISTICS			_	_	
PA	RAMETER	INPUT	ОИТРИТ	MAX or MIN	ALS	AS	
fmax				MIN	30	125	
tw	Н				16.5	4	
	L			MIN	16.5	2	
tsu	su DATA			IVIIIN	15	2	
th	DATA				0	2	
tPLH		CLK	ā	MAX	14	8	
tPHL.		ULK	u	MAX	14	9	
tPZH		ŌE	ā	MAX	18	6	
tPZL		UE	u	IVIAX	18	10	
tPHZ tPLZ		ŌĒ	ō	MAX	10	6	
		UE	u	WAX	15	6	

UNIT fmax : MHz, other : ns

- Bus-Structured Pinout
- Synchronous Clear



#### FUNCTION TABLE

	INP		OUTPUT	
OE	CLR	CLK	D	Q
L	L	1	X	Н
L	H	1	Н	L
L	H	1	L	H
L	H	L	X	Q <sub>0</sub>
H	X	×	X	Z



RECOMMENDED OPERATING CONDITIONS

				_
PARAMETER	MAX or MIN	ALS	AS	UNIT
Icc	MAX	30	142	mA
Іон	MAX	-2.6	-15	mA
lou	MAX	24	48	mA

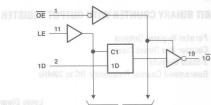
SWITC	HING CHARA	ACTERISTICS							
PAR	AMETER	INPUT	ОИТРИТ	MAX or MIN	ALS	AS	o XANI		
fmax				MIN	30	125	10		
tw				1	16.5	4			
tsu	DATA			MIN	15	2	los		
th	CLR			2	0	2			
tPLH		OLK	ā	144V S	14	8			
tPHL.		CLK	u	MAX	14	9	100		
tPZH		ŌE	ā	MAX	18	6	1000		
tPZL		UE	u	IVIAX	18	10	10.0		
tPHZ		ŌE	ā	MAX	10	6			
tPLZ		UE	u	IVIAX	15	6	OM		
UNIT 1	fmax : MHz, o	ther: ns		8	15		100		

## 580

## **OCTAL D-TYPE TRANSPARENT** LATCHES WITH INVERTED **OUTPUTS**

- 3-State Buffer-Type Outputs Drive Bus Lines
- Inverting-Logic Outputs
- Bus-Structured Pinout





To Seven Other Channels

**FUNCTION TABLE** 

	INPUTS		OUTDUT
OE	ENABLE	D	OUTPUT
L	Н	Н	L
L	Н	L	H
L	L	X	Q <sub>0</sub>
Н	X	X	Z

RECOMMENDED OPERATING CONDITIONS

	100			
PARAMETER	MAX or MIN	ALS	AS	UNIT
lcc	MAX	29	115	mA
Іон	MAX	-2.6	-15	mA
loc	MAX	24	48	mA

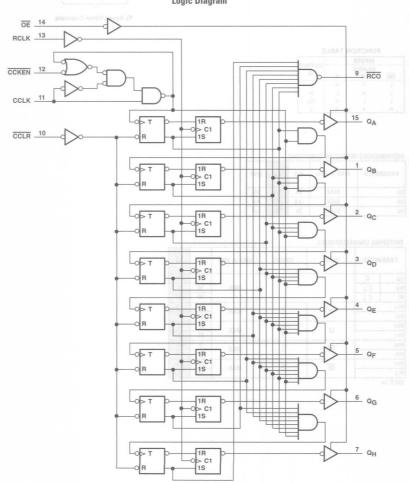
SWITCHING CHARACTERISTICS

PARA	AMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
tw	C		100		15	2
tsu	C 1			MIN	10	2
th	C \				10	3
tPLH .	100 E	100	ā	MAX	18	7.5
tPHL .		D	- u	IVIAA	14	7
tPLH		LE	ā	MAX	22	9
tPHL .		LE	u u	IVIAA	21	8
tPZH		ŌĒ	ā	MAX	18	6.5
tPZL	30 -9	OE .	u	MAX	18	9.5
tPHZ		ŌĒ	ā	MAX	10	6.5
tPLZ		UE	u	WAX	15	7

## 8-BIT BINARY COUNTER WITH OUTPUT REGISTER

- Parallel Register Outputs
- Counter Has Direct Clear
- 3-State Outputs
- Guaranteed Counter Frequency: DC to 20MHz

## Logic Diagram



RECOMMENDED	ODEDATING	COMPLITIONS

HEGGIANALEIAN	DED OF ENATING OC	TENTIONE		_	_
PA	ARAMETER	MAX or MIN	LS	SN74 HC	UNIT
Icc		MAX	65	0.08	mA
	RCO	MAX	-1	-4	mA
Іон	Q	MAX	-2.6	-6	mA
	RCO	MAX	16	4	mA
lor	0	MAX	24	6	mA

#### Logic Diagram

		TERIS	

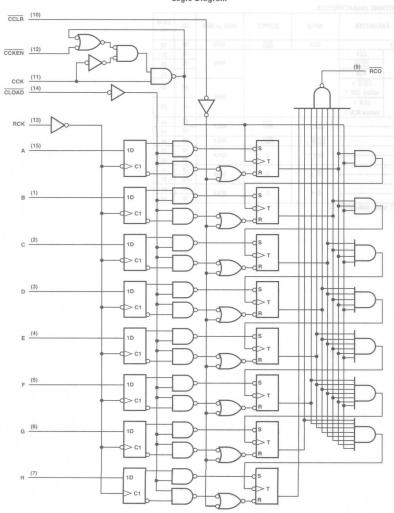
F	PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	SN74 HC
fmax		CCK	RCO	MIN	20	13
tw	CCK				25	31
	CCLR			MIN	20	25
	RCK				20	31
tsu	CCLR ↑ bofore CCK ↑			MIN	20	25
	CCK ↑ bofore RCK ↑			Milly	40	25
tPLH		CCK †	RCO	MAX	22	45
tPHL		CCK	nco	IVIAA	30	45
tPLH		CCLR ↓	RCO	MAX	45	39
tPLH		DCV A	Q	MAX	18	42
tPHL.		RCK ↑	1 7-00-	IVIAA	33	42
tPZH		Ğψ	0.115-	MAX	38	37
tPZL		g ţ	u	IVIAA	45	37
tPHZ		G ↑	0	MAX	30	37
tPLZ		U T	0 80-	IVIAA	38	37

#### UNIT fmax : MHz, other : ns

## 8-BIT BINARY COUNTER WITH INPUT REGISTER

- Parallel Register Inputs
- Counter Has Directly Overriding Load and Clear
- Accurate Counter Frequency: DC to 20MHz

## Logic Diagram



PARAMETER	MAX or MIN	LS	UNIT
Icc	MAX	60	mA
Іон	MAX	-1	mA
lou	MAX	16	mA

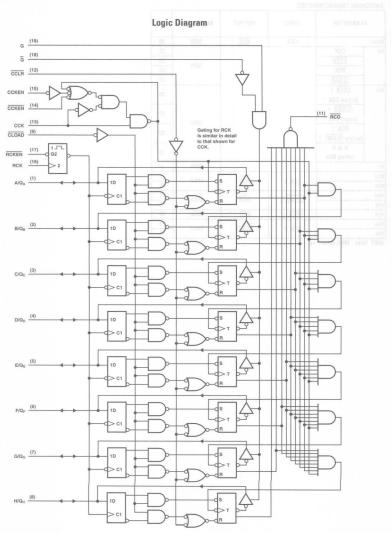
#### HEIT BINARY COUNTER WITH IMPUT REGISTE

- Parallel 3-State I/O: Register Inguts/Counter Outputs
  - Tounter Has Directly Overriding Load and Clear

#### SWITCHING CHARACTERISTICS

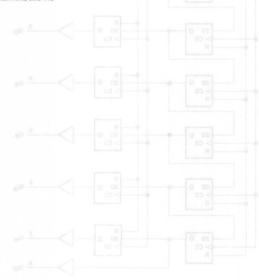
	PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
fmax		CCK	RCO	MIN	20
tw	CCK				25
	CCLR			MIN	20
	RCK			WIIIV	20
	CLOAD				40
tsu	CCLR ↑ bofore CCK ↑				20
	CLOAD ↑ bofore CCK ↑			MIN	20
	RCK ↑ bofore CLOAD ↑			Fine pares	30
	A to H bofore RCK			200	20
th				MIN	0
tPLH		CCK ↑	RCO	MAX	23
tPHL	-	CON	1100	WIAA	30
tPLH .	-	CLOAD 1	RCO	MAX	47
tPHL		CEOMD 1	1100	WIAA	17
tPLH		CCLR ↓	RCO	MAX	45
tPLH		RCK ↑	RCO Q	MAX	53
tPHL.		HON	1100 0	WINA	45

UNIT fmax : MHz, other : ns



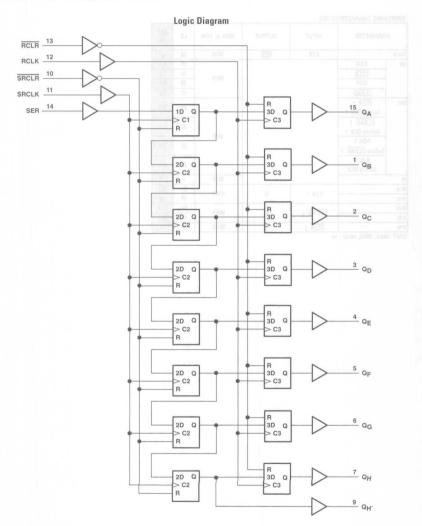
	PARAMETER	MAX or MIN	LS	ACT 11	UNIT
Icc		MAX	85	0.08	mA
Іон	RCO	MAX	-1	-24	mA
IUH	Q	MAX	-2.6	-24	mA
los	RCO	MAX	16	24	mA
lor	0	MAX	24	24	mA

	PARAMETER	INPUT	OUTPUT	MAX or MIN	11	
fmax		CCK	RCO	MIN		
tw	CCK		'		25	9.6
	CCLR			AAINI	20	7.6
	RCK			MIN	20	5.8
	CLOAD				40	6.2
tsu	CCLR ↑ bofore CCK ↑				20	1.2
	CLOAD ↑ bofore CCK ↑			To Man	20	5.1
	RCK ↑ bofore CLOAD ↑			MIN	30	7.4
	A to H bofore RCK				20	2.4
th				MIN	0	0.8
tPLH		001/4	a	MAX	21	15.1
tPHL		CCK ↑	u	IVIAX	39	15
tPLH	- 12	CLOAD 1	Q	MAX	51	19.1
tPHL	30	CLUAD 1	D 68	IVIAX	42	21.7
tPHL		CCLR 1	0	MAX	38	16



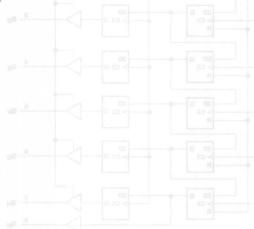
## 8-BIT SHIFT REGISTER WITH OUTPUT LATCHE

- 8-Bit Serial-In, Parallel-Out Shift Registers with Storage
- Independent Direct Overriding Clears on Shift and Storage Registers
- Independent Clocks for Shift and Storage Registers
- Guaranteed Shift Frequency: DC to 20MHz



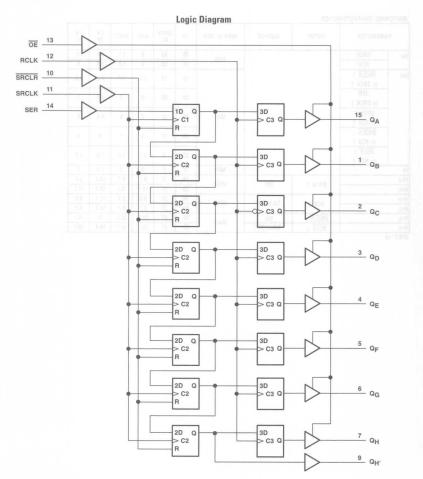
SWITCHING CHARACTERISTICS						
	CHAUTCE	HNIC	CUA	DAG	TEDI	CTICC

F	PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	SN74 HC	AHC	AHCT	LV 3V	LV 5V
tw	SRCK		1	MIN	25	20	5	5.5	5.5	5
	RCK			IVIIN	20	20	5	5.5	5.5	5
tsu	SRCLR ↑ to SRCK ↑				20	10	3.3	3.3	4.8	3.3
	SER to SRCK ↑				20	22	3	3	3.5	3
	SRCK ↑ to RCK ↑	44		MIN	40	22	5	5	8.5	5
	SRCLR ↓ to RCK ↑				40	13	5	5	9	5
	RCLR ↑ to RCK ↑				20	5	3.7	3.8	5.3	3.7
th	97			MIN	0	5	2	2	1.5	2
TPLH		0004 +	OH,	MAN	18	37	9.1	9.1	12.4	9.1
tPHL		SRCK ↑	un	MAX	23	37	10.1	10.1	13.9	10.1
tPLH		201.4	QA to QH	MAX	18	37	8.3	8.3	11.1	8.3
TPHL	-0 -E	RCK ↑	UA to UH		30	37	9.7	9.7	13.1	9.7
<b>TPHL</b>		SRCLR ↓	OH.	MAX	33	37	10.7	10.1	14	10.1
tPHL		RCLR 1	QA to QH	IVIAX	57	31	10.1	10.7	14.4	10.7



## 8-BIT SHIFT REGISTER WITH OUTPUT LATCHE

- 8-Bit Serial-In, Parallel-Out Shift Registers with Storage
- 3-State Outputs
- Shift Register Has Direct Clear
- Accurate Shift Frequency: DC to 20MHz



#### RECOMMENDED OPERATING CONDITIONS

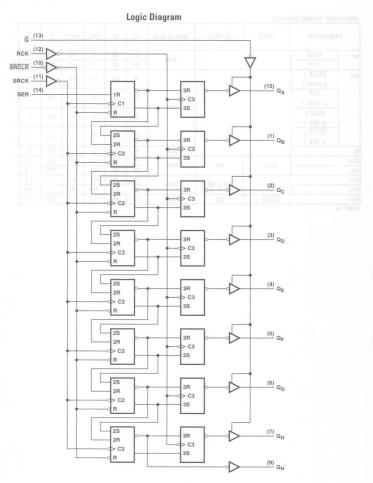
PAR	AMETER	MAX or MIN	LS	SN74 HC	AHC	AHCT	LV 3V	LV 5V	UNIT	SIT SHIFT REGISTER WIT
С		MAX	65	0.08	0.04	0.04	-	0.02	mA	
	ΩH.	MAX	-1	-4	-8	-8	-8	-16	mA	8-Bit Serial-In, Parallel-Out
Н	QA to QH	MAX	-26	-6	-8	-8	-8	-16	mA	Councillector Parallel Outs
	σH.	MAX	16	4	8	8	8	16	mA	
L	QA to QH	MAX	24	6	8	8	8	16	mA	Shift Register Has Direct Cla

#### SWITCHING CHARACTERISTICS

SVVIIGI	HING CHARACTER	1131163		1000 1200 000							
Р	ARAMETER	INPUT	OUTPUT	MAX or MIN	LS	нс	AHC	AHCT	LV 3V	LV 5V	
tw SRCK					25	20	5	5.5	5.5	5	
	RCK			MIN	20	20	5	5.5	5.5	5	
tsu	SRCLR ↑ to SRCK ↑	- 1110	3 -		20	12	2.5	3.8	3	2.5	
	SER to SRCK ↑	No (III)		SE MIN	20	25	3	3	3.5	3	
	SRCK ↑ to RCK ↑				40	19	5	5	8.5	5	
	SRCLR ↓ to RCK ↑	80 (I)		ne	40	13	5	5	9	5	
th		1		MIN	0	0	2	2	1.5	2	
PLH		CDCV A	OH.	MAY	18	40	11.4	11.4	18.5	11.4	
PHL		SRCK ↑	UH L	MAX	25	40	11.4	11.4	18.5	11.4	
PLH		DOV A	QA to QH	MAX	18	37	10.5	10.5	17	10.5	
PHL		RCK ↑	UA TO UH		35	37	10.5	10.5	17	10.5	
tPHL		SRCLR ↓	OH.	MAX	35	44	11.1	11.1	17.2	11.1	

## 8-BIT SHIFT REGISTER WITH OUTPUT LATCHE

- 8-Bit Serial-In, Parallel-Out Shift Registers with Storage
- Open-Collector Parallel Outputs
- Shift Register Has Direct Clear
- Accurate Shift Frequency: DC to 20MHz



#### RECOMMENDED OPERATING CONDITIONS

TILOUTHITILITY	DED OF ENVITORED	T		T
P)	ARAMETER	MAX or MIN	LS	UNIT
Icc		MAX 55		mA
	σH.	MAX	16	mA
Іон	Q	MAX	24	mA
lor	OH.	MAX	-1	mA
Vон	QA to QH	MAX	5.5	V

## IFT RESISTER WITH INPUT LATERS

48 8-Bit Parallel Storage Registers Inputs

Senitringpater has onest coefficiently coast and product

#### SWITCHING CHARACTERISTICS

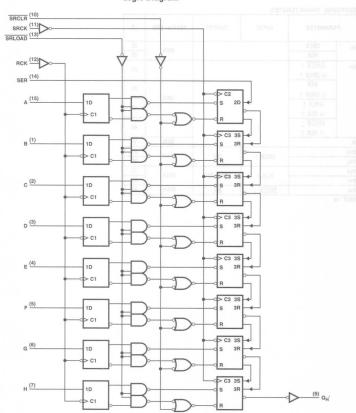
F	ARAMETER	INPUT	OUTPUT	MAX or MIN	LS
tw	SRCK			MIN	25
	RCK			IVIIIV	20
tsu	SRCLR ↑ to SRCK ↑			Y	20
	SER to SRCK ↑			MIN 2	
	SRCK ↑ to RCK ↑			MIN	40
	SRCLR ↓ to RCK ↑				40
th				MIN	0
PLH		CDCV A	OH.	MAX	21
tPHL		SRCK ↑	un	IVIAA	30
tPLH .		RCK ↑	QA to QH	MAX	42
tPHL.		nuk T	un to un	IVIAA	35
tPHL		SRCLR 1	OH.	MAX	35

## 597

## 8-BIT SHIFT REGISTER WITH INPUT LATCHE

- 8-Bit Parallel Storage Registers Inputs
- Shift Register Has Direct Overriding Load and Clear
- Accurate Shift Frequency: DC to 20MHz

## Logic Diagram



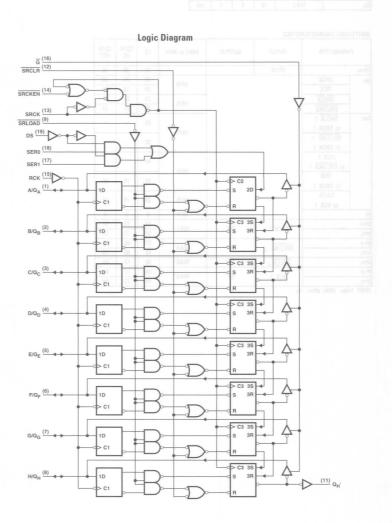
#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	CD74 HC	CD74 HCT	UNIT
Icc	MAX	53	0.16	0.16	mA
Іон	MAX	-1	-4	-4	mA
lou	MAX	16	4	4	mA

#### SWITCHING CHARACTERISTICS

	PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	CD74 HC	CD74 HCT
fmax		SRCK		-	20	20	16
tw	SRCK			MIN	35	24	30
	RCK			IVIIIV	20	18	20
	SRCLR			MIN	20	24	27
	SRLOAD			IVIIIV	40	21	24
tsu	SRCLR ↑ to SRCK ↑			MIN	25	į.	-11-X
	SRLOAD ↑ to SRCK ↑			WIIN	30	1.	-
	RCK ↑ to SRLOAD ↑				40	(	
	SER to SRCK ↑			MIN	20	15	15
	DATA to RCK ↑			MIN	20	15	15
th				MIN	0	3	3
tPLH		Annu .	000	1111	23	53	57
tPHL		SRCK ↑	σH.	MAX	30	53	57
tPLH		001040	OH,	MAN	57	60	72
tPHL		SRLOAD ↓	ин	MAX	44	60	72
<b>TPHL</b>		SRCLR ↓	σH,	MAX	36	53	66
tPLH		DOV A	OH.	MAX	60	72	84
tPHL.		RCK ↑	ин	IVIAX	48	72	84

UNIT fmax : MHz, other : ns



SWITCHING CHARACTERISTICS

PARAMETER	INPUT	ОИТРИТ	MAX or MIN	LS
fmax	SRCK	AL 1100 May 51	MIN	20
tPLH		ΩH.	14437	17
tPHL .	SRCK ↑	ин	MAX	23
tPLH	001010	ΩH.	5.5.A.V	42
tPHL .	SRLOAD ↓	ин	MAX	30
tPHL .	SRCLR ↓	OH.	MAX	27
tplH	DCV A	OH.	MAX	48
tphl .	RCK ↑	ин	IVIAX	36
tPLH	ODOK A	0	MAX	18
tPHL .	SRCK ↑	u	IVIAA	28
tPLH	SRLOAD J	0	MAX	48
tphl.	SHLUAD \$	u	IVIAA	40
tphl.	SRCLR ↓	Q	MAX	38
tPZH	Ğψ	0	MAX	31
tPZL	p †	u	IVIAA	43
tрнz	G↑	0	MAX	38
tPLZ	6.7	0	IVIAX	30

waxamced United Chiefe Senes; MACT) Ixxx: Product Available in Reduced-N

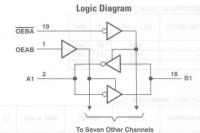
SHOWS MAKENDERS

UNIT fmax : MHz, other : ns

## 620

## **OCTAL BUS TRANSCEIVERS**

- Local Bus-Latch Capability
- 3-State Inverting Outputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



#### **FUNCTION TABLE**

ENABLE	INPUTS	OPERATION
ŌEBA	OEAB	OPERATION
L	L	B data to Abus
Н	Н	Ā data to B bus
Н	L	Isoration
L	Н	B data to Abus A data to B bus

#### RECOMMENDED OPERATING CONDITIONS

NECOMMENDED	OFENATING CON	DITION	)		-					_
PARAMETER	MAX or MIN	LS	ALS	AS	SN74 HC	SN74 BCT	ABT	AC 11	ACT 11	UNIT
lccz	MAX	95	47	77	0.08	10	0.25	0.08	0.008	mA
ICCL	MAX	90	44	122	0.08	84	30	0.08	0.008	mA
Iон (A port)	MAX	-15	-15	-15	-6	-3	-32	-24	-24	mA
loн (B port)	MAX	-15	-15	-15	-6	-15	-32	-24	-24	mA
lot (A port)	MAX	24	24	64	6	24	64	24	24	mA
lot (B port)	MAX	24	24	64	6	64	64	24	24	mA
lor.	MAX		48						-	mA

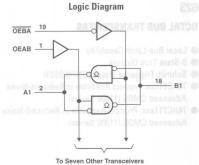
\*620-1

#### SWITCHING CHARACTERISTICS

SWITCHING CHA	AHACTERISTICS		_				1				
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	SN74 HC	SN74 BCT	ABT	AC 11	ACT 11
<b>TPLH</b>	A	В	MAX	10	10	7	26	5.8	4.8	7.4	9.4
tPHL .	A	В	MAX	15	10	6	26	3.6	4.8	7.1	8.6
tPLH	В	A	MAX	10	10	7	26	6.9	4.8	7.4	9.4
tPHL .	В	A	IVIAX	15	10	6	26	3.9	4.8	7.1	8.6
tPZH	OEBA	A	MAX	40	17	8	53	10.6	5.5	8.9	10.3
tPZL	UEBA	A	IVIAA	40	25	9	53	11.1	7.1	8.5	10.1
tPHZ	OEBA		MAX	25	12	6	38	10	7	8.1	10.4
tPLZ	UEBA	A	IVIAX	25	18	12	38	7.8	5.8	8.7	10.9
tPZH	OEAB	В	MAX	40	18	8	53	7.4	6.8	8.8	11.3
tPZL	UEAB	В	IVIAX	40	25	9	53	9	6.4	8.8	11
tPHZ	OEAB	В	MAX	25	12	6	38	8.1	6.5	8.2	9.4
tPLZ	UEAD	D	IVIAA	25	18	13	38	5.9	5.6	8.6	9.6

## **OCTAL BUS TRANSCEIVERS**

- Local Bus-Latch Capability
- Open-Collector True Outputs
- Schmitt-Triggered Inputs (SN74LS621)



#### **FUNCTION TABLE**

ENABLE INPUTS		ODEDATION	
OEBA	OEAB	OPERATION	
L	L	B data to Abus	
Н	Н	A data to B bus	
Н	L	Isoration	
L	Н	B data to Abus	

	CONDITIONS

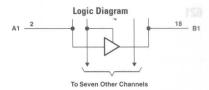
PARAMETER	MAX or MIN	LS	ALS	ALS A-1	AS	UNIT
Icc	MAX	90	48	48	189	mA
Vон	MAX	5.5	5.5	5.5	5.5	V
lou	MAX	24	24	48	64	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS A-1	AS
tPLH			1444	25	33	33	24
tPHL .	A	В	MAX	25	20	20	21
tPLH .	В		144V	25	33	33	7.5
tPHL	В	A A	MAX	25	20	20	7.5
tPLH	0EBA		144V	40	39	39	21
tPHL .	UEBA	A	MAX	50	35	35	9
tPLH	OEAB	В	MAX	40	39	39	22
tPHL 1	UEAB	B	MAX	50	35	35	10
UNIT: ns	3.4	8 85 8	5 1 30 1 7 UP	[ []	(1)		

## 623

- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



#### **FUNCTION TABLE**

ENABLE	INPUTS	OPERATION	
OEBA	OEAB	OPERATION	
L	L	B data to Abus	
Н	Н	A data to B bus	
Н	L	Isoration	
L	Н	B data to Abus A data to B bus	

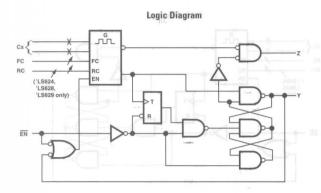
RECOMMENDED	OPERATING CON	DITIONS	5					Am II			83			AIA
PARAMETER	MAX or MIN	LS	ALS	AS	F	SN74 HC	SN74 HCT	SN74 BCT	ABT	AC 11	ACT 11	CD74 AC	CD74 ACT	UNIT
Iccz	MAX	95	55	116	130	0.08	0.08	11	0.25	0.08	0.04	0.16	0.16	mA
ICCL	MAX	90	50	189	140	0.08	0.08	92	30	0.08	0.04	0.16	0.16	mA
Iон (A port)	MAX	-15	-15	-15	-3	-6	-6	-3	-32	-24	-24	-24	-24	mA
loн (B port)	MAX	-15	-15	-15	-15	-6	-6	-15	-32	-24	-24	-24	-24	mA
lot (A port)	MAX	24	24	64	24	6	6	24	64	24	24	24	24	mA
lot (B port)	MAX	24	24	64	64	6	6	64	64	24	24	24	24	mA

#### CWITCHING CHARACTERISTICS

SWITCHING CHAP	ACTENISTICS		100	05	_		1							_	1
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	F	SN74 HC	SN74 HCT	SN74 BCT	ABT	AC 11	ACT 11	CD74 AC	CD74 ACT
tPLH			1449	15	13	9	6.5	26	28	5.2	4.6	7.8	8.5	9.6	10.6
tPHL .	A	В	MAX	15	11	8	7.5	26	28	7.4	4.6	7.1	7.9	9.6	10.6
tPLH			4444	15	13	9	6.5	26	28	6.7	4.6	7.8	8.5	9.6	10.6
tphl .	В	A	MAX	15	11	8.5	7.5	26	28	8	4.6	7.1	7.9	9.6	10.6
tPZH	OEBA		MAX	40	22	11	12	53	53	10.6	7.5	9	9.7	13.4	14.4
tPZL.	UEBA	A	MAX	40	22	10	10	53	53	10.7	7.5	9.1	10	13.4	14.4
tPHZ	OEBA		MAN	25	16	7.5	7.5	38	38	9.8	7.5	8.3	10.9	13.4	14.4
tPLZ	UEBA	A	MAX	25	19	11.5	7	38	38	7.8	7.5	8.8	11.5	13.4	14.4
tPZH	OCAR	В	MAN	40	22	11.5	11.5	53	53	7.6	7.5	9.2	10.7	13.4	14.4
tPZL	0EAB	В	MAX	40	22	11	9.5	53	53	8.9	7.5	9.4	10.9	13.4	14.4
tPHZ	OFAR	D	MAN	25	16	7	10	38	38	7.7	7.5	8.3	9.5	13.4	14.4
tPLZ	OEAB	В	MAX	25	19	9	10	38	38	7.1	7.5	8.8	10	13.4	14.4

## **VOLTAGE-CONTROLLED OSCILLATOR**

- This Voltage Oscillators (VCOs) is Improved Versions of The Original VCO Family: Intelliged against air SN74124, 324, 325, 326, 327
- Separate Supply Voltage Pins for Isolation of Frequency Control Inputs and Oscillators from Outputs
   Circuitry
- Highly Stable Operation over Specified Temperature and / or Supply Voltage Ranges and added vidials and added vidials.



#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
lcc	MAX	35	mA
lou	MAX	24	mA
Іон	MAX	-1.2	mA

#### SWITCHING CHARACTERISTICS

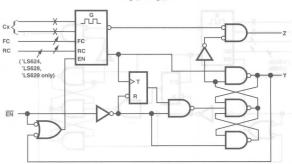
PARAMETER	MAX or MIN	LS
fo	MAX	25

UNIT: MHz

#### **VOLTAGE-CONTROLLED OSCILLATOR**

- This Voltage Oscillators (VCOs) is Improved Versions of The Original VCO Family: conflicted against and SN74124, 324, 325, 326, 327
- Separate Supply Voltage Pins for Isolation of Frequency Control Inputs and Oscillators from Outputs
   Circuitry
- Highly Stable Operation over Specified Temperature and / or Supply Voltage Ranges and Addit Addit Addition
- Two Rexternal Pins Can Offer More Precise Temprature Compensation

## Logic Diagram



#### RECOMMENDED OPERATING CONDITIONS

TIEGOTITITE TO ED	OI EIIIIIII OOII	1	_
PARAMETER	MAX or MIN	LS	UNIT
Icc	MAX	35	mA
Іон	MAX	-1.2	mA
lou	MAX	24	mA

#### SWITCHING CHARACTERISTICS

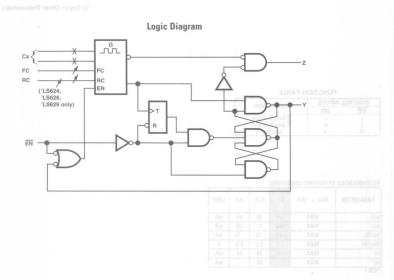
PARAMETER	MAX or MIN	LS
fo	MAX	25

UNIT: MHz



## **VOLTAGE-CONTROLLED OSCILLATOR**

- This Voltage Oscillators (VCOs) is Improved Versions of The Original VCO Family: next and lengths sibility. SN74124, 324, 325, 326, 327
- Separate Supply Voltage Pins for Isolation of Frequency Control Inputs and Oscillators from Outputs
- Highly Stable Operation over Specified Temperature and / or Supply Voltage Ranges



#### RECOMMENDED OPERATING CONDITIONS

THE OUTTO A DECEMBER OF THE OUTE OUT OF THE OUTE OF THE OUTE OF THE OUTE OF THE OUTE OUT OF THE OUTE OUT OF THE OUTE OUT OF THE OUTE OUT OF THE OUT OUT OUT OUT OUT OUT OUT OUT OUT OUT	01 210 111110 0011	I	_
PARAMETER	MAX or MIN	LS	UNIT
lcc	MAX	55	mA
Іон	MAX	-1.2	mA
lou	MAX	24	mA

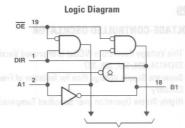
#### SWITCHING CHARACTERISTICS

PARAMETER	MAX or MIN	LS
fo	MAX	25

## 638

#### OCTAL BUS TRANSCEIVERS

- Bidirectional Bus Tranceivers
- Inverting Logic
- Outputs A-Bus: Open-Collector 3-State
- Schmitt-Triggered Inputs (SN74LS638)



To Seven Other Transceivers

#### **FUNCTION TABLE**

CONTROL INPUTS		OPERATION
ŌĒ	DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isoration

RECOMMENDED OPERATING CONDITIONS

					_
PARAMETER	MAX or MIN	LS	ALS	AS	UNIT
lccz	MAX	95	30	61	mA
ICCL	MAX	90	41	122	mA
Іон (В)	MAX	-15	-15	-15	mA
Von (A)	MAX	5.5	5.5	5.5	V
loL	MAX	24	24	64	mA
lot-	MAX		48		mA

\*638-1

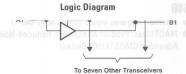
#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS
tPLH				10	12	7
tPHL .	A	A B MAX		15	12	6.5
tPLH .	В	A	MAN	25	25	20
tphl.	В	A	MAX	25	30	7
tPLH	ŌĒ		MAN	40	25	19
tPHL .	OE A		MAX	60	45	9
tpzh	ŌE	В	MANY	40	20	8
tPZL	UE	В	B MAX		22	10
tPHZ	ŌE	D.	MAY	25	10	7
tPLZ	UE	В	MAX	25	15	10

UNIT: ns

DWITCHING CHARACTERISTICS
PARAMETER MACK of MIN LS

#### Schmitt-Triggered Inputs (SN/4LS638)



**FUNCTION TABLE** 

CONTRO	L INPUTS	OPERATION
ŌĒ	DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
Н	X	Isoration

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	UNIT
Iccz	MAX	95	54	100	mA
Iccı	MAX	90	50	154	mA
Іон (В)	MAX	-15	-15	-15	mA
Von (A)	MAX	5.5	5.5	5.5	V
lou	MAX	24	24	64	mA
lor.	MAX		48	-	mA

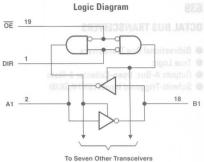
\*639-1

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS
tPLH	28 A EL	В	MAX	15	12	9.5
tPHL	T.E. I SE	D.	IVIAA	15	12	9
tPLH	88 B	A	MAY	25	30	22
tPHL .	В	A	MAX	25	22	9
tPLH	901 <u>0E</u> 84	A	MAX	40	30	21.5
tphl.	OE OE	A	MAX	50	35	11.5
tPZH	OE OE	В	NAV II	40	21	10.5
tPZL	UE	В	MAX	40	25	10.5
tPHZ	OE TO	В	MAY	25	10	7
tPLZ	UE	В	MAX	25	16	10.5

## **OCTAL BUS TRANSCEIVERS**

- Bidirectional Bus Tranceivers
- Inverting Logic
- 3-State Outputs
- Schmitt-Triggered Inputs (SN74LS640, 640-1)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



#### **FUNCTION TABLE**

CONTRO	L INPUTS	OPERATION					
ŌĒ	DIR			OPERATION			
L	L	B data to A bus					
L	H	A datato B bus					
H	X	Isoration					

PARAMETER	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	ACT 11	UNIT
lccz	MAX	95	50	80	0.08	0.16	0.08	0.16	11	0.25	80.0	mA
Iccı	MAX	90	55	123	0.08	0.16	0.08	0.16	94	30	0.08	mA
loн (A port)	MAX	-15	-15	-15	-6	-6	-6	-6	-3	-32	-24	mA
loн (B port)	MAX	-15	-15	-15	-6	-6	-6	-6	-15	-32	-24	mA
lot (A port)	MAX	24	24	64	6	6	6	6	24	64	24	mA
lot (B port)	MAX	24	24	64	6	6	6	6	64	64	24	mA
lor.	MAX	48	48	-	-	-		-	-	*80		mA

\*640-1

SWITCHING CHAR	ACTERISTICS									591193	HE LIAN	AND DE	HIGHN
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	ACT 11
tPLH	A	В	MAX	10	11	7	26	27	28	33	6.5	4.9	10.5
tphL .	A	В	IVIAA	15	10	6	26	27	28	33	3.7	4.9	9.5
tplH .	В	A	MAX	10	11	. 7	26	27	28	33	6.5	4.9	10.5
tPHL	В	A	WAA	15	10	6	26	27	28	33	3.7	4.9	9.5
tPZH	ŌE		MAN	40	21	8	58	45	58	45	10.2	5.8	13.4
tPZL	UE	A	MAX	40	24	10	58	45	58	45	10.7	7.3	13.6
tPHZ	ŌE		MANY	25	10	8	38	45	50	45	10.2	6.8	13.9
tPLZ	ÜE	A	MAX	25	15	13	38	45	50	45	7.8	5.5	14.2
tPZH	ŌE		MAN	40	21	8	58	45	58	45	10.2	5.8	13.4
tPZL	UE	В	MAX	40	24	10	58	45	58	45	10.7	7.3	13.6
tPHZ	ŌE		MAN	25	10	8	38	45	50	45	10.2	6.8	13.9
tPLZ	UE	В	MAX	25	15	13	38	45	50	45	7.8	5.5	14.2

#### **OCTAL BUS TRANSCEIVERS**

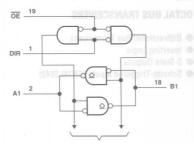
- Bidirectional Bus Tranceivers
- True Logic
- 3-State Outputs
- Schmitt-Triggered Inputs (SN74LS641)



#### **FUNCTION TABLE**

CONTRO	L INPUTS	OPERATION	
G	DIR	OPERATION	
L	L	B data to A bus	
L	H	A datato B bus	
Н	X	Isoration	





To Seven Other Transceivers

RECOMMENDED OPERATING CONDITIONS

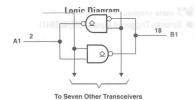
PARAMETER	MAX or MIN	LS	ALS	AS	UNIT
lccz	MAX	95	-	-	mA
Iccl	MAX	90	47	136	mA
Voн	MAX	5.5	5.5	5.5	V
lou	MAX	24	24	64	mA
lor.	MAX	48	48	-	mA

<sup>\*641-1</sup> 

CANITCHING CHARACTERISTICS

SWITCHING CHAR	ACTERISTICS		10000				
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	
tPLH .			MAX	25	25	21	
tPHL .	А	В	IVIAA	25	18	7.5	
tPLH .			MAX	25	25	21	
tPHL .	В	A		25	18	7.5	
tPLH .	ŌE	4.0	MAN	40	30	21	
tPHL .	UE	A,B	MAX	50	30	9	
tPLH .	DID	4.0	144V	40	32	22	
tPHL .	DIR A,B MAX		MAX	50	32	10	

## Schmitt-Triggered Inputs (SN74LS642)



**FUNCTION TABLE** 

CONTRO	L INPUTS	OPERATION	
ŌĒ	DIR		
L	L	B data to A bus	
L	H	A data to B bus	
H	X	Isoration	



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	UNIT
lccz	MAX	95	-		mA
ICCL	MAX	90	28	104	mA
Vон	MAX	5.5	5.5	5.5	V
lou	MAX	24	24	64	mA
lor.	MAX	48	48		mA

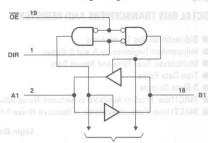
\*642-1

SWITCHING CHARACTERISTICS

INPUT	OUTPUT	MAX or MIN	LS	ALS	AS
		MAN 20	25	30	24
А	В	IVIAX	25	22	7.5
В	А	MAX	25	30	24
			25	22	7.5
OF DID		MAN	40	30	23.5
UE, DIK	A	IVIAX	60	38	11.5
OF DID		MAN	40	30	23.5
UE, DIK	В	WAX	60	38	11.5
	A B OE, DIR	A B B A  OE, DIR A	A         B         MAX           B         A         MAX           OE, DIR         A         MAX	A B MAX 25 B A MAX 25 0E, DIR A MAX 40 0E DIR B MAX 40	A B MAX 25 30 25 22 B A MAX 25 30 0E, DIR A MAX 40 30

## OCTAL BUS TRANSCEIVERS

- Bidirectional Bus Tranceivers
- True Logic
- 3-State Outputs
- Schmitt-Triggered Inputs (SN74LS645, 645-1)



To Seven Other Transceivers

**FUNCTION TABLE** 

OPERATION	CONTROL INPUTS		
OPERATION	DIR	ŌĒ	
B data to A bu	L	L	
A data to B bu	H	L	
Isoration	X	H	

RECOMMENDED OPERATING CONDITIONS

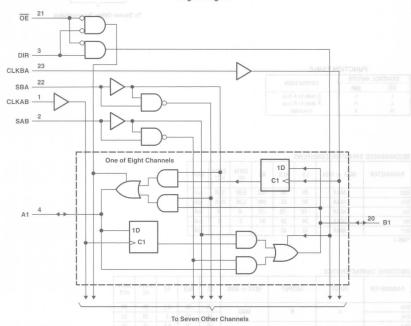
HEOOMHHEITBED	OT ENDTHING GOTT	DITTO TE	1	_	_	_	_
PARAMETER	MAX or MIN	LS	ALS	AS	SN74 HC	SN74 HCT	UNIT
lccz	MAX	95	58	123	0.08	0.08	mA
lcci	MAX	90	55	149	0.08	0.08	mA
Іон	MAX	-15	-15	-15	-6	-6	mA
lou ne	MAX	24	24	64	6	6	mA
ln:*	MAX	48	48	-			mA

\*645-1

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	SN74 HC	SN74 HCT
tPLH	Α	В	MAN	15	10	9.5	26	28
tPHL .			MAX	15	10	- 9	26	28
tPLH	В	А	644V	15	10	9.5	26	28
tPHL .			MAX	15	10	9	26	28
tPZH	ŌĒ	THAA THA	MAX	40	20	11	58	58
tPZL				40	20	10	58	58
tPHZ	ŌĒ		MAX	25	10	7	50	50
tPLZ	OE	A		25	15	12	50	50
tPZH	ŌE	38 18-	MAX	40	20	11	58	58
tPZL.	OE .	ы В		40	20	10	58	58
tPHZ	ŌE	В	MAY	25	10	7	50	50
tPLZ	UE		MAX	25	15	12	50	50

- Bidirectional Bus Tranceivers
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- True Data Paths
- 3-State Outputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



PARAMETER	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	ABT Ver.A	LVTH 3V	UNIT
lcc	MAX	165	88	211	0.08	0.16	0.08	0.08	67	30	30	5	mA
Іон	MAX	-15	-15	-15	-6	-6	-6	-6	-15	-32	-32	-32	_mA
lou	MAX	24	24	48	6	6	6	6	64	64	64	64	mA
OL*	MAX	- 1	48	98 -	1-1	01-	25*	-	- 2	-	-		mA

			100				
PARAMETER	MAX or MIN	AC 11	CD74 AC	ACT 11	CD74 ACT	LVC 3V	UNIT
Icc	MAX	0.08	0.08	0.08	0.08	0.01	mA
Іон	MAX	-24	-24	-24	-24	-24	mA
lou	MAX	24	24	24	24	24	mA
lor.	MAX		-	-	-	-	mA

					FUNCI	ION IMPL	- Lin	
		INP	UTS			DATA	1/O†	
OE	DIR	CLKAB	CLKBA	SAB	SBA	A1-A8	B1-B8	OPERATION OR FUNCTION
H	X	H to L	H to L	X	X	Input Input	Input Input	Isolation Store A and B data
L	L	X X	X H to L	X X	L H	Output Output	Input Input	Real-time B data to A bus Stored B data to A bus
L	Н	X H to L	X	L	X	Input Input	Output Output	Real-time A data to B bus Stored A data to B bus

<sup>†</sup> The data output functions can be enabled or disabled by various signals at OE and DIR. Data input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

## SWITCHING CHARACTERISTICS

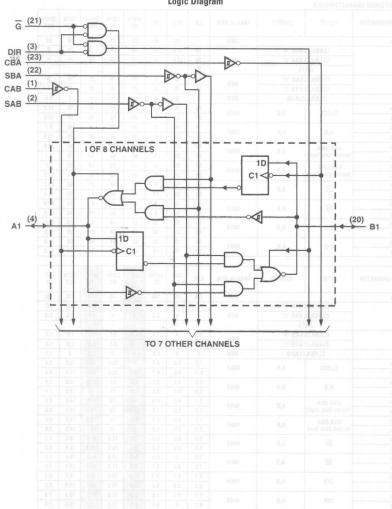
							01174	0074	04174	0074	0.117
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT
fmax			MIN	-	40	90	27	25	27	20	83
	CLKBA,CLK	AB "H"		15	12.5	5	19	20	19	31	6
tw	CLKBA,CLK	AB "L"	MIN	30	12.5	6	19	20	19	31	6
	DATA	4		30	-			-	-	-	-
	CLKBA,CLK	AB "H"	MIN	15	10	6	25	15	25	15	6
tsu	CLKBA,CLK	(AB "L"	MIN	15	10	6	25	15	25	15	6
th	CLKBA,C	LKAB	MIN	0	0	0	5	9	5	5	0.5
tplH.	NOON.	4.0	2447	25	30	8.5	45	55	45	55	11.2
tphl.	CLOCK	A,B	MAX	35	17	9	45	55	45	55	10.6
tPLH	4.0		1111	18	20	9	34	34	34	46	9.5
tphl .	A,B	B,A	MAX	20	12	7	34	34	34	46	10.5
tPLH .	SAB,SBA	A D	MAX	40	25	11	48	43	48	58	13.8
tPHL .	(sored data high)	A,B	MAX	35	20	9	48	43	48	58	9.1
tPLH	SAB,SBA	4.0		50	35	11	48	43	48	58	12
tphL .	(sored data low)	A,B	MAX	25	20	9	48	43	48	58	12.9
tpzH	ŌĒ	A D	BAAN.	55	17	9	61	44	61	56	13.2
tPZL	UE	A,B	MAX	65	20	14	61	44	61	56	14.4
tрнz	ŌĒ	A D	MAX	35	10	9	61	44	61	44	10.9
tPLZ	UE	A,B	IVIAX	35	16	9	61	44	61	44	10.5
tpzH	DIR	A,B	MAX	45	30	16	61	44	61	56	13.1
tPZL	UIK	A,B	IVIAX	60	25	18	61	44	61	56	14.6
tPHZ	DIR	A D	MAX	30	10	10	61	44	61	44	12.6
tPLZ	DIK	A,B	IVIAX	30	16	10	61	44	61	44	11.8

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ABT A Ver.	LVTH 3V	AC 11	CD74 AC	ACT 11	CD74 ACT	3V LVC
fmax			MIN	125	125	150	100	125	105	110	150
	CLKBA,CLI	KAB "H"		4	4	3.3	- 5	4	4.8	4.5	3.3
tw	CLKBA,CL	KAB "L"	MIN	4	4	3.3	5	4	4.8	4.5	3.3
	DAT	A	1	1	12.7	- 1		-	-	7. 1	1 4
	CLKBA,CLI	KAB "H"	MIN	3.5	3	1.2	4.5	2.5	4.5	2.5	1.5
tsu	CLKBA,CL	KAB "L"	IVIIIN	3	3	1.6	4.5	2.5	4.5	2.5	1.5
th	CLKBA,C	LKAB	MIN	0	0	0.8	1	2	2.5	2	1.7
tplH	CLOCK	A D	MAX	7.8	5.6	4.7	11	13.5	13.5	15.5	8.4
tphL .	CLUCK	A,B	IVIAX	8.4	5.6	4.7	12.2	13.5	14.9	15.5	8.4
tPLH	A.B	D. A.	MAX	6.9	4.8	3.5	8.8	11	11.5	12.5	7.4
tPHL .	A,B	B,A	IVIAA	6.9	5.4	3.5	9.8	-11	12	12.5	7.4
tPLH	SAB,SBA	4.0	MAX	7.1	6.5	4.9	9.4	12	11.5	14.5	8.6
tPHL .	(sored data high)	A,B	IVIAA	7.9	5.9	4.9	10.7	12	13.5	14.5	8.6
tplH	SAB,SBA	A,B	MAX	7.1	6.5	4.9	9.9	12	12.4	14.5	8.6
tPHL	(sored data low)	A,B	MAX	7.9	5.9	4.9	11	12	13.1	14.5	8.6
tPZH	ŌĒ	A,B	MAX	6.3	6.3	5.2	12	13.5	14.4	15.5	8.2
tpzi.	UE	A,B	IVIAX	8.8	8.8	5.2	13.1	13.5	15.3	15.5	8.2
tрнz	ŌĒ	A,B	MAX	8.3	5	5.5	8.9	13.5	11.6	15.5	7.5
tplz	UE	A,b	IVIAA	7.5	4.5	5.5	8.3	13.5	10.6	15.5	7.5
tPZH	DIR	A,B	MAY	6.7	6.7	5.2	12.6	13.5	15.3	15.5	8.3
tPZL	1 DIK	A,B	MAX	9.5	9.5	5.2	13.7	13.5	16.5	15.5	8.3
tPHZ	DIR	A D	MAN	7.7	5.7	5.6	8.7	13.5	11.3	15.5	7.9
tPLZ	DIK	A,B	MAX	8.2	6	5.6	8.1	13.5	10.3	15.5	7.9

UNIT fmax : MHz other : ns

## **OCTAL BUS TRANSCEIVERS AND REGISTERS**

- Bidirectional Bus Tranceivers
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- True Data Paths
- Open-Collector Outputs



FUNCTION	TARLE

INPUTS	DATA I/O†	OPERATION OR FUNCTION
the Bure terroupale le étorad on audit jour-to-pion transition of the cior	w innus	OPERATION OR FUNCTION

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
Icc	MAX	150	mA
Voн	MAX	5.5	V
lou	MAX	24	mA

### SWITCHING CHARACTERISTICS

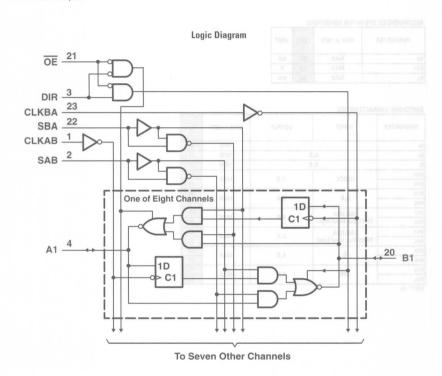
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
tw			MIN	30
tsu	A,B		MIN	15
th	A,B		MIN	0
tPLH .	CLOCK	A D	MAX	35
tphL .	CLUCK	A,B	IVIAX	45
tplH .	- A,B	B,A	MAX	26
tPHL .		D,A	MAX	27
tPLH	SAB,SBA	A,B	MAX	50
tPHL .	(With Bus Input High)	A,B	IVIAA	45
tplH	SAB,SBA	A,B	MAX	60
tPHL .	(With Bus Input Low)	A,D	IVIAA	30
tPLH ne	- G	A,B	MAX	40
tPHL .	- 6	A,D	IVIAA	50
tPLH	DIR	A,B	MAX	35
<b>TPHL</b>	DIK	M,D	WAX	40

UNIT: ns

a Seven Other Channels

# **OCTAL BUS TRANSCEIVERS AND REGISTERS**

- Bidirectional Bus Tranceivers
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Inverting Data Paths
- 3-State Outputs



					1 01401	TON TABL	- bar		
		INF	UTS			DATA	A I/O†	OPERATION OR FUNCTION	
ŌĒ	DIR	CLKAB	CLKBA	SAB	SBA	A1-A8	B1-B8	OPERATION OR FUNCTION	
H	X	H to L	H to L	X	X	Input Input	Input Input	Isolation Store A and B data	
L L	L L	X	X H to L	×	L H	Output Output	Input Input	Real-time B data to A bus Stored B data to A bus	
L	Н	X	X	L	X	Input	Output	Real-time A data to B bus	

† The data output functions can be enabled or disabled by various signals at OE and DIR. Data input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

#### RECOMMENDED OPERATING CONDITIONS

RECOMMENDED OPE	RATING CONDITIO	N2	_			-	į-
PARAMETER	MAX or MIN	LS	ALS	AS	SN74 HC	SN74 HCT	UNIT
lcc	MAX	180	88	195	0.08	0.08	mA
Іон	MAX	-15	-15	-15	-6	-6	mA
lou	MAX	24	24	48	6	6	mA

#### SWITCHING CHARACTERISTICS

SWITCHING CHA	ARACTERISTICS			_			No.	
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	SN74 HC	SN74 HCT
fmax			MIN	-	40	90	27	27
	CLKAB, CL	KBA "H"	MIN	15	12.5	5	19	19
tw	CLKAB, CL	KBA "L"	MIN	30	12.5	6	19	19
	DAT	Ά	MIN	30				
tsu	CLKAB, C	CLKBA	MIN	15	10	6	25	25
th	CLKAB, C	CLKBA	MIN	0	0	0	5	5
tPLH .	CLOCK	4.0	MAX	25	33	8.5	45	45
tPHL .	CLUCK	A,B	MAX	40	20	9	45	45
tPLH	4.0	D 4		18	17	8	34	34
tPHL .	A,B	B,A	MAX	25	10	7	34	34
tPLH	SAB,SBA	4.0	1111	55	25	-11	48	48
tPHL .	(With Bus Input High)	A,B	MAX	40	21	9	48	48
tPLH .	SAB,SBA			40	39	. 11	48	48
tPHL .	(With Bus Input Low)	A,B	MAX	40	22	9	48	48
tPZH	ŌĒ	100	1	50	22	9	61	61
tPZL	OE	A,B	MAX	55	22	15	61	61
tPHZ	ŌĒ	4.0		45	10	9	61	61
tPLZ	OE .	A,B	MAX	35	15	9	61	61
tPZH	DIR		MAX	40	27	16	61	61
tPZL	DIK	A,B	MAX	45	19	18	61	61
tPHZ	DID	4.0	1444	35	14	10	61	61
tPLZ	DIR	A,B	MAX	30	15	10	61	61

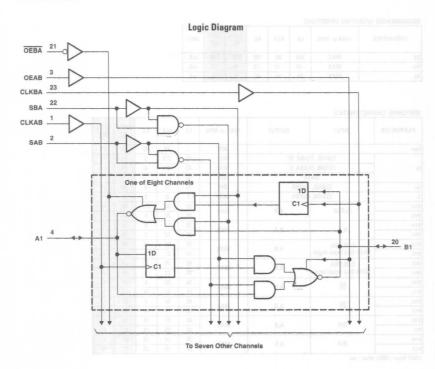
UNIT fmax : MHz other : ns

OCTAL BUS TRANSER

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· Inverting Data Paths

- 651 Inverting Data Paths 3-State Outputs



		INP	UTS			DATA	. VO	OPERATION OF FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1-A8	B1-B8	OPERATION OR FUNCTION
L	Н	H to L	H to L	×	X	Input Input	Input Input	Isolation Store A and B data
X	Н	<b>†</b>	H to L	X	X	Input Input	Unspecified Output	Store A, hold B Store A in both registers
L	X L	H to L	<b>†</b>	×	X X	Unspecified Output	Input Input	Hold A, store B Store B in both registers
L	L L	X	X H to L	X	L H	Output Output	Input Input	Real-time B data to A bus Stored B data to A bus
Н	H	X H to L	×	L H	X X	Input Input	Output Output	Real-time A data to B bus Stored A data to B bus
н	L	H to L	H to L	Н	н	Output	Output	Stored A data to B bus and stored B data to A bus

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	SN74 HC	SN74 HCT	SN74 BCT	ABT	CD74 ACT	UNIT
Icc	MAX	165	82	195	0.08	0.08	62	30	160	mA
Іон	MAX	-15	-15	-15	-6	-6	-15	-32	-24	mA
lou	MAX	24	24	48	6	6	64	64	24	mA
lor.	MAX		48	200	-				-	mA

\*651-1

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	SN74 HC	SN74 HCT	SN74 BCT	ABT	CD74 ACT
fmax			MIN	1	40	90	27	20	85	125	110
	CLKBA, CLK	(AB "H"	MIN	15	12.5	5	19	25	4.8	4	4.5
tw	CLKBA, CLI	(AB "L"	MIN	15	12.5	6	19	25	7	4	4.5
	DATA	4	MIN	15	1 1	-					-
tsu	A,B		MIN	15	10	6	25	19	6	3	2.5
th	A,B		MIN	0	0	0	5	5	1	0	2
tPLH .	CLOCK	A,B	MAX	24	32	8.5	45	45	11.7	5.6	15.5
tPHL	CLUCK	A,D	IVIAA	35	17	9	45	45	11.8	5.6	15.5
tPLH	A,B	B.A	MAX	18	18	9	34	34	12.6	6.2	12.5
<b>TPHL</b>	A,B	D,A	IVIAX	30	10	7	34	34	9.8	5.4	12.5
tPLH .	SAB,SBA	A,B	MAX	47	38	11	48	48	9.8	6.5	15.5
tphl.	(With Bus Input High)	A,B	MAX	33	21	9	48	48	15.5	5.9	15.5
tPLH .	SAB,SBA	A,B	MAX	35	25	11	48	48	14.6	6.5	15.5
tphi.	(With Bus Input Low)	A,D	MAX	30	21	9	48	48	12.8	5.9	15.5
tPZH	OEBA	А	MAX	44	20	10	61	61	12	5.8	15.5
tPZL	UEDA	А	WAX	60	18	16	61	61	13.1	8.5	15.5
tPHZ	OEBA	A	MAX	38	9	9	61	61	10.2	5	15.5
tPLZ	UEBA	A	WAX	30	12	9	61	61	9.6	4.1	15.5
tPZH	OEAB	В	MAX	29	22	11	61	61	8.3	6.5	15.5
tPZL	ULAB	D	WAX	40	21	16	61	- 61	9.7	7.4	15.5
tPHZ	DEAB	В	MAX	38	12	10	61	61	15	5.5	15.5
tPLZ	UEAB	В	IVIAX	30	14	11	61	61	12.3	5.1	15.5

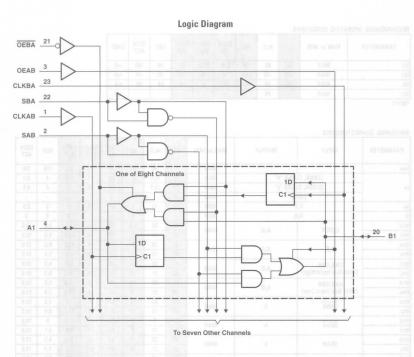
UNIT fmax : MHz other : ns

Multiple W

● 74AC11x

# OCTAL BUS TRANSCEIVERS AND REGISTERS

- Bus Tranceivers / Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- True Data Paths
- 3-State Outputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



	FUNCTION	TABLE	
т		DATE	

	.E	<b>FUNCTION TABL</b>						
	TA I/O	DA			UTS	INP		
OPERATION OR FUNCTION	B1-B8	A1-A8	SBA	SAB	CLKBA	EBA CLKAB		OEAB
Isolation Store A and B data	Input Input	Input Input	X	X	H to L ↑	H to L	H	L
Store A, hold B Store A in both registers	Unspecified Output	Input Input	×	×	H to L	† †	Н	Х
Hold A, store B Store B in both registers	Input Input	Unspecified Output	×	×	†	H to L ↑	X L	L
Real-time B data to A bus Stored B data to A bus	Input Input	Output Output	L H	×	X H to L	×	L L	L
Real-time A data to B bus Stored A data to B bus	Output Output	Input Input	×	L H	X	X H to L	H	Н
Stored A data to B bus and stored B data to A bus	Output	Output	н	н	H to L	H to L	L	Н

PARAMETER	MAX or MIN	LVTH 3V	AC 11	CD74 AC	ACT 11	CD74 ACT	LVC 3V	UNIT
Icc	MAX	5	0.08	0.16	0.08	0.16	0.01	mA
Гон	MAX	-32	-24	-24	-24	-24	-24	mA
lou	MAX	64	24	24	24	24	24	mA

SWITCHING CHARACTERISTICS

OEBA

OEAB

OEAB

A

В

tPZL tPHZ tPLZ tPZH tPZL tPHZ tPHZ Outputs A Bus: Open-Collector B Bus: 3-State

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	
fmax			MIN		40	90	27	20	20	17	77	
	CLKBA, CL	KAB "H"	MIN	15	12.5	5	19	24	25	38	6.5	
tw	CLKBA, CL	KAB "L"	MIN	15	12.5	6	19	24	25	38	6.5	
	DAT	ΓΑ	MIN	15	~ :	- 1	-	-	-	-00		1
tsu .	A,B I	High	MIN	15	10	6	25	18	19	18	5	43
tsu .	A,B I	Low	MIN	15	10	6	25	18	19	18	5	
th	A,i	В	MIN	0	0	0	5	11	5	5	1	000
tplh	CLOCK	A,B	MAX	25	30	8.5	45	66	45	66	10.5	RE
tphl .	CLUCK	A,D	IVIAA	36	17	9	45	66	45	66	9.9	
tplH	A,B	B,A	MAX	18	18	9	34	41	34	56	8.9	P
tphl.	A,D	D,A	IVIAA	20	12	7	34	41	34	56	9.8	1
tplh	SAB,SBA	A,B	MAX	35	35	11	48	51	48	69	13.1	148
tphl.	(With Bus Input High)	A,D	WAX	32	20	9	48	51	48	69	8.5	
tplH	SAB,SBA	A,B	MAX	50	25	11	48	51	48	69	11.3	1
tphl.	(With Bus Input Low)	A,b	IVIAX	23	20	9	48	51	-48	69	12.5	1
tPZH .	OEBA	Δ.	MAX	45	17	10	61	53	61	68	10.6	1
PZH	UEBA	- Gr A	WAX	54	18	16	61	53	61	68	12	1

MAX

MAX

MAX

38 10

30 16

30

38

38

22

18 16 61

61 53 61 53 10

61

11 61

53 61 53 53 61 68

10 10 61 53 61 53 11.6

30 16 11 61 53 61 53 11.3

53 61 68 9.3

9.5

8.1

PARAMETER	INPUT	ОИТРИТ	MAX or MIN	ABT	ABT Ver.A	LVTH 3V	AC 11	CD74 AC	ACT 11	CD74 ACT	3V LVC
fmax			MIN	125	125	150	105	125	105	110	100
	CLKBA, CI	LKAB "H"	MIN	4	4	3.3	4.8	4	4.8	4.5	3.3
tw	CLKBA, C	LKAB "L"	MIN	4	4	3.3	4.8	4 .	4.8	4.5	3.3
	DA	TA	MIN	-		-		7.1	-	-	-
tsu	A,B	High	MIN	3.5	3	1.2	4.5	2.5	4	2.5	1.9
tso	A,B	Low	MIN	3.5	3	1.6	4.5	2.5	4	2.5	1.9
th	A,	В	MIN	0	0	0.8	1	2	2.5	2	1.7
tplh	CLOCK	A,B	MAX	7.8	5.6	4.7	10.7	13.5	13.1	15.5	8
tphl	CLUCK	A,D	IVIAA	8.4	5.6	4.7	12	13.5	14.4	15.5	8
tPLH	A,B	B,A	MAX	6.7	4.8	3.5	8.6	11	11.1	12.5	7.4
tphl.	A,D	D,A	IVIAX	6.7	5.4	3.5	9.6	11	11.6	12.5	7.4
tPLH	SAB,SBA	A,B	MAX	6.9	6.5	4.9	9.1	12	11	14.5	8.7
tPHL .	(With Bus Input High)	A,D	IVIAA	7.7	5.9	4.9	10.7	12	13.3	14.5	8.7
tPLH	SAB,SBA	A,B	MAX	6.9	6.5	4.9	9.9	12	12.2	14.5	8.7
tphl .	(With Bus Input Low)	A,D	IVIAA	7.7	5.9	4.9	10.9	12	12.6	14.5	8.7
tрzн	OEBA	A	MAX	5.8	5.8	5.2	10.9	13.5	12.6	15.5	7.4
tPZL	UCDA	M	IVIAA	8.5	8.5	5.2	12.2	13.5	13.8	15.5	7.4
tрнz	OEBA	A	MAX	8.2	5	5.5	7.6	13.5	9.9	15.5	7.5
tplz.	ULDA	A	IVIAA	6.8	4.1	5.5	7.1	13.5	9.3	15.5	7.5
tpzH	- OEAB	В	MAX	6.5	6.5	4.7	11.3	13.5	15.2	15.5	7.1
tpzl	ULMB	υ .	IWIAA	7.4	7.4	4.7	12.3	13.5	16.1	15.5	7.1
tPHZ	OEAB	В	MAX	6.9	5.5	5.6	7.6	13.5	10.3	15.5	7.4
tPLZ	ULAD	0	WIAA	6.2	5.1	5.6	7.2	13.5	9.3	15.5	7.4

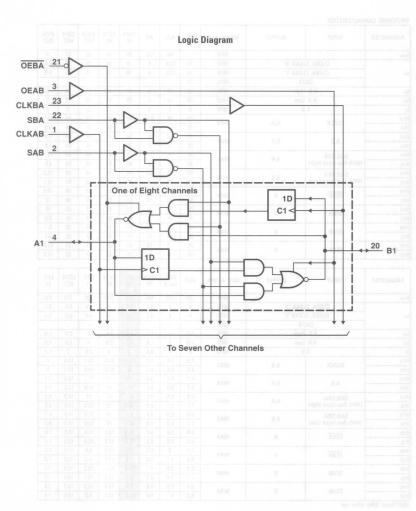
UNIT fmax : MHz other : ns

# **OCTAL BUS TRANSCEIVERS AND REGISTERS**

- Bus Tranceivers / Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Inverting Data Paths
- Outputs

A Bus: Open-Collector

B Bus: 3-State



L	L	1		^	FIII	NCTION TABLE		
L L	L	×	X H or L	×	L H	Output	Input	Real-time B data to A bus Stored B data to A bus
Н	Н	X	X	L	X	Input	Output	Real-time A data to B bus
Н	H	HorL	X	H	X	Input	Output	Stored A data to B bus
Н	L	H or L	H or L	Н	Н	Output	Output	Stored A data to B bus and stored B data to A bus

NOTES:

1 The data output functions can be enabled or dissabled by a variety of level combinations at GAB or GBA. Data input functions always are enabled; i.e., data at the bus terminals is storedd on every low-to-high transition on the clock inputs.

\$ Select control = 1: clocks can occur simultaneously.

Select control = 1: clock must be staggered to load both registers.

#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	UNIT
Icc	MAX	165	88	mA
Іон	MAX	-15	-15	mA
lou	MAX	24	24	mA

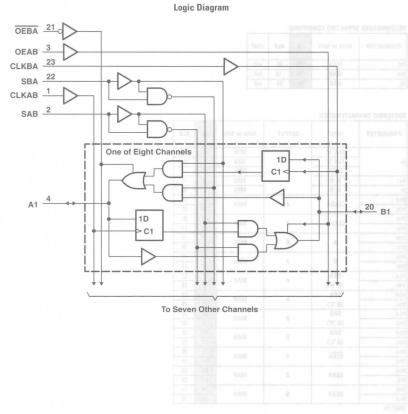
SWITCHING CHAP	ACTERISTICS				
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS
	CLK "H"		MIN	15	14.5
tw	CLK "L"	10	MIN	30	14.5
	DATA		MIN	30	-
tsu	A, B	1	MIN	15	10
th	A, B	N	MIN	0	0
tPLH	CLKDA		MAN	38	64
tPHL .	CLKBA	A	MAX	39	22
tPLH .	OLIVAD	-	MAY	23	30
tPHL .	CLKAB	В	MAX	36	17
tPLH		-	1447	18	18
<b>TPHL</b>	A	В	MAX	30	15
tPLH	В			32	56
tPHL	В	A	MAX	24	15
tPLH	SBA		MAY	57	62
tPHL .	(B "H")	A	MAX	39	25
tPLH	SBA		MAY	51	62
tphl.	(B "L")	A	MAX	35	25
tPLH	SAB	В	MAX	48	35
tPHL .	(A "H")	В	IVIAX	33	22
tPLH .	SAB		1447	36	25
tPHL .	(A "L")	В	MAX	30	22
tPLH	OEBA		MAN	35	30
tPHL .	UEBA	A	MAX	55	24
tPZH	OFAR		MAN	29	22
tPZL	0EAB	В	MAX	38	22
tPHZ	OFAR	D	MAY	39	14
tPLZ	0EAB	В	MAX	29	16

UNIT:ns

- Bus Tranceivers / Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- True Data Paths
- Outputs

A Bus: Open-Collector

B Bus: 3-State



						2.7	110			
		INP	UTS			DATA	4 1/0	OPERATION OR FUNCTION		
DEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1-A8	B1-B8	OF EMAILOR OF TOROTTO		
L	H	H to L ↑	H to L	X	X	Input Input	Input Input	Isolation Store A and B data		
X	H	<b>↑</b>	H to L	X	×	Input 9 800	Unspecified Output	Store A, hold B Store A in both registers		
L	X L	H to L	1	X	X	Unspecified Output	Input Input	Hold A, store B Store B in both registers		
L L	L L	X	X H to L	X	L H	Output Output	Input Input	Real-time B data to A bus Stored B data to A bus		
Н	Н	X H to L	X	L H	×	Input Input	Output	Real-time A data to B bus Stored A data to B bus		
Н	L	H to L	H to L	н	н	Output	Output	Stored A data to B bus and stored B data to A bus		

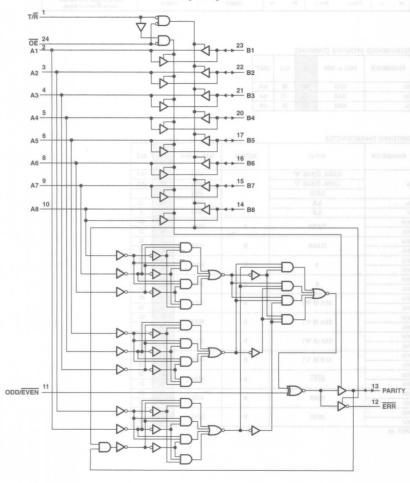
## RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	UNIT
Icc	MAX	180	88	mA
Іон	MAX	-15	-15	mA
loL	MAX	24	24	mA

### SWITCHING CHARACTERISTICS

SWITCHING CHAIN	CTEMOTICS	GB - 4-3			
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS
	CLKBA, CLKAB "H"		MIN	15	14.5
tw	CLKBA, CLKAB "L"	15 87	MIN	30	14.5
-	DATA	_	MIN	30	
tsu	A,B	14	MIN	15	10
th	A,B	88	MIN	0	0
tPLH .	OLKDA		1411	33	64
tPHL .	CLKBA	A	MAX	36	22
tPLH .	OLIVAR.		1447	21	30
tPHL .	CLKAB	В	MAX	33	17
tPLH .			1111	18	18
tPHL.	A — 🔾	В	MAX	30	15
tPLH .		I W. I	Jan.	27	56
tPHL	. B	A	MAX	21	21
tPLH .	004 (0.00)	(B "H") A		48	62
tPHL.	SBA (B "H")		MAX	32	25
tPLH .	004 (0.00		1411	54	62
tPHL	SBA (B "L")	A	MAX	29	25
tPLH	0.40 (4.888)		MAX	35	25
tPHL .	SAB (A "H")	'H") B		27	22
tPLH .	SAB (A "L")	В	MAX	45	35
tPHL .	SAB (A 'L')	В	IVIAX	21	22
tPLH .	OEBA		MAX	35	30
tPHL ST	UEBA	A	IVIAX	53	24
tPZH .	OFAR		MAN	29	22
tPZL	OEAB	В	MAX	33	22
tPHZ	OFAR	В	MAX	39	14
tPLZ	OEAB	В	WAX	29	16

UNIT: ns

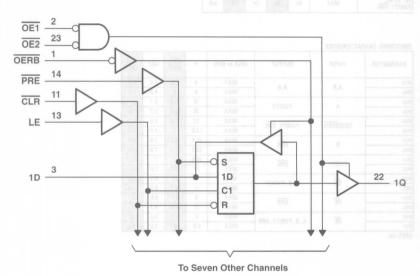


RECOMMENDED 0	PERATING CONDIT	TIONS				
PARAMETER	MAX or MIN	F	SN74 BCT	ABT	ACT 11	UNIT
Іссн	MAX	125	2	0.25	0.08	mA
ICCL	MAX	150	90	40	0.08	mA
Iccz	MAX	145	1	0.25	0.08	mA
Іон А1-А9	MAX	-3	-3	-32	-24	mA
IOH B1-B9, PARITY, ERR	MAX	-12	-15	-32	-24	mA
IoL A1-A8	MAX	24	24	64	24	mA
IOL B1-B8,	MAX	64	64	64	24	mA

MITCHING	CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	F	SN74 BCT	ABT	ACT 11
tPLH	4.0	D.A.	MAX	8	6.6	4.6	9.4
tPHL .	A,B	B,A	MAX	8	9	4.3	9.4
tPLH .	A	DADITY	MAX	16	15.4	8.1	14.4
tphL .	A	PARITY	MAX	16	15.9	7.7	15
tPLH	ODD/EVEN	PARITY FRR	MAX	12	7.1	4.9	10.7
tphL .	UDD/EVEN		MAX	12.5	9	4.9	11.3
tPLH	В	ERR	MAX	22.5	15.3	7.9	23.6
tPHL .			MAX	22.5	15.5	7.8	24.6
tplH	PARITY	ERR	MAX	16.5	13.2	7.7	14.6
tphl.	PARITY		MAX	17	13.9	7.5	14.7
tPZH	ŌĒ	A D DADITY	MAX	9	9.1	6.5	12.1
tPZL.	UE	A, B, PARITY	MAX	11	16.3	6.5	13.8
tPZH	ŌE	ERR	MAX	9	9.1	6.6	12.1
tPZL	UE	CHH	MAX	11	16.3	9.2	13.8
tPHZ	ŌE	A D DARITY FRR	MAX	8	9.1	6.2	12.1
tPLZ	UE	A, B, PARITY, ERR	MAX	6.5	8	7.8	11.6

- 3-State I/O-Type Read-Back Inputs
- True Outputs
- Bus-Structured Pinout



DECOMMENDED	OPERATING	CONDITION

	PARAMETER	MAX or MIN	ALS	UNIT					
Icc		MAX	73	mA					
	Q	MAX	-2.6	mA					
Іон	D	MAX	-0.4	mA					
	Q	MAX	24	mA					
loL	D	MAY	8	mΔ					

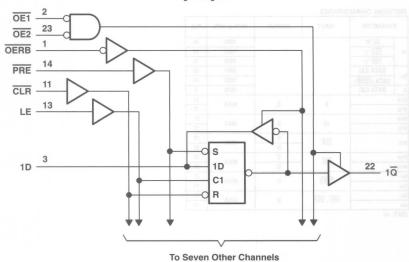
BIT D-TYPE TRANSPARENT READ-BACK LATE

- - Inverted Outputs
    - B Rus-Structured Pingut

Logic Diserem

,	PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
	LE "H"			MIN	10
tw	CLR "L"			MIN	10
	PRE "L"			MIN	10
tsu DA1	DATA (LE)			MIN	10
	DATA (OERB)			MIN	10
lh	DATA (LE)			MIN	5
tPLH		D	Q	MAX	14
PHL		U	u	IVIAA	18
PLH		LE	0	MAX	21
PHL	2	LL		WAX	27
tPHL		CLR	0	MAX	29
urnu		CLIT	D	WAX	32
tPLH		PRE	۵	MAX	22
tPHL		The state of the s	D	WAY G	28
ten	101	OERB	D	MAX	21
tdis		GEND		WIFA	14
ten		OE1, OE2	a	MAX	21
tdis		OLT, OLL		100.00	14

To Seven Other Channels



### RECOMMENDED OPERATING CONDITIONS

	PARAMETER	MAX or MIN	ALS	UNIT
lcc		MAX	79	mA
la.	۵	MAX	-2.6	mA
Іон	D	MAX	-0.4	mA
la.	O.	MAX	24	mA
lor	D	MAX	8	mA

## SWITCHING CHARACTERISTICS

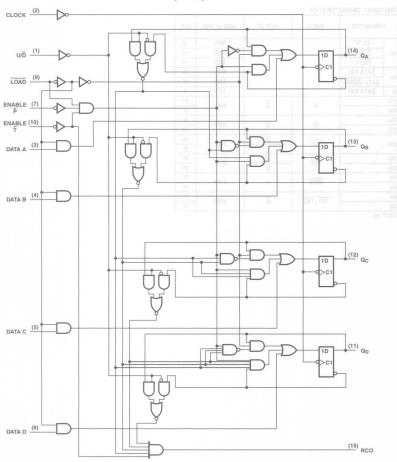
PARAMETER		INPUT OUTPUT		MAX or MIN	ALS
LE "H"				MIN	10
tw	CLR "L"			MIN	10
	PRE "L"			MIN	10
	DATA (LE)			MIN	10
tsu	DATA (OERB)			MIN	10
th	DATA (LE)			MIN	5
tPLH		D		MAX	20
tPHL .		U	ā	IVIAA	15
tPLH		LE Q		MAX	28
tPHL				IVIAA	22
tPHL	CLR Q		ā	MAX	24
urni	80	D Q		IVIAA	26
tPLH		PRE		MAX	25
tPHL		D		IVIAA	28
ten tdis		OERB	D	MAX	21
		UERB D		IVIAX	14
ten		OE1, OE2	ā	MAX	21
tdis		OLI, OEZ	u u	IVIAA	14

## UNIT: ns



# SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTER

- Fully Synchronous Operation for Counting and Programming
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading



RECOMMENDED	ODEDATING	COMPITIONS

HEOOMHEREE	01 218111110 0011		1
PARAMETER	MAX or MIN	LS	UNIT
Icc	MAX	34	mA
Іон	MAX	-0.4	mA
lo <sub>L</sub>	MAX	8	mA

SWITCHING CHARACTERISTICS

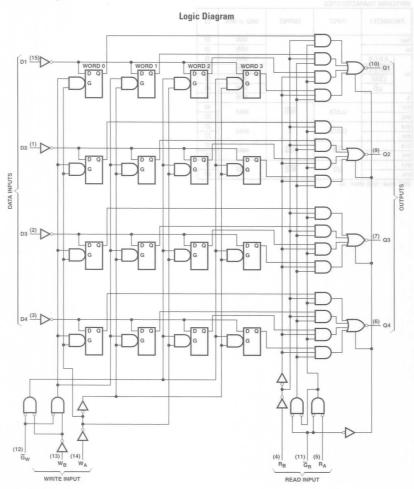
PA	RAMETER	INPUT OUTPUT		MAX or MIN	LS	
fmax		-(		MIN	25	
tw				MIN	20	
	A,B,C,D			MIN	25	
tsu	ENP,ENT			MIN	40	
tsu	LOAD			MIN	30	
	U/D			MIN	45	
th				MIN	0	
tPLH		CLOCK	RCO	MAX	40	
tPHL		CLUCK	nco	IVIAA	60	
tPLH		CLOCK	0	MAX	27	
tPHL		CLUCK	u	MAX	27	
tPLH		ENT	RCO	MAX	17	
tPHL	20 100	EIVI	nC0	WAX	45	
tPLH		U/D	RCO	MAX	35	
tPHL		0/0	ncu	IVIAX		

UNIT fmax : MHz other : ns

# 670

# **4-BY-4 REGISTER FILE**

- Separate Read / Write Addressing Permits Simultaneous Reading and Writing
- Organized as 4 Words of 4 Bits
- Expandable to 512 Words of n-Bits
- 3-State Outputs



WRI	TE INF	PUTS		WC	RD		
WB	WA	Gw	0	1	2	3	
L	L	L	Q = D	Qo	Q <sub>0</sub>	Q <sub>0</sub>	
L	H	L	Q <sub>0</sub>	Q = D	Qo	Q <sub>0</sub>	
Н	L	L	Q <sub>0</sub>	Q <sub>0</sub>	Q = D	Qo	
Н	H	L	Qo	Q <sub>0</sub>	Qo	Q = D	
~	V	ы	00	00	Oa	On	

READ INPUTS			OUTPUTS				
RB	RA	GR	Q1	Q2	Q3	Q4	
L	L	L	W0B1	W0B2	W0B3	W0B4	
L	Н	L	W1B1	W1B2	W1B3	W1B4	
Н	L	L	W2B1	W2B2	W2B3	W2B4	
Н	Н	L	W3B1	W3B2	W3B3	W3B4	
X	X	Н	Z	Z	Z	Z	



## RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	CD74 HC	CD74 HCT	UNIT
Icc	MAX	50	0.16	0.16	mA
Іон	MAX	-2.6	-6	-6	mA
lou	MAX	8	6	6	mA

## SWITCHING CHARACTERISTICS

STATE CHIEF CHAIL	ACTEMIONIO					
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	CD74 HC	CD74 HCT
tw			MIN	25	24	30
tsu (D)			MIN	10	18	18
tsu (W)			MIN	15	18	30
th (D)			MIN	15	5	5
th (W)			MIN	5	5	5
Datch			MIN	25	30	38
tPLH .	Read		111V	40	59	53
tPHL .	Select	Q.	MAX	45	59	53
tPLH .	Write	0	MAN	45	75	75
tPHL .	Enable	0	MAX	50	75	75
tPLH .		_	1411	45	75	75
tPHL .	Data	0	MAX	40	75	75
tPZH .	Read	Q	1447	35	45	57
tPZL.	Enable	u	MAX	40	45	57
tPHZ	Read	0	MAN	50	45	53
tPLZ	Disable	0	MAX	35	45	53

UNIT: ns

## **16-BIT SHIFT REGISTER**

- 16-Bit Serial-In, Serial-Out Shift Register with 16-Bit Parallel-Out Storage Register
- Performs Serial-to-Parallel Conversion

# **Logic Diagram** SER/Q15 16 PE† (7-11, 13-23) P0-P15 Q0-Q15 D0-D15 Y0-Y15 16 Y0-Y15 SH CLK (2) CLK 16BIT SER IN Q15 STORAGE 16-BIT SHIFT REGISTER MODE/STRCLK (5) STRCLR (4) † When PE is active, data synchronously parallel loaded into the shift registers form the 16 P inputs and no shifting takes place.

		INP	UTS				SHIFT REGISTER FUNCTIONS ST			STORAGE	REGISTER				
CS R/W	011.01.1/	OTDOLD	MODE/	SER/ Q15	SHIFT	READ FROM	WRITE INTO	PARALLEL	FUNC	TIONS					
CS	R/W	SH CLK	STRCLR	STRCLK	UIS	SHIFT	SERIAL INPUT	SERIAL INPUT	LOAD	CLEAR	LOAD				
Н	X	X	X	X	Z	NO	NO	NO	NO		NO				
X	X	X	L	X				1	Steine	YES	O-lains				
L	L	Į.	X	X	Z	YES	NO	YES	NO						
L	Н	X	×	X	Q15		YES	NO	HOIS		NO				
L	Н	1	X	L	Q14n	YES	YES	NO	NO		NO				
L	Н	1	L	X	L	NO	YES		YES	YES;	NO				
L	н	<u></u>	Н	X	Y15n	NO	YES		YES	NO	NO				
L	L	X	Н	+	Z		NO	S. STEPHER		NO	YES				

## RECOMMENDED OPERATING CONDITIONS

P	ARAMETER	MAX or MIN	LS	UNIT
Icc		MAX	80	mA
In	SER/Q15	MAX	-2.6	mA
Іон	Y0-Y15	MAX	-0.4	mA
lou	SER/Q15	MAX	24	mA
IOL	Y0-Y15	MAX	8	mA

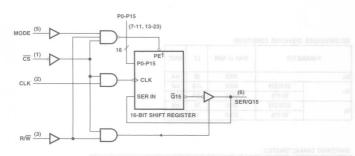
## SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	
fmax				MIN	20	
	CLK			MIN	20	
tw	CLR			MIN	20	
	SER/Q15			MIN	20	
tsu	Y0-Y15			MIN	20	
	Mode			MIN	35	
	R/W,CS			MIN	35	
	SER/Q15			MIN	0	
th	Y0-Y15			MIN	0	
	Mode			MIN	0	
tPLH		STRCLR	Y0-Y15	MAX	40	
tplH		MODE/	Y0-Y15	MAX	45	
tphl .		STRCLK	10-115	IVIAX	45	
tPLH tPHL		011 0114		MAX	33	
		SH CLK	SER/Q15	WAX	40	

UNIT fmax : MHz other : ns

# **16-BIT SHIFT REGISTER**

- 16-Bit Parallel-In, Serial-Out Shift Register
- Performs Parallel-to-Serial Conversion



† When PE is active	, data synchronously parallel loaded into the
shift registers form t	he 16 P inputs and no shifting takes place.

	hifting takes place.		

**FUNCTION TABLE** 

Ī		INF	UTS	SER/	OPERATION					
	CS	R/W	MODE	CLK	Q15	OFERATION				
	Н	X	X	X	Z	Do nothing				
	L	L	×	Į.	Z	Shift and write (serial load)				
	L	Н	L	<b>.</b>	Q14n	Shift and read				
	- 7	Н	Н		P15	narallel load				

# MATERIAL PROPERTY OF THE PROPE

12-Bit Address Competator with Enable

Logic Disuram

P/	ARAMETER	MAX or MIN	LS	UNIT
1.7	ANAIVIE I EN	WIAX OF WITH	LO	ON
CC		MAX	40	mA
lau.	SER/Q15	MAX	-2.6	mA
Іон	P0-P15	MAX	-0.4	mA
	SER/Q15	MAX	24	mA
lou	P0-P15	MAX	8	mA

## SWITCHING CHARACTERISTICS

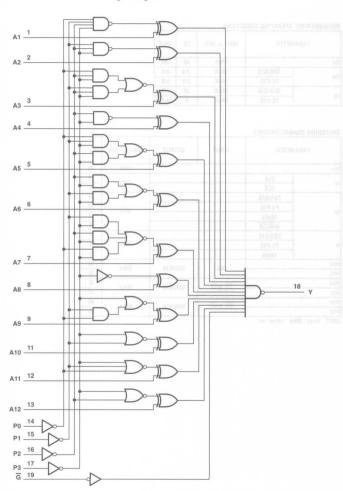
	TITALITA OTELLIO TIOO							
PA	RAMETER	INPUT	OUTPUT	MAX or MIN	LS			
fmax				MIN	20			
tw	CLK			MIN	20			
tw	CLR			IVIIIV	20			
	SER/Q15				20			
Su	P0-P15		4	MIN	20			
SU	Mode			IVIIIV	35			
	R/W,CS				35			
	SER/Q15			of Fil	0			
th .	P0-P15		1	MIN	0			
	Mode		- Marie	-(	0			
PLH	T.H		Н		SER/Q15	MAX	33	
tphL .		CLK	SEN/UIS	WAX	40			
tpzh	41.	CS, R/W	SER/Q15	MAX	45			
tPZL Y		03, N/VV	361/013	WAA	45			
tPHZ		CS, R/W	SER/Q15	MAX	40			
tPLZ		US, H/W SER/U		MAN	40			

UNIT fmax: MHz other:ns

# ADDRESS COMPARATOR

• 12-Bit Address Comparator with Enable





								" 17	0.10								
OUTPUT								UTS	INP								
Y	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	P0	P1	P2	P3	G
L	Н	Н	Н	Н	H	Н	Н	Н	Н	Н	Н	Н	L	L	L	L	L
L	Н	H	H	H	H	H	H	H	H	H	H	L	H	L	L	L	L
L	H	H	H	H	H	H	H	H	H	H	L	L	L	H	L	L	L
L	Н	H	H	H	H	H	H	H	H.	L	L	L	Н	H	L	L	L
L	Н	Н	Н	Н	Н	Н	Н	Н	L	L	L	L	L	L	Н	L	L
1	H	H	H	Н	H	H	H	L	L	L	L	L	H	L	Н	L	L
Derti	H	H	H	H	H	H	L	L	L	L	L	L	L	H	H	L	L
L	H	Н	Н	Н	H	L	L	L	L	L	L	L	H	Н	H	L	L
L	Н	Н	H	Н.,	L	L	L	L	L	L	L	L	L	L	L	Н	L
L	H	H	Н	L	L	L	L	L	L	L	L	L	H	L	L	Н	L
L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L	Н	L
L	Н	L	L	L	1	L	L	L	L	L	L	L	H	H	L	H	L
L	L	Н	Н	Н	L	L	L	L	L	L	L	L	L	L	Н	Н	L
L	L	H	Н	L	L	L	L	L	L	L	L	L	Н	L	H	Н	L
L	L	Н	L	L	L	L	-	L	L	L	L	L	L	H	H	.H.	L
L	L	L	L	L	L	L	L	L	L	L	L	L	Н	Н	Н	Н	L
Н							tions	mbina	her co	All of							L
H							on	nbinatio	ny com	Ar							Н

## RECOMMENDED OPERATING CONDITIONS

	_		_
MAX or MIN	ALS	SN74 HC	UNIT
MAX	28	0.08	mA
MAX	-2.6	-4	mA
MAX	24	4	mA
	MAX MAX	MAX 28 MAX -2.6	MAX 07 MIN ALS HC  MAX 28 0.08  MAX -2.6 -4

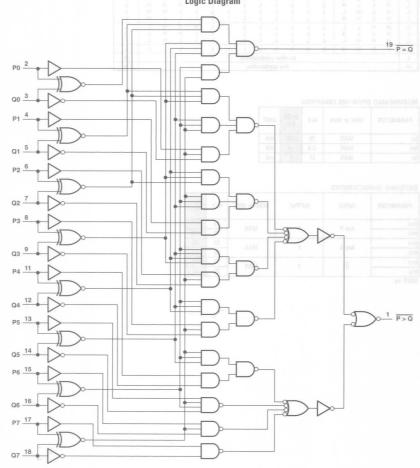
## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 HC
tPLH	A D	V	MAX	25	375
tphL .	Any P		IVIAX	35	375
tPLH	A A	V	MAN	22	78
tphL .	Any A	т.	MAX	30	78
tplH	G	Y	MAY	13	31
tphl.	G	Y	MAX	25	31

## UNIT: ns

- Totem-Pole Outputs
- Hysteresis at P and Q Inputs
- 20kΩ Pullup Resistors on the Q Inputs





FUNCTION TABLE

1 014	01101117	
DATA	OUT	PUTS
INPUT P, Q	P=Q	P>Q
P=Q	L	Н
P>Q	Н	L
P-0	н	Н

- - Totem-Pale Butputs
  - Hysterasis at P and Q Inputs

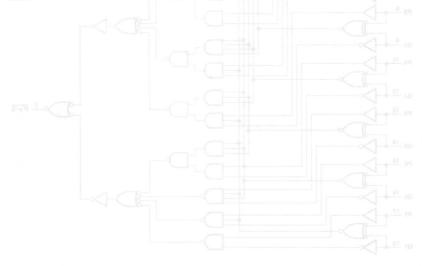
## RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	SN74 HC	UNIT
Icca	MAX	70	0.11	mA
Іон	MAX	-0.4	-4	mA
lou	MAX	24	- 4	mA

## SWITCHING CHARACTERISTICS

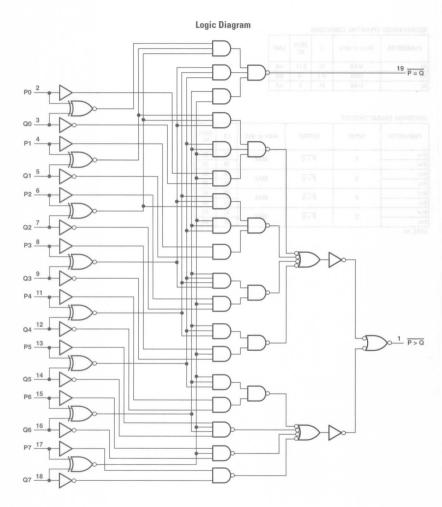
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	SN74 HC
tPLH .	P	P = 0	MAX	25	69
tphl.	P	P = U	IVIAX	25	69
tPLH .	0	P = 0	MAX	25	69
tphL .	и	P = U	IVIAX	25	69
tplh	Р	P > 0	MAX	30	69
tPHL .	r	r>u	IVIAA	30	69
tplh	н		MAX	30	69
tPHL .	u	P > 0	IVIAX	30	69

### UNIT: ns



- Totem-Pole Outputs
- Hysteresis at P and Q Inputs





FUNCTION TABLE

DATA	OUT	PUTS	
INPUT P, Q	P=Q	P>Q	
P=Q	L	Н	
P>Q	Н	L	
D-O	LI	LI LI	

Totem-Pale Outputs

Annual Disease Commission of the

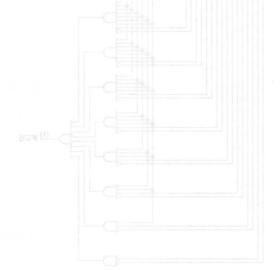
### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	SN74 HC	UNIT
Icc	MAX	65	0.08	mA
Іон	MAX	-0.4	-4	mA
loL	MAX	24	4	mA

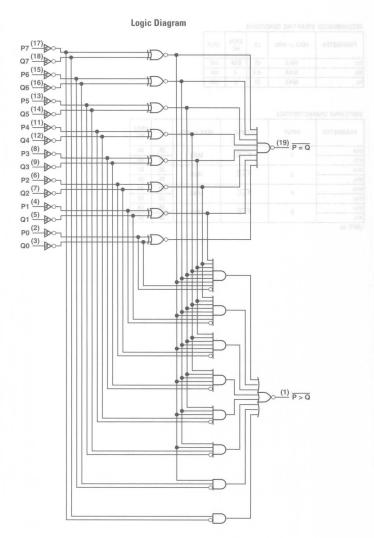
### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	SN74 HC
tPLH	P	$\overline{P} = 0$	MAX	25	69
tphL .	Р	P = U	MAX	25	69
tPLH .	0	P = Q	MAN	25	69
tphL .	и	P=u	MAX	25	69
tplH	Р		MAN	30	69
tphl.	Р	P > Q	MAX	30	69
tPLH .	0	P > Q	MAY	30	69
tPHL .	IL Q		MAX	30	69

UNIT: ns



- Totem-Pole Outputs
- Hysteresis at P and Q Inputs



**FUNCTION TABLE** 

INPUTS			OUTPUTS	
DATA	ENABLE		P=Q	P>Q
P, Q	G1	G2	P=Q	P>G
P=Q	L	L	L	Н
P>Q	L	L	H	L
P <q< td=""><td>L</td><td>L</td><td>Н</td><td>Н</td></q<>	L	L	Н	Н
X	Н	Н	H	Н

DIT INSULTIV COMPARATOR

- Torem-Pole Outputs
- Hysteresis at P and C inputs

## marpaid sign.

RECOMMENDED OF	RATING CONDITIONS
----------------	-------------------

PARAMETER	MAX or MIN	LS	UNIT
Icc	MAX	75	mA
Іон	MAX	-0.4	mA
lou	MAX	24	mA

CIANTOUNA	CILA	DACTE	DICTICC

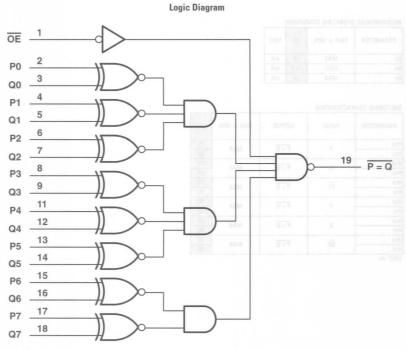
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
tPLH .	P	P = Q	MAX	25
tPHL .	r	P=U		30
tPLH	0	$\overline{P} = \overline{Q}$	MAX	25
tphl .	u u			30
tPLH .	G1	$\overline{P} = \Omega$	MAX	20
tPHL .				30
TPLH	Р	P > 0	MAX	30
tphL .	P	P>U		30
tPLH	Q	P > Q	MAX	30
tPHL .				30
tPLH .	G2	P > Q	MAX	30
tPHL .	62	P>U		25



# 8-BIT IDENTITY COMPARATOR

- Totem-Pole Outputs
- Hysteresis at P and Q Inputs

# **Logic Diagram**



11	IPUTS	OUTPUT
DATA	ENABLE	P=Q
P, Q	Ğ	P=Q
P=Q	L	L
P>Q	L	Н
P <q< td=""><td>L</td><td>Н</td></q<>	L	Н
X	Н	н

# YNCHRONOUS UP/DOWN COUNTER WITH OUTPUT REGISTER, MULT

Multiplexed Districts for Counter or Latched Bata

3-State Outputs Drive Bus Lines Oirectly

British Countries Dispose Chaire

#### RECOMMENDED OPERATING CONDITIONS

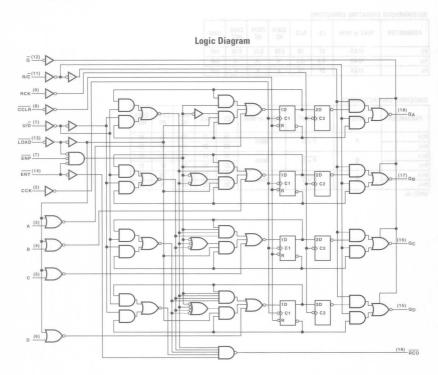
	MAN MIN		ALS	SN74	CD74	CD74	UNIT
PARAMETER	MAX or MIN	LS	ALS	HC	HC	НСТ	UNIT
lcc	MAX	65	19	0.08	0.16	0.16	mA
Іон	MAX	-0.4	-2.6	-4	-4	-4	mA
lou	MAX	24	24	4	4	4	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	SN74 HC	CD74 HC	CD74 HCT
tp.h			MAY	18	12	53	51	51
tphL .	P	P = Q	MAX	23	20	53	51	51
tPLH .	α - <u>G</u>	$\overline{P} = \overline{Q}$ $\overline{P} = \overline{Q}$	MAX	18	12	53	51	51
tPHL				23	20	53	51	51
tPLH				18	12	30	36	36
tPHL .				20	22	30	36	36

# SYNCHRONOUS UP/DOWN COUNTER WITH OUTPUT REGISTER, MULTIPLEXED THREE-STATE OUTPUT

- Multiplexed Outputs for Counter or Latched Data
- 3-State Outputs Drive Bus Lines Directly
- Binary Counter, Direct Clear



#### RECOMMENDED OPERATING CONDITIONS

TILOUISTIVILIA	DED OF ENATING GO	1401110140		
P	ARAMETER	MAX or MIN	LS	UNIT
Icc		MAX	70	mA
Іон	Q	MAX	-2.6	mA
IUH	RCO	IVIAA	-0.4	mA
Inc	Q	MAN	24	mA
TOL	BCO	MAX	8	mA

SYNCHRONGUS UP/DOWN COUNTER WITH OUTPUT

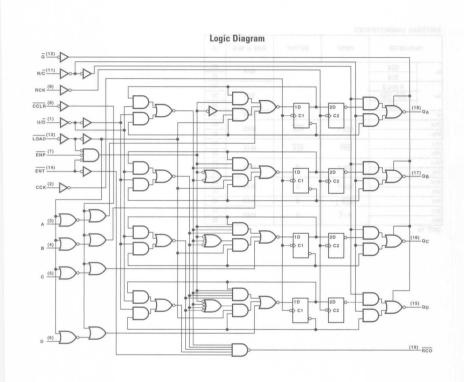
#### SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS
tw	ССК			MIN	25
UV	RCK			IVIIIV	25
	A thru D				30
tsu	ENT, ENP			MIN	30
	U/D				35
th				MIN	0
tPLH .		001/ 4	RCO	MAX	40
tPHL		CCK ↑	NCU	IVIAA	40
tPLH		ENT	RCO	MAX	20
tPHL		EIVI	nco	IVIAA	20
tPLH		COV +	_0_	MAX	20
tPHL	001/1	CCK ↑		IVIAA	25
PLH		DON A		MAX	20
tPHL		RCK ↑	0	IVIAX	25
tPHL		CCLR ↓	0	MAX	40
tplH		R/C	0	MAX	25
tPHL .		n/C	u u	IVIAA	25

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# SYNCHRONOUS UP/DOWN COUNTER WITH OUTPUT REGISTER, MULTIPLEXED THREE-STATE OUTPUT

- Multiplexed Outputs for Counter or Latched Data
- 3-State Outputs Drive Bus Lines Directly
- Binary Counter, Synchronous Clear

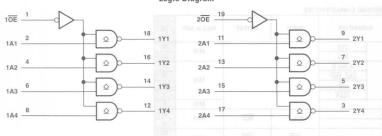


#### RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	UNIT
Icc		MAX	70	mA
	Q	MAX	-2.6	mA
Іон	RCO	MAX	-0.4	mA
le:	0	MAX	24	mA
lor	RCO	MAX	8	mA

	PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
tw	ССК			MIN	25
LW	RCK	1		IVIIIV	25
	A thru D	-q o		SAS	30
tsu	ENT, ENP			MIN	30
tsu	U/D	d a Ti		13	35
	CCLR			CAR	30
th				MIN	0
tPLH.	277	CCK ↑	RCO	MAX	40
tPHL .		CCK	nco	IVIAA	40
tPLH .		ENT	RCO	MAX	20
tphl.		CIVI	nco	IVIAA	20
tPLH .		CCK ↑	Q	MAX	20
tPHL		CCK	u	IVIAA	25
tPLH		BCK &	0	MAX	20
tPHL.		RCK ↑	u	IVIAA	25
tPLH.		R/C	Q	MAX	25
tPHL .		n/C	u	IVIAA	25

# Logic Diagram



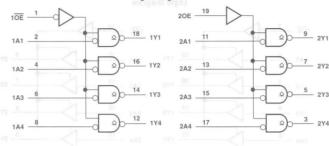
## RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	SN74 BCT	UNIT
lcc	MAX	80	86	mA
Von -	MAX	5.5	5.5	V
lot.	MAX	64	64	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AS	SN74 BCT
PLH		V	MAX	19	11.3
tPHL .	A	, r	IVIAX	6	4.2
PLH	OE Y MAX		MAN	19.5	16.5
PHL	UE	Y	MAX	7.5	10.3

# Logic Diagram



#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	SN74 BCT	SN64 BCT	UNIT
Icc	MAX	95	77	77	mA
Voн	MAX	5.5	5.5	5.5	V
lou	MAX	64	64	64	mA

### SWITCHING CHARACTERISTICS

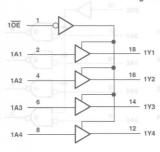
SWITCHING CHAR	ACTENIOTICS					
PARAMETER	INPUT	OUTPUT	MAX or MIN	AS	SN74 BCT	SN64 BCT
tPLH .	А	Y	MAX	18.5	10.1	10.1
tPHL .			IVIAA	6	6.6	6.6
tPLH	10E	1Y	1747	20	19.7	19.7
tPHL .	IUE		MAX	7	6.9	6.9
tPLH .	20E	201	MAN	21	18	18
tPHL .	ZUE	2Y	MAX	7.5	8.5	8.5

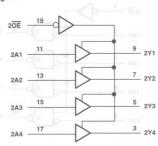
HMIT-ne

# OCTAL BUFFER/LINE DRIVER/LINE RECEIVER WITH OPEN-COLLECTOR OUTPUTS [373] US [AT30]

- pnp Inputs Reduce dc Loading
- Open-Collector Versions of SN74ALS244 and SN74AS244

# Logic Diagram





#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	SN74 BCT	UNIT
lcc	MAX	19	94	76	mA
Voн	MAX	5.5	5.5	5.5	V
lou	MAX	24	64	64	mA

#### SWITCHING CHARACTERISTICS

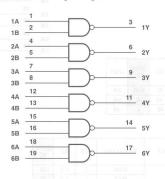
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	SN74 BCT
tplH	Λ	Υ	MAX	15	18.5	10
tphl.	А		IVIAA	12	6	7.2
tPLH	ŌĒ	v	MAX	16	18.5	17.5
tphl.	UE	1	IVIAA	13	7	9.9

# **HEX 2-INPUT NAND DRIVERS**

 $\bullet$  Y =  $\overline{A \bullet B}$ 

High Capacitive-Drive Capability

# Logic Diagram



#### **FUNCTION TABLE**

INP	UTS	OUTPUT
Α	В	Υ
Н	Н	L
L	X	Н
X	L	Н

#### RECOMMENDED OPERATING CONDITIONS

NECOMMENDED	UPENATING CON	DITIUNS			13.1
PARAMETER	MAX or MIN	ALS	AS	SN74 HC	UNIT
Icc	MAX	12	27	0.08	mA
Іон 🛚 🕊	MAX	-15	-48	-6	mA
lor	MAX	24	48	6	mA

#### SWITCHING CHARACTERISTICS

SWITCHING CHAP	ACTERISTICS		Ad			
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	SN74 HC
tPLH .	A D	V	MAX	7	4	25
tPHL	A, B	1	MAX	8	4	25

# 805

# **HEX 2-INPUT NOR DRIVERS**

- $\bullet$  Y =  $\overline{A + B}$
- High Capacitive-Drive Capability

#### **FUNCTION TABLE**

INP	UTS	OUTPUT
Α	В	Υ
Н	X	L
X	Н	L
L	L	H

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	SN74 HC	UNIT
Icc	MAX	14	32	0.08	mA
Іон	MAX	-15	-48	-6	mA
lou	MAX	24	48	6	mA

#### SWITCHING CHARACTERISTICS

OTTITOTHE OTHER	PIOTEINIOTIO			_		-
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	SN74 HC
tplH .	A, B	v	MAX	7	4.3	24
tPHL .	A, D	Y	MAX	8	4.3	24

#### UNIT:ns

# 808

# **HEX 2-INPUT AND DRIVERS**

- Y = A + B
- High Capacitive-Drive Capability

#### **FUNCTION TABLE**

	INP	UTS	OUTPUT
l	Α	В	Υ
	Н	Н	Н
ı	L	X	L
1	X	L	L

#### RECOMMENDED OPERATING CONDITIONS

RECOMMENDED	OPERATING CON	IDITIONS		
PARAMETER	MAX or MIN	SN74 HC	AS	UNIT
Icc	MAX	0.08	33	mA
Іон	MAX	-6	-48	mA
lou	MAX	6	48	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	AS
tPLH	A D	v	MAX	25	6
tphl.	A, B	,	MAX	25	6

UNIT:ns

1A	1		0	
1B	2	>-	3	1Y
2A	4		6	
2B	5	>-	1050	2Y
	7			
3A 3B	8	>	9	3Y
	12		11	
4A 4B	13	>	-11	4Y
5A	15			
5B	16 A1	\ \ 	14	5Y
JD	18			



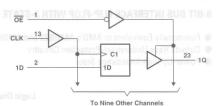
# Logic Diagram

		•				
1A	1			3		
1B	2	o con	)	3	1Y	
	4					
2A 2B	5	6.17	)	ь	2Y	
3A	7		XAI	9		
3B	8	-	)—	-	3Y	
4A	12	95	XAI	11		
4B	13		)—	- 11	4Y	
5A	15	_=	1831128	14		
JA	16			14	5Y	



# 10-BIT BUS INTERFACE FLIP-FLOPS TUSTUO 3 OE 4 MITH 4004 WITH 3-STATE OUTPUT

- Outputs Have Undershoot-Protection Circuitry
- Power-Up High-Impedance State



#### FUNCTION TABLE

INPUTS			OUTPUT
OE	CLK	D	Q
L	î	Н	H
L	1	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

#### RECOMMENDED OPERATING CONDITIONS

TIEGOTI TIETO ED	OT EMPTITIES SOIT	I	1		
PARAMETER	MAX or MIN	AS	ABT	LVC	UNIT
Icc	MAX	113	38	0.01	mA
Іон	MAX	-24	-32	-24	mA
lou	MAX	48	64	24	mA

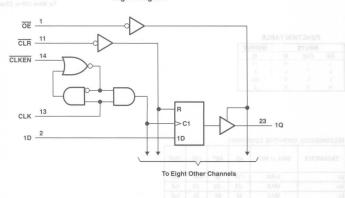
#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AS	ABT	LVC
				,,,,	1101	3V
	Н	igh	MIN	8	2.9	3.3
tw	L	OVV	MIN	8	3.8	3.3
tsu			MIN	6	2.1	1.9
th				.0	1.3	1.5
tPLH .	CLK	Q	MAX	7.5	6.2	7.3
tPHL .	CLK	u	IVIAX	13	6.7	7.3
tPZH	ŌE			11	5.8	7.6
tPZL	UE	Q	MAX	12	6.3	7.6
tPHZ	ŌE	0	MAX	8	6.7	6.2
tPLZ	UE	u	IVIAX	8	6.5	6.2

# 9-BIT BUS INTERFACE FLIP-FLOP WITH 3-STATE OUTPUT 250 JR-4LF 33 A3 R3 TM 208 TI8-01

- Functionally Equivalent to AMD's AM29823 and AM29824
- Outputs Have Undershoot-Protection Circuitry
- Power-Up High-Impedance State

# Logic Diagram



	INPU	INPUTS	PUTS		OUTPUT
OE	CLR	CLKEN	CLK	D	Q
L	L	X	X	X	L
L	Н	L	1	H	Н
L	Н	L	1	L	L
L	H	H	X	X	Qo
H	×	Y	V	Y	7

#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	ABT	TAC.	UNIT
Icc	MAX	103	38	0.01	mA
Іон	MAX	-24	-32	-24	mA
lou	MAX	48	64	24	mA

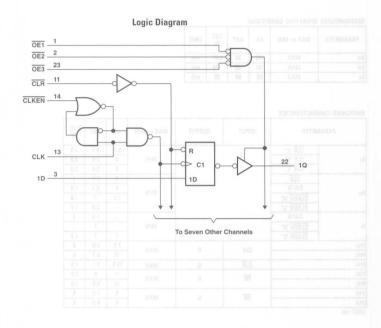
#### SWITCHING CHARACTERISTICS

P	ARAMETER	INPUT	OUTPUT	MAX or MIN	AS	ABT	LVC 3V
	CLR "L"		g 5-		6.5	5.5	3.3
tw	CLK "H"			MIN	8	2.9	3.3
	CLK "L"				8	3.8	3.3
	CLR				8	2.5	-1
	DATA				6	2.1	1.3
<b>İ</b> su	CLKEN "H"			MIN	7.5	2	1.8
	CLKEN "L"			+ +	-	3.3	1.8
	DATA				-	1.3	2
th	CLKEN "H"	V		MIN	-	1	-
	CLKEN "L"				0	2	1.3
tPLH		CLK	0	MAN	7.5	6.8	8
tphl		CLK	۵	MAX	13	6.7	8
tPHL		CLR	Q	MAX	15.5	7.1	7.9
tpzh				MAX	11	6	7.2
tPZL		UE	OE Q		12	6.5	7.2
tPHZ		ŌĒ	0	MAX	8	7.5	6
tPLZ .		UE	OE Q		8	6.9	6

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# 8-BIT BUS INTERFACE FLIP-FLOP WITH 3-STATE OUTPUT

- Improved I<sub>OH</sub> Specifications (Max: -24mA)
- Outputs Have Undershoot-Protection Circuitry
- Power-Up High-Impedance State



		INPUTS			OUTPUT
OE	CLR	CLKEN	CLK	D	Q
L	L	X	X	X	L .
L	H	L	1	H	Н
L	Н	L	1	L	L
L	H	H	X	X	Q <sub>0</sub>
H	X	X	X	X	Z

#### ART RUFFERS/RUS DRIVERS

- 3-State Dutputs Drive Bus Lines or Buffer Memory
   Arthrees Familians.
- 74AC11xxx Product Available in Reduced-Noise
- 74ACT11xxx: Product Available in Reduced-Noise

#### RECOMMENDED OPERATING CONDITIONS

TIEGOTHINIETEDED	OT EMPTING CON		
PARAMETER	MAX or MIN	AS	UNIT
Icc	MAX	95	mA
Іон	MAX	-24	mA
lor	MAX	48	mA
		-	

#### FUNCTION TABLE

#### SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	AS
1.8 1.52	CLR "L"				4
tw	CLK "H"	ISAM.		MIN	- 8
10.5	CLK "L"				- 8
7.3	CLR	XARR		30	- 8
İsu	DATA			MIN	6
	CLKEN	XAM		70	6
th				MIN	0
tplh		CLK	Q	MAX	7.5
tphL		- CLK		IVIAA	13
TPHL .		CLR	Q	MAX	15.5
tpzh			0	MAX	11
tPZL		J. UE	u	IVIAX	12
tPHZ		ŌĒ	0	MAX	8
tPLZ		UE	OE Q		8

8

# 10-BIT BUFFERS/BUS DRIVERS

Address Registers

VAACT type: Product Available in Reduced-Noisi

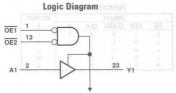
74ACT11xxxx Product Available in Reduced-Noise

#### ECOMMENDED OFFICE CONDITIONS

#### PUNCTION TABLE

## **10-BIT BUFFERS/BUS DRIVERS**

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



To Nine Other Channels

FUNCTION TABLE

INPUTS OUT		OUTPUT
OE2	Α	Y
L	Н	Н
L	L	L
H	X	Z
X	X	Z
	DE2 L L H	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	AC 11	ACT 11	LVC 3V	UNIT
Icc	MAX	40	80.0	0.08	0.01	mA
Іон	MAX	-32	-24	-24	-24	mA
lou	MAX	64	24	24	24	mA

#### SWITCHING CHARACTERISTICS

SWITCHING CHA	RACTERISTICS						
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	AC 11	ACT 11	3V LVC
tplh	Toronto A	Y	MAX MAX	4.8	8.7	9.2	6.7
tPHL	MIM A			4.7	9.7	11.2	6.7
tpzh	ŌĒ			5.9	9.7	11.3	7.3
tPZL	UE			6.9	13	14	7.3
tPHZ	- OE			6.8	9.1	12	6.7
tPLZ				6.9	8.8	11.6	6.7

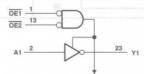
#### UNIT: ns

# 828

# **10-BIT BUFFERS/BUS DRIVERS**

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

# **Logic Diagram**



To Nine Other Channels

#### **FUNCTION TABLE**

Γ		INPUTS		OUTPUT
Γ	OE1	OE2	Α	Y
Ī	L	L	Н	L
	L	L	L	Н
	H	X	X	Z
	X	H	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AC 11	ACT 11	LVC 3V	UNIT
lcc	MAX	0.08	0.08	0.01	mA
Іон	MAX	-24	-24	-24	mA
lou	MAX	24	24	24	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AC 11	ACT 11	3V
tPLH			MAN	9.5	10.2	6.7
tphl.	А		MAX	10.4	11.7	6.7
tPZH	ŌĒ		MAX	10.7	12.1	7.3
tPZL	UE	T T		13.2	14.7	7.3
tPHZ	ŌĒ	1	MAN	9.6	12.3	6.7
tPLZ	UE		MAX	9.2	11.7	6.7

# 832

# Logic Diagram

# **HEX 2-INPUT OR DRIVERS**

	γ	=	Α	+	В	
-			, ,		_	

High Capacitive-Drive Capability

## **FUNCTION TABLE**

	INP	UTS	OUTPUT
Ì	Α	В	Υ
ſ	Н	X	Hose
1	X	H	H
1	L	L	L

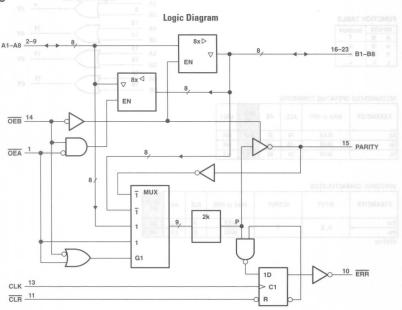
1A	eleagy:		149 TI8 3		
1B	2	$\supset$	3	1Y	
2A	4		6		
2B	5	_) >	0	2Y	
3A	7	1	9		
3B	8	$\supset$	3	3Y	
4A	12		11		
4B	13	_) >	. 0-	4Y	
5A	15	1	14		
5B	16	_) >		5Y	
6A	18		17		
6P	19	_) >		6Y	

#### RECOMMENDED OPERATING CONDITIONS

MAX or MIN	ALS	AS	SN74 HC	UNIT
MAX	16	36	0.08	mA
MAX	-15	-48	-6	mA
MAX	24	48	6	mA
	MAX MAX	MAX 16 MAX -15	MAX 16 36 MAX -15 -48	MAX or MIN ALS AS HC  MAX 16 36 0.08  MAX -15 -48 -6

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	SN74 HC
tPLH	A D	V	MAX	9	6.3	25
tPHL .	A, B	Y	MAX	8	6.3	25



			NPUT:	S		0	UTPU	TS AND I	/0		
В	OEA	CLR	CLK	Ai Σ OF H's	Bi Σ OF H's	А	В	PARITY	ERR	FUNCTION	INTERFACE D-TY
	Н	X	Х	Odd Even	NA	NA	Α	L	NA	A data to B bus and generate parity	uffer-Type Catouts Dr
	L	Н	1	NA	Odd Even	В	NA	NA	H	B data to A bus and check parity	uner-type uarpus ur stured Pinout
	X	L	X	X	X	X	NA	NA	H	Check error flag register	
	Н	H L H	No↑ No↑ ↑	X X Odd Even	×	Z	Z	Z	NC H H L	Isolation	odra Bus-Driving Latel high-Impedance Sta
	L	X	Х	Odd Even	NA	NA	Α	H	NA	A data to B bus and generate inverted parity	

Logic Disorem

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT	FUNCTION
CLR	CLK	POINT P	ERR <sub>n-1</sub> †	ERR	
Н	1	Н	Н	Н	
H	1	X	L	H	Sample
H	1	L	X	L	
L	X	X	X	Н	Clear

† The state of ERR before any changes at CLR, CLK, or point P



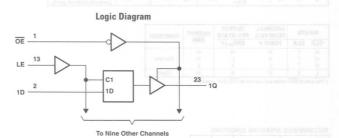
#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
Icc	MAX	38	mA
Іон	MAX	-32	mA
lou	MAX	64	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
tplH	A or B	B or A	MAX	5.3
tPHL .	A or B	B OF A	WAX	5.3
tPLH		DARITY	144V	11.2
tPHL .	A	PARITY	MAX	11
tPZH	ŌE	PARITY	MAX	10.5
tPZL	OE	PARITY	IVIAA	10
tPLH	CLR	ERR	MAX	5.2
tpht.	CLK	ERR	MAX	6.2
tPZH	ŌĒ	A.B. or PARITY	1447	6.5
tPZL	UE	A,B, OF PARITY	MAX	6.5
tPHZ	ŌĒ	A.D DADITY	MAN	7.9
tPLZ	UE	A,B, or PARITY	MAX	8.1

- The Environment of the Environme
- 3-State Buffer-Type Outputs Drive Bus Lines Directly
   Bus-Structured Pinout
- Provide Extra Bus-Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up High-Impedance State



Γ		INPUTS	OUTPUT	
Г	OE	LE	D	Q
Г	L	Н	Н	L
l	L	H	L	H
l	L	L	X	Q <sub>0</sub>
ı	Н	X	X	Z

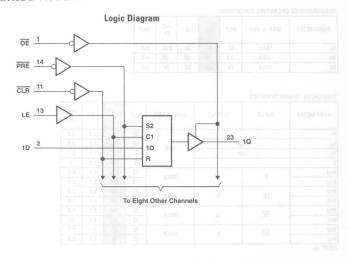
#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	ABT	LVC 3V	UNIT
Icc	MAX	62	94	38	0.01	mA
Іон	MAX	-2.6	-24	-32	-24	mA
lor.	MAX	24	48	64	24	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	ABT	SV.
tw		200	4 1	20	4	3.3	3.3
tsu	Hi	gh	MIN	10	2.5	2.5	2.1
tsu	Lo	W	MIN	10	2.5	1.5	2.1
th				5	2.5	1.5	1
tPLH	D	Q	MAX	13	6.5	6.2	6.7
tphL .	U	u	IVIAX	13	10.5	6.2	6.7
tplh	LE	0	MAY	21	12	6.5	7.6
tphl.	LE	Q	MAX	26	12	6.7	7.6
tPZH	ŌE	Q	MAX	12	14	5.3	7.2
tPZL	UE	u	IVIAX	12	16	6.3	7.2
tPHZ	ŌĒ	0	MAX	10	8	7.1	5.9
tPLZ	OE Q	u u	IVIAX	12	8	6.5	5.9

# 9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTDUTS



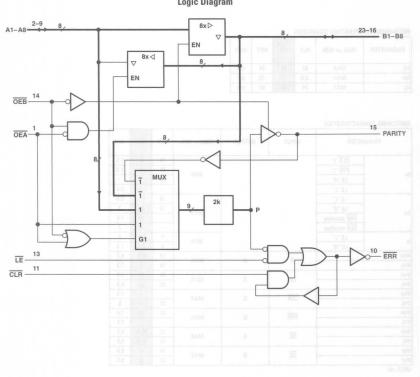
		ОИТРИТ			
PRE	CLR	OE	LE	D	OUIFUI
L	Н	L	X	X	Н
H	L	L	X	X	L
L	L	L	×	X	H
H	H	L	H	L	L
Н	H	L	H	H	H
H	H	L	L	X	Q <sub>0</sub>
	2.41				_

RECOMMENDED OPERATING CONDITIONS

NEGOIVINIENDED	OI LIMING CON	T		_	-
PARAMETER	MAX or MIN	ALS	AS	ABT	UNIT
Icc	MAX	67	92	34	mA
Іон	MAX	-2.6	-24	-32	mA
IOL	MAX	24	48	64	mA

					-		
P	PARAMETER		T OUTPUT MAX or MIN		ALS	AS	ABT
	CLR "L"			-	35	4	5.5
tw	PRE "L"			MIN	35	4	4.5
W	LE "H"			MIIN	20	4	
	LE "L"				-	4	3.4
	LE "L"			385	10	2.5	2.5
	LE "H"			MIN	10	2.5	3
tsu	PRE inactive			IVIIIV	-	15	1.6
	CLR inactive				-	14	2
h	LE "L"			MIN	5	2.5	1
ın	LE "H"			IVIIIV	5	2.5	1.5
IPLH -	000	D 0		MAX	13	6.5	6.7
tPHL .	4	U	u	IVIAA	18	9	7.2
IPLH .		LE	Q	MAX	21	12	7.2
tPHL .		LE	u	IVIAX	26	12	6.9
tPLH .		CLR	0	MAX	1-7	-	7.1
tPHL		CLK	U MAX		23	13	8
tPLH		PRE	Q	MAX	22	10	7.4
PHL		PHE	u u	MAX		-	7.2
PZH PZL		Q		MAX	12	10.5	5.7
				MAX	14	13.5	6.5
tPHZ	PHZ		Q	MAX	10	8	6.8
PLZ		OE Q		MAX	12	8	5.9

# Logic Diagram



		- 1	NPUT	S		0	UTPU	T AND I/O	Os	
OEB	ŌĒĀ	CLR	LE	Ai Σ OF H	Bi† Σ OF H	Α	В	PARITY	ERR‡	FUNCTION
L	Н	Χ	X	Odd Even	NA	NA	Α	L H	NA	A data to B bus and generate parity
Н	L	Н	L	NA	Odd Even	В	NA	NA	H	B data to A bus and check parity
Н	L	Н	Н	X	X	X	NA	NA	NC	Store error flag
X	X	L	Н	X	X	X	NA	NA	Н	Clear error flag register
Н	Н	H H H	H	X X L Odd H Even	х	Z	Z	Z	NC H H L	Isolation§ (parity check)
L	L	Х	X	Odd	NA	NA	Α	H	NA	A data to B bus and generate inverted parity

INPL	JTS	TO DEVICE	OUTPUT PRE-STATE	OUTPUT	FUNCTION
CLR	LE	POINT P	ERR <sub>n-1</sub> †	ERR	
L	L	L H	Х	L H	Pass
Н	L	X H	X L H	L L H	Sample
L	Н	×	X	Н	Clear
Н	Н	×	L H	L H	Store

#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
Icc	MAX	38	mA
Іон	MAX	-32	mA
lou	MAX	64	mA

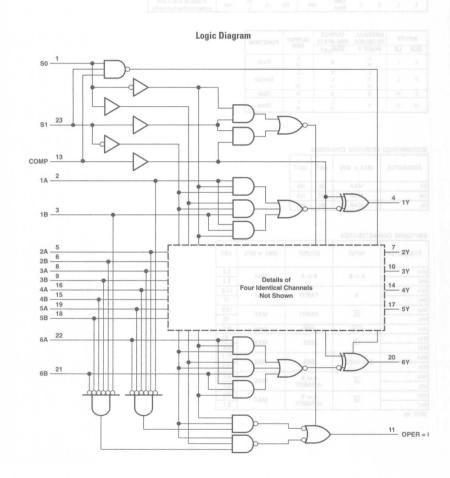
#### SWITCHING CHARACTERISTICS

SWITCHING CHA	The state of the s			-	
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	
tplH VIII	A D	D A	MAN	5.3	
tphl .	A or B	B or A	MAX	5.3	
tPLH TPLH		PARITY	MAN	11.2	
tphl	A	PARITY	MAX	11	
tPLH TO	ŌE	DADITY	MAY	10.5	
tphL .	UE	PARITY	MAX	10	
tPLH .	CLR	ERR	MAX	6.2	
tPLH .	LE	ERR	MAX	6	
tphl.	LE	Enn	WAX	6.6	
tPLH 08	B or RARITY	ERR	MAX	11.7	
tPHL .	B OF HARITY	Enn	IVIAX	12.8	
tPZH	ŌĒ	A or B	MAX	6.7	
tPZL	UE	or PARITY	IVIAX	6.7	
tPHZ	ŌĒ	A or B	MAX	7.9	
tPLZ	UE	or PARITY	WAX	8.1	

OIVII. IIS

# **HEX 2-TO-1 UNIVERSAL MULTIPLEXERS**

- Select True or Complementary Data
- Perform AND/NAND (Masking) of A or B Operand
- Cascadable to Expand Number of Operands
- Detect Zeros on A or B Operands
- 3-State Outputs Interface Directly with System Bus



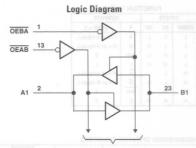
L	l H	н	L	Inc. Inc.
Н	L	L	Ā	H = all A inputs L
Н	L	н	B	H = all B inputs L
H	H	L	A•B	Z
Н	Н	Н	Z	Z

#### RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALS	AS	UNIT
		INIMA OF IVITIN	ALS	MO	UNIT
		MAX	36	135	mA
ICCL		MAX	33	175	mA
Юн	Y	MAX	-2.6	-15	mA
	OPER = 0	MAX	-2.6	-2	mA
	Y	MAX	24	48	mA
IOL	OPER = 0	MAX	24	20	mA

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
t <sub>pd</sub>	A or B (COMP = "H")	Y inverting	MAX	14	12
<b>t</b> pd	A or B (COMP = "L")	Y non-inverting	MAX	14	10
tpd	S0 or S1	Y		33	13
tpd	COMP	Y	MAY	18	13
tpd	A or B	OPER = 0	MAX	37	14
tpd	S0 to S1	OPER = 0	1.0	23	18
ten	00 +- 01	Y	MANY	35	12
tdis	S0 to S1	Y	MAX	23	11
ten	COMP	Y	MAN	24	12
tdis	COMP	Y	MAX	21	9
ten	SO	0050 0	MAN	20	12
tdis	50	OPER = 0	MAX	27	9
ten	S1	0050 0	MANY	25	12
tdis	51	OPER = 0	MAX	19	9
ten	COMP	OPER = 0	MAX	25	13
tdis	COMP	UPER = U	IVIAX	20	9

# 10-BIT TRANSCEIVERS WITH 3-STATE OUTPUTS



#### **FUNCTION TABLE**

INP	UTS	OPERATION	
OEAB OEBA		OPERATION	
L	Н	A data to B bus	
Н	L	B data to A bus	
H	H	Isolation	
L	L	Latch A and B (A = B)	

	To Nine Other Channels	3

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVC 3V	UNIT
lcc	MAX	38	0.01	mA
Іон	MAX	-32	-24	mA
lor	MAX	64	24	mA

# SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVC 3V	XAM
tPLH		D 4	MAX	5.2	6.4	
tPHL .	A or B	B or A	IVIAX	4.9	6.4	
tpzh	OEAB or OEBA	B or A	MAX	5.9	7	XAW
tPZL				6.9	7	
tphz		B or A	MAN	7.5	5.9	MAM
tPLZ	OEAB or OEBA		MAX	7.1	5.9	XAM

# 9-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

3-State Outputs

## **FUNCTION TABLE**

OPERATION	INPUTS				
OPERATION	OEBA2	OEBA1	OEAB2	OEAB1	
Latch A and I	L	L	L	L	
A to B	X	Н	L	L	
A IO B	H	X	L	L	
B to A	Lao.	L	X	Н	
B to A	Library	L	H	X	
	X	Н	X	Н	
Isolation	H	X	X	H	
ISOIATION	H	X	H	X	
	V	LI	L	v	

# OEBA1 11 OEBA2 13 OEAB1 14 OEAB2 14 OEAB2 14 OEAB2 14 OEAB2 14 OEAB2 15 OEAB2 16 OEAB2 17 OEAB2 17 OEAB2 18 OEA

Logic Diagram

To Eight Other Channels

#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVC 3V	UNIT
Icc	MAX	38	0.01	mA
Іон	MAX	-32	-24	mA
lou	MAX	64	24	mA

#### SWITCHING CHARACTERISTICS

SWITCHING CHAN	ACTENISTICS	- 10 m	1500-011		
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVC 3V
tPLH	A or B	D A	MAX	5.7	6.1
tphl.	A OF B	B or A	MAX	3.9	6.1
tPZH	ŌĒ	A D	MAX	5.5	7.2
tPZL	UE	A or B	MAX	5.4	7.2
tPHZ	ŌĒ	A D	MANY	6.7	6.3
tPLZ	UE	A or B	MAX	6.9	6.3

**Logic Diagram** CLK 14 S0 1 S1 2 SN74ALS867A Only (asynchronous clear) ENP 23 A 3 B 4 C \_5 D 19 QD D 6 E 7 18 QE G 9 ⊅ 16 QG H 10 D-13 RCO ENT 11

S1	S0	FUNCTION	
L	L	Clear	
L	Н	Count down	
Н	L	Load	
Н	Н	Countum	

#### RECOMMENDED OPERATING CONDITIONS

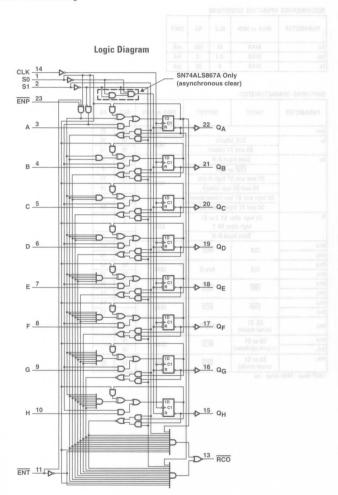
PARAMETER	MAX or MIN	ALS	AS	UNIT
Icc	MAX	45	195	mA
Іон	MAX	-0.4	-2	mA
lou	MAX	8	20	mA

DADAMETER	INPUT OUTPUT		MAX or MIN	410	AS
PARAMETER	INPUT	001101	MAX or MIN	ALS	AS
fmax		10 -0	MIN	35	50
tw	CLK (c	lock)	MIN	14	10
	S0 and S	IVIIIV	10	10	
tsu	Data inp	ut A-H		10	4
	ENP o	r ENT		15	8
	S0 low and S	1 high (load)	MIN	12	10
	S0 and S1 I	IVIIIV	-	10	
	S0 high and S1 low (count down)			12	40
	S0 and S1 hig		12	40	
th	S0 high after S1 ↑ or S1 high after S0 ↑		MIN	3	
	Data inp	out A-H		0	0
tPLH	CLK	RCO	MAX	14	22
tphl .	CLK	nco	IVIAA	14	16
tPLH	CLK	Any Q	MAX	16	11
tphl.	CLK	Ally u	IVIAA	16	15
tplh	ENT	RCO	MAX	14	10
tphl .	LIVI	HOU	IVIAA	9	17
tplh	ENP	RCO	MAX	-	14
tрнL	LINE	nou	IVIAA	. 500	17
tPHL .	S0, S1 (clear mode)	Any Q	MAX	26	
tPLH	S0 or S1	RCO	MAX	16	-
tphl.	(count up/down)	nco	IVIAA	16	) -
tPHL .	S0 or S1 (clear mode)	RCO	MAX	16	21

UNIT fmax : MHz other : ns

# 8-BIT SYNCHRONOUS BIDIRECTIONAL COUNTER

- Fully Programmable with Synchronous Counting and Loading
- Synchronous Clear
- Ripple-Carry Output for n-Bit Cascading



S1	S0	FUNCTION	
L	L	Clear	
L	Н	Count down	
Н	L	Load	
Н	Н	Count up	

#### RECOMMENDED OPERATING CONDITIONS

OT ENTAINING GOTE	I		
MAX or MIN	ALS	AS	UNIT
MAX	45	195	mA
MAX	-0.4	-2	mA
MAX	8	20	mA
	MAX or MIN  MAX  MAX	MAX or MIN ALS  MAX 45  MAX -0.4	MAX 45 195 MAX -0.4 -2

SWITCHING CHA	ARACTERISTICS			-	+
PARAMETER	INPUT	NPUT OUTPUT MAX		ALS	AS
fmax			MIN	35	45
tw	CLK		MIN	14	11
tsu	Data inpu	t A-H		10	5
	ENP or		15	9	
	S0 low and S1	MIN	13	11	
	S0 and S1 lo	IVIIIV	13	11	
	S0 high and S1 lov		13	50	
	S0 and S1 high		13	50	
th	S0 high after S1 ↑ or S1 high after S0 ↑		MIN	3	
	Data inpu		0	0	
tPLH .	CLK	RCO	MAX	14	35
tphl	CLK	ncu	IVIAA	14	18
tplH .	CLK	Any Q	MAX	16	11
tPHL .	CLK	Any u	IVIAA	16	15
tPLH	ENT	RCO	MAX	14	15
tPHL	EIVI	ncu	WIAX	9	17
tplH .	ENP	RCO	MAX	-1-	19
tphl.	CINP	ENP		-	18
tPLH	S1	RCO	MAX	15	- 1
tPHL	(count up/down)	nuu	IVIAA	15	
tplH .	S0	RCO RCO	MAX	16	lan
tPHL .	(clear/load)	1100	IVIMA	12	-

UNIT fmax : MHz other : ns

16 16

Three Identical Channels Not Shown

	FIL	E SELECT	INPUT/OUTPUT			
SO	S1	FILE SEL	S2	S3	I/O SEL	
L	L	1R to A, 1R to B	L	L	A out B A out, B out	
H	L	2R to A, 1R to B				
L	H	1R to A, 2R to B				
H	H	2R to A, 2R to B				
L	L	A to 1R, 1R to B	Н	L	A in B A in, B out	
Н	L	A to 2R, 1R to B				
L	H	A to 1R, 2R to B				
Н	H	A to 2R, 2R to B	-			
L	L	1R to A, B to 1R	L	Н	A out B A out, B in	
H	n.L.	2R to A, B to 1R	170			
L	H	1R to A, B to 2R				
H	H	2R to A, B to 2R	0.1			
L	L	B to 1R	Н	Н	A in Bin A in, B	
H	L	A to 2R, B to 1R				
L	H	A to 1R, B to 2R	- 11		-0	
H	H	B to 2R	25			

#### RECOMMENDED OPERATING CONDITIONS

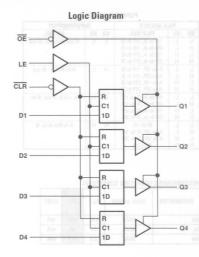
ALS	AS	UNIT
110	190	mA
24	48	mA
-2.6	-15	mA
	24	24 48

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
tw	W	rite	MIN	12	12
tsu	Address be	efore write ↓		5	5
	Data bef	ore write †	MIN	15	15
	Select be	fore write ↓	1	12	12
th	Address be	efore write ↓		0	0
	Data bef	ore write ↑	MIN	0	0
	Select be	fore write ↓		12	12
ta(A)	Any A	Any DQ	MAX	19	15
ta(S)	SO	Any DQA	144V	15	13
	S1	Any DQB	MAX	15	13
tdis	S2	Any DQA		14	11
	S3	Any DQB	MAX	14	11
ten	S2	Any DQA		17	12
	\$3	Any DQB	MAX	17	12
tpd	W	Any DQ	T-	23	19
	DA	DQB	MAX	26	22
	DQB	DQA	1	26	22

### **DUAL 4-BIT D-TYPE LATCHES**

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Asynchronous Clear



### FUNCTION TABLE

	INF			
ŌĒ	CLR	CLR ENABLE		OUTPUT
L	L	X	X	L
L	H	H	Н	H
L	H	H	L	L
L	Н	L	X	Qo
H	X	X	X	Z

### RECOMMENDED OPERATING CONDITIONS

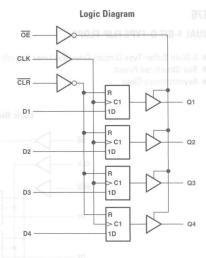
HEGOMINIENDED	OI EINTING GOIL	T	F	-
PARAMETER	MAX or MIN	ALS	AS	UNIT
Icc	MAX	31	129	mA
Іон	MAX	-2.6	-15	mA
lou	MAX	24	48	mA

### SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	ALS	AS
	CLR low				15	5
tw LE high				NAIN!	10	5
tsu th				MIN	10	2
					7	4.5
tPLH .		D	Q	MAN	14	9.5
tPHL.		U	u	MAX	14	7,5
tPLH		15 0			22	13
tPHL		LE	a	MAX	21	7.5
tPHL.		CLR	Q	MAX	20	9
tPZH		ŌĒ		1111	18	6.5
tPZL		UE	Q	MAX	18	10.5
tPHZ		ŌE Q		1111	10	7.5
tPLZ		0E Q		MAX	15	7.5

### **DUAL 4-BIT D-TYPE EDGE-**TRIGGERD FLIP-FLOPS

- 3-State Buffer-Type Outputs Drive Bus Lines
- Bus-Structured Pinout
- Asynchronous Clear



### **FUNCTION TABLE**

OUTDUT	INPUTS					
OUTPUTS	D	CLK D		ŌĒ		
Leo	X	X	L	L		
H	H	1	H	L		
L	L	1	H	L		
Qn	X	L	H	L		
z	X	X	X	H		

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
lcc	MAX	32	160	mA
Іон	MAX	-2.6	-15	mA
lou	MAX	24	48	mA

### SWITCHING CHARACTERISTICS

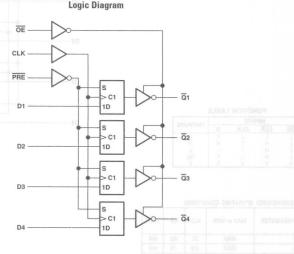
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS				
fmax			MIN	30	125				
tw	PRE or	CLR low		10	2				
	CLI	K "H"	MIN	16.5	3				
	CL	K "L"		16.5	4				
tsu	Data		MIN	15	2				
	PRE or C	LR inactive	IVIIIV	10	4				
th			MIN	0	1				
tPLH	01.14	CLK	CLK	CIV	CI K	Q	MAX	14	8.5
tPHL .	ULK	u	IVIAA	14	10.5				
tphl	CLR	0	MAX	17	9.5				
tPZH	ŌĒ	_	MAN	18	7				
tPZL	UE	0	MAX	18	10.5				
tPHZ	ŌĒ	0	MANY	10	6				
tPLZ	UE	Q.	MAX	12	7.5				

UNIT fmax : MHz other : ns

### **DUAL 4-BIT D-TYPE FLIP-FLOPS**

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Asynchronous Clear

### Logic Diagram



### FUNCTION TABLE (each filip-flop)

	INP	UTS		OUTPUT
OE	PRE	CLK	D	Q
L	L	X	X	L
L	H	1	H	L
L	H	1	L	H
L	H	L	X	Q <sub>0</sub>
н	X	X	X	Z

### T MAGNITUOE COMPARATOR

this stool man P alderints ( 2002 ALERS )

RECOMMENDED OPERATING CONDITIONS

RECOMMENDED	UPENATING CON	DITIUNS		_
PARAMETER	MAX or MIN	ALS	AS	UNIT
lcc	MAX	31	160	mA
Іон	MAX	-2.6	-15	mA
lou	MAX	24	48	mA

mergald algo.

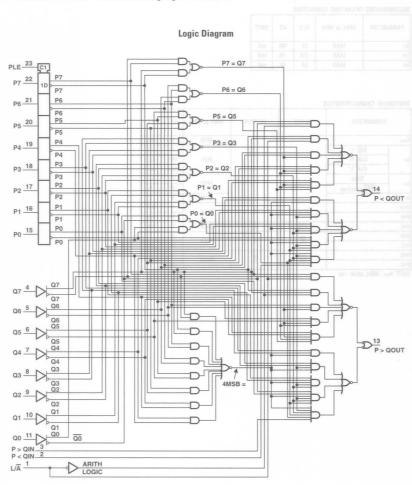
SWITCHING CHARACTERISTICS

	PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
fmax		- Cl		MIN	30	80
	PRE "L"			- Salar	10	4.5
tw	CLK "H"	-		MIN	16.5	6.2
	CLK "L"			P2 = 02	16.5	6.2
	Data			MIN	15	4.5
tsu	PRE inactive			INITIN	10	5
th TUO				MIN	0	2
tPLH		01.16	ā	MAX	14	8.5
tPHL .		CLK	u u	IVIAA	14	10.5
tPHL	-	PRE	ā	MAX	19	9.5
tPZH	- OE		ā	MAY	18	7
tPZL		OE OE	u	MAX	18	11
tPHZ tPLZ		ŌĒ	ā	MAN	10	7
		UE	u	MAX	13	7

UNIT fmax : MHz, other : ns

### 8-BIT MAGNITUDE COMPARATOR

- SN54AS885 Latchable P-Input Ports with Power-Up Clear
- Choice of Logical or Arithmetic (Two's Complement) Comparison
- Data and PLE Inputs Utilize pnp Input Transistors to Reduce dc Loading Effects
- Cascadable to n Bits While Maintaining High Performance



ELINICTION TABLE

FUNCTION TABLE							
		INF	OUTPUTS				
COMPARISON	L/A	DATA P0-P7, Q0-Q7	P > QIN	P < QIN	P > QOUT	P < QOUT	
Logical	Н	P > Q	×	X	Н	L	
Logical	Н	P < Q	×	X	L	H	
Logical†	H	P = Q	HorL	H or L	H or L	HorL	
Arithmetic	L	PAGQ	X	×	Н	L	
Arithmetic	L	QAGP	X	X	L.	H	
Arithmetic <sup>†</sup>	L	P = Q	HorL	HorL	H or L	HorL	

In these cases, P > QOUT follows P > QIN and P < QOUT follows P < QIN. AG = arithmetically greater than

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	UNIT	
Icc	MAX	210	mA	
Іон	MAX	-2	mA	
loL	MAX	20	mA	



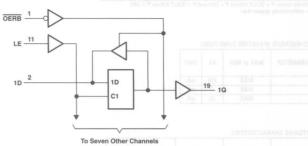
### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AS
tsu	Data befo	ore PLE ↓		2
th	Data aft	er PLE ↓	MIN	4
tPLH .	L/Ā	P < QOUT,	MAN	13
tPHL .	L/A	P > QOUT	MAX	13
tPLH	P < QIN,	P < QOUT,	MAN	8
tphL .	P > QIN	P > QOUT	MAX	8
tPLH	Any P or Q	P < QOUT,	MAN	17.5
tPHL	data input	P > QOUT	MAX	15

### 8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

- 3-State I/O-Type Read-Back Inputs
- True Logic Outputs
- Bus-Structured Pinout

### **Logic Diagram**



Zin MIN in X

### RECOMMENDED OPERATING CONDITIONS

HECOMINIEME	ED OF ENATING CO	JIVDITIONS		T
PA	RAMETER	MAX or MIN	ALS	UNIT
Icc		MAX	70	mA
Іон	Q	MAX	-2.6	mA
IUH	D	IVIAA	-0.4	mA
lou	0	MAX	24	mA
IUL	D	IVIAX	8	mA

### SWITCHING CHARACTERISTICS

SWITCHING CHAN	ACTENISTICS		_	
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
tw	LE	high	MIN	10
tsu	Data be	fore LE ↓	MIN	10
	Data bet	fore OERB	IVIIN	10
th	Data a	fter LE ↓	MIN	5
tPLH	n	Q	MAX	17
tphl.	U	u	WAX	24
tPLH	LE	0	MAX	26
tPHL .	LE	Q.	MAX	26
ten	OERB	D	MAX	21
tdis	UEHB	D	MAX	19

### 9-BIT D-TYPE TRANSPARENT

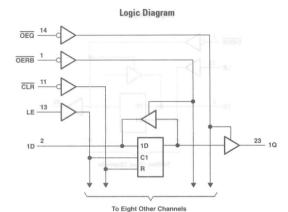
### 10-8(T D-TYPE TRANSPARENT READ-BACK LATCHES

- 3-State I/O-Type Read-Back Inputs
- True Logic Outputs
- Bus-Structured Pinout
- Designed with Nine Bits for Parity Applications

### 3-State I/O-Type Read-Back Inputs

True Logio Outputs

Bus-Structured Pinout



### RECOMMENDED OPERATING CONDITIONS

PA	RAMETER	MAX or MIN	ALS	UNIT
Icc		MAX	80	mA
Іон	0	MAX	-2.6	mA
IUH	D	IVIAA	-0.4	mA
in.	Q.	MAX	24	mA
lor	D	IVIAX	8	mA

### SWITCHING CHARACTERISTICS

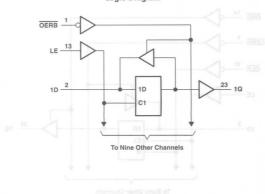
SWITCHING CHARAC	TERISTICS			1
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
tw	С	.н.	MIN	10
	CLF	R "L"	MIN	10
tsu	Data be	efor LE ↓	MIN	10
	Data befo	or OERB ↓	IVIIIV	10
th	Data af	fter LE↓	MIN	5
tPLH .	D	Q	MAX	14
tphl .	U	u u	IVIAA	16
tplh	LE	Q	MAX	20
tphl .	LE	u u	IVIAA	25
<b>TPHL</b>	CLR	0	MAX	20
	CLN	D	IVIAA	26
ten	OERB	D	MAX	21
tdis	UEND	D	IVIAX	14
ten	ŌΕQ	0	MAX	18
tdis	ozu	u u	IVIAX	14

### 10-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

- 3-State I/O-Type Read-Back Inputs
- True Logic Outputs
- Bus-Structured Pinout

- 3-State I/O-Type Read-Back Inputs
  - True Logic Outputs
  - Sus-Structured Pineut
- Designed with Nine Bits for Parity Applications

### **Logic Diagram**



PROTECTION DATE OF THE PROTECTION

20172-15T73AFEBIS BUILDING

### RECOMMENDED OPERATING CONDITIONS

PAF	RAMETER	MAX or MIN	ALS	UNIT
Icc		MAX	82	mA
	Q	MAN	-2.6	mA
Іон	D	MAX	-0.4	mA
le:	0	MAX	24	mA
lor	D	WAX	8	mA

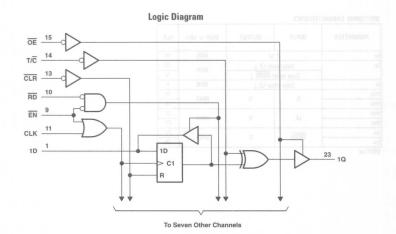
### SWITCHING CHARACTERISTICS

OTTITO OTTAINA	TEMOTIO		_	_
PARAMETER	INPUT OUTPUT		MAX or MIN	ALS
tw	C "H"		MIN	10
tsu	Data be	efor LE ↓	MIN	10
	Data befo	or OERB ↓	IVIIIV	10
th	Data affter LE ↓		MIN	5
tplh	D	0	MAX	14
tphl.	D	u u	IVIAA	18
tplh	LE	0	MAX	21
tphl .	LE	u		27
ten	OERB	n	MAY	21
tdis	UEND	D	MAX	16

HMIT-ne

### 8-BIT D-TYPE EDGE-TRIGGERED READ-BACK LATCHES

- 3-State I/O-Type Read-Back Inputs
- True Logic Outputs
- T/C Determines True or Complementary Data at Q Outputs



### RECOMMENDED OPERATING CONDITIONS

HEOOMHINEIT	DED OF EINTERING	ocitoo.	Т	
P	ARAMETER	MAX or MIN	ALS	UNIT
Icc		MAX	85	mA
	0	MAX	24	mA
lor	D	IVIAX	8	mA
	Q	MANY	-2.6	mA
Іон	8 D	MAX	-0.4	mA

### QUAD 2-INPUT NAND

### DO DATE Version of CALLAND

### Driver Version of SN74ASDI

### High Capacitive-Drive Capability

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
tw	CLR	low		10
	CLK	low	MIN	14.5
	CLK	high		14.5
tsu	Data befo	re CLK ↑		15
	EN low bet	ore CLK ↑	MIN	10
	CLK high be	fore EN ↑*1	IVIIN	15
	CLR high (inactiv	e) before CLK ↑	Am 16	10
th	Data afte	1/	0	
	EN low af	MIN	5	
	RD high aft		5	
tplH	CLK	Q	MAX	28
tphl.	( T/C = H or L )	MIN.		28
tplh	CLR (T/C = L)	0	MAX	27
tphl .	CLR (T/C = H)	u	IVIAA	23
tplh	T / P	T/C Q		23
tphl .			MAX	23
tphl .	CLR	D	MAX	30
ten*3	RD	D	MAX	16
tdis*4	NU	D	MAX	19
ten*3	EN	alfi a Dal	MAX	16
tdis**4	CIV III III	sid a Dol	IVIAA	19
ten*3	ŌE	0	MAY	15
tdis*4	OE.	4	MAX	10

## RABLE REFUNMENTERS NOW, AND STREET NOW, AND ST

### UNIT: ns \*1 This setup time ensures that EN

- \*1 This setup time ensures that EN will not false clock the date register.
- \*2 This hold time ensures that there will be no conflict on the input date bus. WE are \$4402.1AAVME to protect the results of the second secon
- $^{*3}$  =  $t_{\,\text{PZH}}$  or  $t_{\,\text{PZL}}$

-	- 6	HΖ	U	٠	PLZ	

### QUAD 2-INPUT NAND BUFFERS/DRIVERS

- Buffer Version of SN74ALS00A
- Driver Version of SN74AS00
- High Capacitive-Drive Capability

## Logic Diagram 1 2 4

1A

1B



Logic Diagram

### **FUNCTION TABLE**

INPUTS		OUTPUT
Α	В	Y
Н	Н	L
L	X	H
X	L	Н

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
Icc	MAX	7.8	19	mA
Іон	MAX	-2.6	-48	mA
lou	MAX	24	48	mA

### SWITCHING CHARACTERISTICS

JWITCHING CHAIL	ACTEMOTICS		T		
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
tPLH	A or B	63 v	MAX	8	4
tPHL	A OF B	EL	IVIAX	7	4

UNIT: ns

### 1004

### **HEX INVERTING DRIVERS**

- Driver Version of SN74ALS04B and SN74AS04
- High Capacitive-Drive Capability

### FUNCTION TABLE

TOTO HOLL INDEE				
INPUT A	OUTPUT			
H	L			

### RECOMMENDED OPERATING CONDITIONS

NEGOWINIENDED	OI LIMITING CON	T	,	_
PARAMETER	MAX or MIN	ALS	AS	UNIT
Icc	MAX	12	27	mA
Іон	MAX	-15	-48	mA
lo <sub>L</sub>	MAX	24	48	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
tPLH .	A or B	V	MAX	7	4
tPHL .	A OF B	1	IVIAX	6	4

### HEX INVERTING BUFFER GATES WITH OPEN-COLLECTOR OUTPUTS

Buffer Version of SN74ALS05A

### **FUNCTION TABLE**

INPUT A	OUTPUT
H	L
L	H

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	UNIT
lcc	MAX	12	mA
Vон	MAX	5.5	٧
loL	MAX	24	mA

### SWITCHING CHARACTERISTICS

				1
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
tpLH	Δ.	V	MAX	30
tphi	A	1	IVIAA	10

## UNIT: ns

### QUADRUPLE 2-INPUT POSITIVE-AND BUFFERS/DRIVERS

- Buffer Version of SN74ALS08
- Driver Version of SN74AS08

### **FUNCTION TABLE**

INP	UTS	OUTPUT
Α	В	Y
Н	Н	Haz
L	X	Agr
v	1	1

### RECOMMENDED OPERATING CONDITIONS

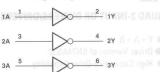
HEGOWINENDED	OF LIMITING CON	DITIONS		_
PARAMETER	MAX or MIN	ALS	AS	UNIT
lcc	MAX	9.3	22	mA
Іон	MAX	-2.6	-48	mA
lau	MAX	24	48	mA

### SWITCHING CHARACTERISTICS

SWITCHING CHAR	ACTERISTICS				_
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
tPLH .	A or B	V	MAX	9	6
tPHL .	A UI D	т.	IVIAA	9	6

### UNIT: ns

### Logic Diagram





### Logic Diagram

1A 1		3 1V	
1B 2	$\Box$ $\supset$	1Y 2 9 18	
1B —			

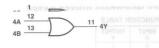
2A 4	-	6	
2B 5		2Y ydilidi	



44 12		10-1100	
4B 13	$oxed{oxed}$		

### OUAD 2-INPUT OR RUFFERS/DRIVERS





FUNCTION TABLE

INP	UTS	OUTPUT	
Α	В	Υ	
Н	X	Н	
X	H	H	
L	L	L	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
Icc	MAX	10.6	24	mA
Іон	MAX	-2.6	-48	mA
lou	MAX	24	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
tplH	A or B	YANA Y	MAX	9	6.3
tPHL	A or B	Y	MAX	12	6.3
UNIT:ns	30	633			

1034

### HEX DRIVERS

- SN74AS1034A Offer High Capacitive-Drive Capability
- Noninverting Drivers

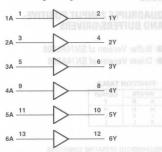
FUNCTION TABLE

INPUT A	OUTPUT
H	H -
1	1

RECOMMENDED	OPERATING CON	DITIONS	3	
PARAMETER	MAX or MIN	ALS	AS	UNIT
Icc	MAX	14	35	mA
Іон	MAX	-15	-48	mA

MAX

**Logic Diagram** 



SWITCHING CHARACTERISTICS

	Service of the Servic	,	_	,		1		
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	f to XAM		
tPLH .	٨	v	MAX	8	6			
tPHL .	А	, i	MAX	8	6	XAIR		
HMIT- ne				-	-			

48 mA

### **HEX BUFFERS WITH OPEN-COLLECTOR OUTPUTS**

Noninverting Buffers with Open-Collector Outputs

### **FUNCTION TABLE**

	INPUT A	OUTPUT
1	Н	H
L	L	L

### RECOMMENDED OPERATING CONDITIONS

TIEGOTATIVIETADED	OI EIDTING OOK	L	_
PARAMETER	MAX or MIN	ALS	UNIT
lcc	MAX	14	mA
Vон	MAX	5.5	V
loc	MAX	24	mA

### SWITCHING CHARACTERISTICS

FW1 -			263	1
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
tPLH		V	MAX	30
tPHL	A		IVIAX	12

### 1240

### **OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS**

- Low-Power Versions of SN74ALS240A
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers

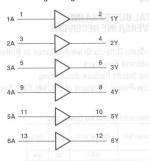
### PECOMMENDED OPERATING CONDITIONS

UPERATING CON	DITION	5
MAX or MIN	ALS	UNIT
MAX	13	mA
MAX	14	mA
MAX	-15	mA
MAX	16	mA
	MAX or MIN  MAX  MAX  MAX	MAX 13 MAX 14 MAX -15

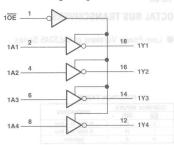
### SWITCHING CHARACTERISTICS

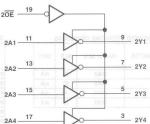
OTTITOTITIES	Ullimile	HOTEMOTIO	10 1140	10.11	
PARAMETE	R	INPUT	OUTPUT	MAX or MIN	ALS
tPLH .	25.	7	V	MAX	13
tPHL .	25	Ā	Yno A	30	13
tPZH	57	0E	V	MAX	20
tPZL	81	UE IVI	aYan A	30	22
tPHZ		ŌĒ	γ	MAX	10
tPLZ		UE			13
UNIT: ns					-

### Logic Diagram



### Logic Diagram





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### OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- pnp Inputs Reduce dc Loading
- Low-Power Versions of SN74ALS244 Series

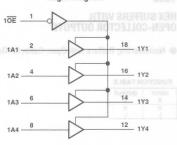
### RECOMMENDED OPERATING CONDITIONS

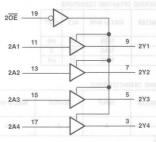
PARAMETER	MAX or MIN	ALS	UNIT
lccz	MAX	20	mA
ICCL	MAX	17	mA
Іон	MAX	-15	mA
lou	MAX	16	mA

### SWITCHING CHARACTERISTICS

SWITCHING CHAR	ACTERISTICS			_
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
tPLH	A	Y	MAX	14
tphl.				14
tPZH	ŌE	Y	MAX	22
tPZL	UE			22
tPHZ	ŌE	V	MAN	13
tPLZ	UE	Y	MAX	16
HAUT, no				

### Logic Diagram





### 1245

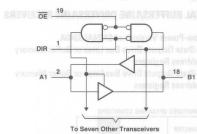
### **OCTAL BUS TRANSCEIVERS**

Low-Power Versions of 4ALS245 Series

### FUNCTION TABLE

CONTROL INPUTS		
OE	DIR	OPERATION
Lby	L.	B data to A bus
L	Н	A data to B bus
Н	X	Isolation

### Logic Diagram



### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	UNIT
lccz	MAX	36	mA
ICCL	MAX	33	mA
Іон гус —	MAX	-15	mA
lou	MAX	16	mA

### SWITCHING CHARACTERISTICS

				Г	1
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	10
tPLH TPLH	A or B	B or A	MAX	13	h
tPHL .	AUID	D OF A	IVIAX	13	1
tPZH	ŌE	A or B	MAX	25	
tPZL	UE			25	1
tрнz	ŌĒ	A or B	MAY	12	1
tPLZ		AUID	MAX	18	1

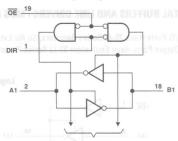
### Logic Diagram

### OCTAL BUS TRANSCEIVERS

- Lower-Power Versions of SN74ALS640B
- Inverting Logic Upon and anotalizable leman
- 3-State Outputs

FUNCTION TABLE

CONTROL INPUTS		
ŌĒ	DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
Н	X	Isolation



### To Seven Other Transceivers

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	UNIT
Icc	MAX	32	mA
Іон	MAX	-15	mA
lou	MAX	16	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
tplh	A or B	B or A	MAX	15
tPHL .	AOFB	D OF A	IVIAA	10
tpzh		ŌE A or B	MAX	20
tPZL	UE			22
tPHZ	ŌE	A or B	MAN	10
tPLZ	UE	A or B	MAX	13

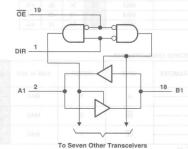
UNIT: ns

### 1645

### **OCTAL BUS TRANSCEIVERS**

- Lower-Power Versions of SN74ALS645A
- 3-State Outputs

### Logic Diagram



### **FUNCTION TABLE**

П	CONTROL INPUTS			
	ŌĒ	DIR	OPERATION	
	L	L	B data to A bus	
	L	H	A data to B bus	
	Н	X	Isolation	

### RECOMMENDED OPERATING CONDITIONS

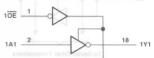
PARAMETER	MAX or MIN	ALS	UNIT
Icc	MAX	38	mA
Іон	MAX	-15	mA
lou	MAX	16	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	
tplH	A or B	B or A	MAX	13	
tphl	AorB	BOLA	IVIAX	13	
tPZH	ŌĒ		A D	MAN	25
tPZL	UE	A or B	MAX	25	
tphz	ŌE	A D	MAN	12	
tPLZ	UE	A or B	MAX	18	

UNIT: ns

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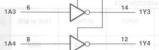


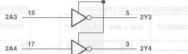












RECOMMENDED	OPERATING	CONDITIONS	

PARAMETER	MAX or MIN	ALS	ВСТ	ABT	UNIT
Iccz	MAX	20	8	0.25	mA
ICCL	MAX	23	76	30	mA
Гон	MAX	-15	-12	-32	mA
lor	MAX	15	12	12	mA

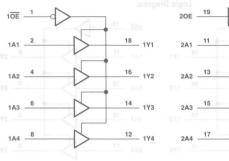
SWITCHING CHARACTERISTICS

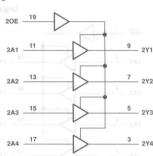
SWITCHING CHAR	ACTERISTICS					
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	вст	ABT
tPLH	A	V .	MAX	10	5.7	4.8
tphl.	A	1	IVIAA	10	4.4	5.4
tPZH	ŌĒ	V	MAX	17	9.3	5.2
tPZL	UE	1	MAX	20	12.4	6.8
tPHZ	ŌE	- v	MAX	10	8.7	6.4
tPLZ	UE	V 1	IVIAA	15	10.6	6.2

### OCTAL BUFFERS AND LINE DRIVERS / MOS DRIVERS WITH 3-STATE OUTPUTS METABLES LATTED

- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABT2241A)
  - Output Ports Have Equivalent 33-Ω Series Resistors, So No External Resistors Are Required (SN74BCT2241)

### Logic Diagram





### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	ABT	UNIT
lccz	MAX	9	0.25	mA
Iccı	MAX	76	30	mA
Іон	MAX	-12	-32	mA
lor	MAX	12	12	mA

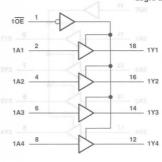
### SWITCHING CHARACTERISTICS

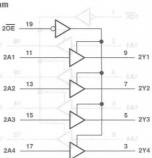
SWITCHING CHARACTERISTICS					1117
PARAMETER	INPUT	PUT OUTPUT MAX or		SN74 BCT	ABT
tPLH	A		MAX	4.9	4.7
tPHL .	A Y MAX		6.9	5.6	
tPZH	10E	Y	MAX	8.9	5.8
tPZL	10E	T	IVIAA	10.3	8.4
tPHZ	10E	Y	MAX	8.7	6.6
tPLZ	105	,	IVIAX	11.3	6.4
tPZH	20E	Y	MAX	8.9	5.8
tPZL	ZUE	т т	MAX	10.3	8.4
tPHZ	20E	Y	MAN	8.7	6.6
tPLZ	ZUE	Y	MAX	11.3	6.4

### OCTAL BUFFERS AND LINE DRIVERS / MOS DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABT2244A)
  - Output Ports Have Equivalent 33-Ω Series Resistors, So No External Resistors Are Required (SN74BCT2244)
  - $\bullet \ \, \text{Output Ports Have Equivalent 26-} \Omega \, \text{Series Resistors, So No External Resistors Are Required (SN74LVC2244A)} \\$

Logic Diagram





### **FUNCTION TABLE**

INPL	JTS	OUTPUT
ŌĒ	Α	Y
Н	X	Z
L	L	L
L	Н	H

### RECOMMENDED OPERATING CONDITIONS

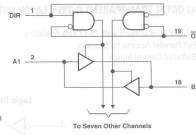
PARAMETER	MAX or MIN	ALS	SN74 BCT	ABT	LVC 3V	UNIT
lccz	MAX	23	10	0.25	0.01	mA
ICCL	MAX	22	77	30	0.01	mA
Гон	MAX	-15	-12	-32	-12	mA
lou	MAX	15	12	12	12	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 BCT	ABT	TAC 3A
tPLH .		v	MAN	16	4.9	4.7	5.5
tPHL .	A	Y	MAX	17	6.7	5.6	5.5
tPZH			1447	17	8.7	5.5	7.1
tPZL	UE		MAX	14	10.4	8.3	7.1
tPHZ	<u> </u>		1444	9	7.8	6.6	6.8
tPLZ	UE	Y	MAX	9	9.8	5.8	6.8

### OCTAL TRANSCEIVER AND LINE/ TATE-6 HT MOS DRIVERS WITH 3-STATE OUTPUTS

- B Port Has Equivalent 33-Ω Series Resistors, So No External Resistors Are Required (SN74BCT2245)
- B-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABT2245)
- Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABTR2245)
- All Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required (SN74LVCR2245)
- B-Port Outputs Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required (SN74LVTH2245)



### **FUNCTION TABLE**

INPUTS						
OE DIR			OPE	KA	ПС	N
L	L	В	data	to	Α	bus
L	Н	Α	data	to	В	bus
H	X	Isolation				

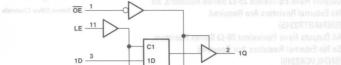
### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	ABT	ABTR	LVCR 3V	LVTH 3V	UNIT
lccz	MAX	15	0.25	0.25	0.01	0.19	mA
Iccı	MAX	100	32	32	0.01	5	mA
loн (A port)	MAX	-3	-32	-12	-12	-32	mA
loн (B port)	MAX	-12	-12	-12	-12	-12	mA
lot (A port)	MAX	24	64	12	12	64	mA
lot (B port)	MAX	12	12	12	12	12	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT	ABT	ABTR	LVCR 3V	LVTH 3V
tPLH		В	MAX	5.8	3.8	3.8	6.3	4.4
tPHL .	A	В		7.8	4.5	4.5	6.3	4.4
tPLH .	В	A	MAX	7	3.6	3.8	6.3	3.5
tPHL .	Ь	A	WAX	7.7	4	4.5	6.3	3.5
tPZH	ŌĒ	В	MAX	9.9	6.1	6.1	8.2	6.2
tPZL		В	IVIAA	12.2	6.3	6.3	8.2	6.2
tPHZ	ŌE	В	MAX	8.2	5.3	5.3	7.8	5.9
tPLZ	UE	В		9.2	4.8	4.8	7.8	5.4
tPZH	ŌE	A	MAN	11.1	5.5	6.1	8.2	5.5
tPZL	UE	A	MAX	11.4	5.7	6.3	8.2	5.5
tPHZ	ŌĒ	Α	MAX	9.4	5.6	5.3	7.8	5.9
tPLZ	UE	A	MAX	7.6	4.5	4.8	7.8	5

B-Port Outputs nave equivelent are Regulard Resistors, So No External Resistors Are Regulard margaid



To Seven Other Channels

### Logic Diagram

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	F	UNIT
lcc	MAX	66	mA
Іон	MAX	-3	mA
lou	MAX	12	mA

### SWITCHING CHARACTERISTICS

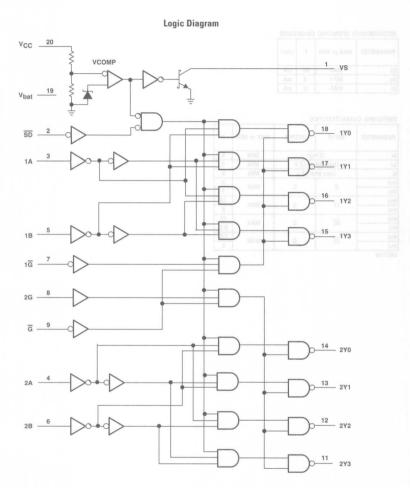
PARAMETER	INPUT	OUTPUT	MAX or MIN	F
tiv	LE high		MIN	6
tsu	Data be	fore LE ↓	MIN	2
th	Data a	fter LE ↓	MIN	6
tPLH	D	0	MAX	9
tPHL .	U	u	IVIAX	7
tPLH	LE	0 0	MAX	13
tPHL .	LE	u	WAX	8
tРZH	ŌE	n	MAX	12
tPZL	UE	u	IVIAX	9.5
tPHZ	ŌĒ		MAX	7.5
tPLZ	UE	u	IVIAX	6

UNIT:ns

### MEMORY DECODER WITH ON-CHIP V<sub>CC</sub> MONITOR

- Built-In Supply-Voltage Monitor for V<sub>CC</sub>
- Separate Enable Inputs for Easy Cascading

### | FUNCTION TABLE | (sec) letch) | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 100 | 10



### FUNCTION TABLE

	R	NPUT	S			OUT	DUITE	
CONTROL			SELECT		OUTPUTS			
G	1G	SD	1B	1A	1Y0	111	112	113
Н	X	X	X	X	Н	Н	H	H
X	Н	X	X	X	Н	H	Н	H
X	X	L	X	X	Н	H	H	Н
L	L	H	L	L	L	H	H	H
L.	L	H	L	H	H	L	H	H
L	L	H	H	L	H	H	L	H
L	L	H	H	Н	H	H	H	L

	PUTS	OUT			S	IPUT	11	
	013	0011		ECT	SEL	OL	NTR	CC
2Y3	2Y2	2Y1	2Y0	2A	2B	SD	2G	G
H	Н	Н	Н	X	X	X	X	Н
H	H	H	H	X	X	X	H	X
H	H	Н	Н	X	X	L	X	X
H	H	H	L	L	L	Н	H	L
H	H	L	Н	Н	L	H	H	L
H	L	H	H	L	H	H	H	L
41.1	H	Н	н	H	H	H	H	1

RECOMMENDED	OPERATING	CONDITIONS

ILCONNINCTADED	OI EIIATIITO OOI	DITTOTAL		
PARAMETER	MAX or MIN	SN74 BCT	UNIT	
lcc	MAX	3	mA	
Іон	MAX	-0.4	mA	
lbst (Output low)	MAX	3	mA	
lou	MAX	8	mA	

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	ОИТРИТ	MAX or MIN	SN74 BCT
tPLH .	A or B	AV	MAX	12
tPHL .	A or B	Any Y	IVIAX	12
tPLH	A	AV	MAX	10
tPHL .	Any G	Any Y	MAX	11
tPLH	SD	Any Y	MAX	12
tPHL	30	Any t	IVIAA	12
tPLH .	N	A V	MAX	250
tPHL	V <sub>cc</sub>	Any Y	IVIAA	250
tPLH		VS	MAX	250
tPHL .	V <sub>cc</sub>	V.S	IVIAA	250

### RECOMMENDED OPERATING CONDITIONS

RECOMMENDED	OFENATING CON	DITION	3
PARAMETER	MAX or MIN	ALS	UNIT
lccz	MAX	22	mA
Icci	MAX	25	mA
Іон	MAX	-0.4	mA
lou	MAX	12	mA

### SWITCHING CHARACTERISTICS

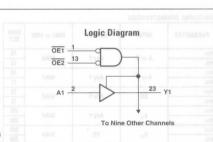
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
tPLH		Y	MAX	15
tPHL .	А	,	IVIAA	12
tPZH	ŌĒ		MAX	15
tPZL	UE	Y		20
tPHZ	ŌE	Y	MAN	10
tPLZ	UE	1.	MAX	12

All output resistors are 25  $\Omega$ .

2827

### 10-BIT BUS/MOS MEMORY DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABT2827)
- Output Ports Have Equivalent 25-Ω Resistors; No External Resistors Are Required (SN74BCT2827C)



RECOMMENDED OPERATING CONDITIONS

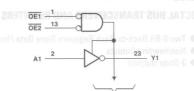
PARAMETER	MAX or MIN	SN74 BCT	ABT	UNIT
lccz	MAX	6	0.25	mA
lccL	MAX	40	40	mA
Іон	MAX	-1	-12	mA
lou	MAX	12	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT	ABT
tPLH .	Δ.	Y	MAX	6	5.5
tphl.	Α		IWIAA	7.8	5.1
tPZH	ŌĒ	Y	MAX	10.7	6.7
tPZL	UE	1	IVIAA	12.9	7.8
tPHZ	ŌE	γ	MAN	13	7.2
tPLZ	UE	, ,	MAX	10	7.5

### 10-BIT BUS/MOS MEMORY DRIVERS WITH 3-STATE INVERTING OUTPUTS

 Output Ports Have Equivalent 33-Ω Series Resistors, So No External Resistors Are Required (SN74BCT2828)



To Nine Other Channels

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	UNIT
lccz	MAX	6	mA
lccr.	MAX	40	mA
Іон	MAX	-1	mA
lou	MAX	12	mA

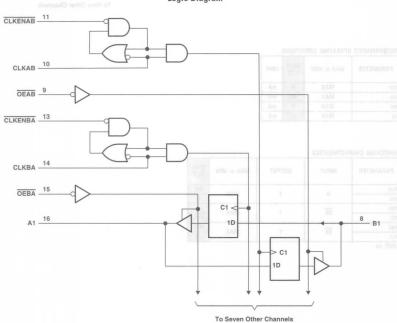
### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT
tPLH		V	MAX	6.6
tphl.	Α	1	IVIAX	5
tPZH	ŌĒ	V	MAX	9
tPZL R	UE	,	IVIAA	11.5
tPHZ	ŌE	V	MAX	10.8
tPLZ	UE	1	IVIAA	8.7

### **OCTAL BUS TRANSCEIVERS AND REGISTERS**

- Two 8-Bit Back-to-Back Registers Store Data Flowing in Both Directions
- Noninverting Outputs 3-State Outputs





### **FUNCTION TABLE†**

	INPUTS					
CLKENAB	CLKAB	OEAB	A	В		
Н	X	L	X	Bo		
L	1	L	L	L		
L	1	L	H	and Han		
X	X	H	X	Z		

† A-to-B data flow is shown; B-to-A data flow is similar but uses CLKENBA, CLKBA, and OEBA.
‡ Level of B before the indicated steady-state input conditions were established

### RECOMMENDED OPERATING CONDITIONS

P/	ARAMETER	MAX or MIN	SN74 BCT	ABT	SV.	LVT 3V	UNIT
Icc		MAX	55	35	0.01	5	mA
Іон	A	MAX	-3	-32	-24	-32	mA
IUH	В	IVIAA	-15	-32	-24	-32	mA
lou	A	MAX	24	64	24	64	mA
IUL	В	IVIAA	64	64	24	64	mA

SWITCHING CHARACTERISTICS

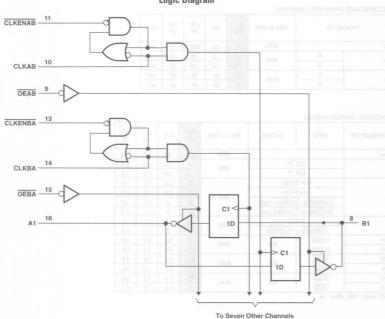
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT	ABT	3V LVC	LVT 3V
fmax			MIN	125	150	150	150
tw	CLK	"H"	MIN	4	3.3	3.3	3.3
	CLK	"L"	IVIIIV	4	3.3	3.3	3.3
tsu	A or E	High		2.5	2.5	1.3	1.5
	A or B Low  CLKENAB or CLKENBA High  CLKENAB or CLKENBA Low		MIN	2.5	2.5	1.3	1.5
				2	3	1.1	1.5
			5 10	2	3	1.1	1.9
th page 1	Ac	r B	MIN	1.5	1.5	1.1	1
	CLKENAB o	r CLKENBA	IVIIIV	2.5	2	1.1	1.2
tPLH	CLKBA	A,B	MAX	9	5.9	8.2	4.6
tPHL .	CLKAB	A,D	IVIAA	10.5	6.3	8.2	4.6
tPZH	OEBA	A,B	MAX	8.2	5.6	7.8	4.6
tPZL	OEAB	G A,D	IVIAA	12.9	6.6	7.8	4.6
tPHZ	OEBA	A,B	MAX	8.4	6.4	7.8	5.4
tPLZ	OEAB	A,D	IVIAA	7	6.2	7.8	5.1

UNIT fmax : MHz other : ns

### **OCTAL BUS TRANSCEIVERS AND REGISTERS**

- Two 8-Bit, Back-to-Back Registers Store Data Flowing in Both Directions
- Inverting Outputs
- 3-State Outputs

### **Logic Diagram**



	INP	ОИТРИТ		
OEAB	CLKAB	OEAB	Α	В
Н	1	L	X	Ao
L	1	L	L	Н
L	1	-a	H	10
X	X	Н	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses
CEBA, CLKBA, and OEBA.

‡ Level of B before the indicated steady-state input conditions were



RECOMMENDED OPERATING CONDITIONS

PARA	METER	MAX or MIN	SN74 BCT	UNIT
lcc		MAX	55	mA
	A	v	-3	mA
Іон	В	MAX	-15	mA
	A	1111	24	mA
lor	В	MAX	64	mA

SWITCHING CHARACTERISTICS

OTTITOTING GIA	11/10/12/11/01/100						
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT			
fmax			MIN	110			
tw	CL	K "H"	MIN	4.5			
	CL	K "L"	IVIIIN	4.5			
tsu	A or	B High	Aris	2.5			
	A or	B Low	MIN	2.5			
	CLKENAB or	CLKENBA High	Acre	2			
	CLKENAB or	CLKENBA Low	Lot	2			
th	A	or B	MIN	1.5			
	CLKENAB	or CLKENBA	Am	2			
tPLH	CLKBA	A,B	MAX	9.5			
tphl.	CLKAB	A,D	IVIAA	10.2			
tPZH	OEBA	A,B	MAX	8.8			
tPZL	OEAB	A,D	WIAA	14			
tPHZ	OEBA	A,B	MAX	9.1			
tPLZ	OEAB	A,D	MAA	7.6			

UNIT fmax : MHz other : ns

### OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

# Logic Diagram DIR 22 OE A1 To Seven Other Channels

### **FUNCTION TABLE**

INP	UTS	
OE	DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

RECOMMEN	NDED OPERATIN	G CONDITIONS								
PAI	RAMETER	MAX or MIN	V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	LVCC	UNIT	KAM			
	1			OPEN	0.05	mA	M			
ICCA	B to A	MAX	3.6	3.6	0.05	mA	103			
				5.5	0.05	mA				
	4	1447	0.0	3.6	0.05	mA				
ICCB	A to B	MAX	3.6	5.5	0.08	mA	N/			
		MAN	2.7		-12	mA				
Іона		MAX	3.3	3	-24	mA				
		1447	2.7	3.3	-12	mA	100			
Іонв		MAX	3.3	3	-24	mA				
1000			2.7	_	12	mA	105			
IOLA		MAX	3.3	3	24	mA				
			2.7	3.3	12	mA	100			
IOLB		MAX	3.3	3	24	mA				
			2.10			100	NIM			

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	$V_{CCA} = 2.5V$ $V_{CCB} = 3.3V$	$V_{CCA} = 3.6V$ $V_{CCB} = 5V$
tPLH .	A	В	MAX	9.4	6
tphL .	А	B MAX		9.1	5.3
tPLH	В	A	MAX	11.2	5.8
tPHL .	В	A	IVIAX	9.9	7
tPZL	ŌĒ	Ā	MANY	14.5	9.2
tPZH	UE	A	MAX	12.9	9.5
tPZL	ŌĒ	B	144V	13	8.1
tРZH	UE	В	MAX	12.8	8.4
tPLZ	ŌĒ	Ā	MAN	7.1	7
tphz	UE	A	MAX	6.9	7.8
tPLZ	ŌĒ	B	MAN	8.8	7.3
tPHZ	UE	В	MAX	8.9	7

### **DUAL 4-INPUT POSITIVE-NOR GATES**

 $Y = \overline{A + B + C + D}$ 



Logic Diagram

### **FUNCTION TABLE**

	INP	UTS		OUTPUT
Α	В	C	D	Y
L	L	L	L	Н
H	X	×	X	rotte f
X	H	X	X	L
X	X	H	X	L
X	X	X	Н	_ L/

NOTES: H = High Voltage Level L = Low Voltage Level X = Irrelevant

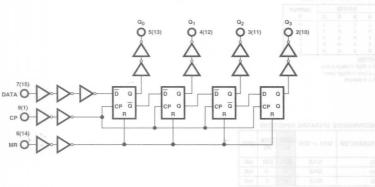
### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	UNIT
lcc	MAX	0.02	0.04	mA
Іон	MAX	-4	-4	mA
lou	MAX	4	4	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74
tPLH	A D C D	V	MAX	28	30
A, B, C, D		Y	MAX	28	30

### Logic Diagram



### **FUNCTION TABLE**

INPUTS			OUTPUT			
CP	D	R	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q3
1		L	L	q'o	q'1	q'2
1	h	L	Н	g'o	91	92
1	X	L	q'o	91	92	q's
X	X	Н	L	L	L	L

- H = High Voltage Level
  h = High Voltage Level One Set-up Time Prior to the Low to High
  Clock Transition
- L = Low Voltage Level
  I = Low Voltage Level One Set-up Time Prior to the Low to High Clock Transition

- Clock Transition X = Dn't Care X = Dn't C

### RECOMMENDED OPERATING CONDITIONS

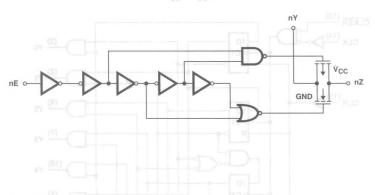
PARAMETER	MAX or MIN	CD74 HC	UNIT
lcc	MAX	0.16	mA
Гон	MAX	-4	mA
lou	MAX	4	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
fmax			MIN	45
tw	C	lock		24
		MR	MIN	45
tsuL	D-4-	In to CP	MIN	18
tsun	Data-	in to CP	MIN	18
th	Data-In to CP		MIN	0
tPLH .	Clock	0-	MAX	54
tphl.	CIOCK	Qn		54
tPLH .	MR	Qn	MAX	83
tPHL	IVIN	(Clock High)	WAX	83
tplh	MD	Qn	MAN	98
tphl.	MR	(Clock Low)	MAX	98

UNIT fmax: MHz other:ns

### Logic Diagram



### **FUNCTION TABLE**

INPUT nE	SWITCH
L	OFF
Н	ON
7777777	

NOTES: H = High Level Voltage L = Low Level Voltage

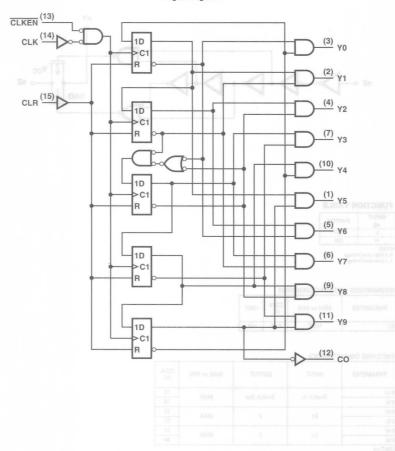
### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
Icc	MAX	0.32	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
TPLH .	Switch In	Switch Out	MAX	18
tphL .				18
tPZH	En	Z	MAX	57
tPZL				57
tPHZ	En	_		44
tPLZ		Z	MAX	44

Logic Diagram



OUTPUT	INPUTS					
STATET	CLR	CLKEN	CLK			
No Change	L	X	L			
No Change	L	Н	X			
"0" = H, "1"-"9" = L	н	×	X			
Increments Counter	L	L	1			
No Change	L	X	1			
No Change	L	1	X			
Increments Counter	1	Ť.	н			

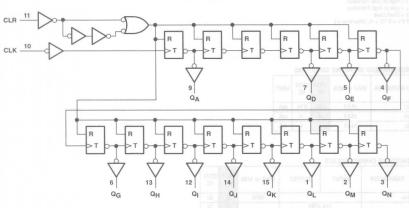
# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	UNIT
lcc	MAX	0.08	0.16	mA
Іон	MAX	-4	-4	mA
lot -	MAX	4	4	mA

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC
fmax	- 80	70	MIN	25	20
	CLI	(CP)	MIN	20	24
tw	CLR	(MR) H	MIN	20	24
	CLKEN to C	CLKEN to CLK (CE to CP )		13	22
tsu	CLK Inactive		MIN	13	-
th	CLKEN to CLK (CE to CP )		MIN	5	0
tplh	CLK Y, CO		MAX	58	69
tphL .	(CP)	(0 to 9, TC)	IVIAX	58	69
tplh	CLKEN	Y, C0	MAX	63	75
<b>TPHL</b>	(CE)	(0 to 9, TC)	IVIAA	63	75
tplH .	CLR	Y	MAX	58	69
tphl .	(MR) (0 to 9)		IVIAX	58	69
tPLH .	CLR	CO	MAN	-	69
TPHL	(MR)	(TC)	MAX	58	69

UNIT fmax : MHz, other : ns

# Logic Diagram



## **FUNCTION TABLE**

1	CLK	CLR	OUTPUT
Ī	*	L	No Change
	4	L	Advance to Next State
1	X	Н	All Outputs Are Low

 $\begin{aligned} &\text{NOTE: H = High Voltage Level, L = Low Voltage Level,} \\ &\text{X = Don't Care,} = \uparrow Transition from Low to High Level,} \\ &\text{$\downarrow$ = Transition from High to Low.} \end{aligned}$ 

## RECOMMENDED OPERATING CONDITIONS

HECONNINCIADED OF ENATING CONDITIONS								
PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT			
Icc	MAX	0.08	0.16	0.16	mA			
Іон	MAX	-4	-4	-4	mA			
IOL.	MAX	4	4	4	mA			

## SWITCHING CHARACTERISTICS

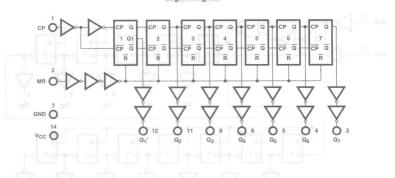
SWITC	HING CHARACTER	RISTICS					
F	PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
fmax				MIN	22	20	16
	CLK	1		MIN	23	24	30
tw	CLR high	1			18	24	30
tsu	CLK	CLR inactive	before CLK ↓	MIN	15	-	-
tPLH tPHL tPHL		OLK	0.	MANY	38	42	60
		CLK	QΑ	MAX	38	42	60
		CLR	Any	MAX	35	51	60

UNIT fmax : MHz other : ns

Same Pinouts as CM0S4040

1 Vec 2V to 6V

# **Logic Diagram**



**FUNCTION TABLE** 

CLK	CLR	OUTPUT STATE		
1	L	No Change		
1	L	Advance to Next State		
X	Н	All outputs Are Low		

H = High Voltage Level, L = Low Voltage Level, X = Don't Care, † = Transition form Low to High Level, \( \pm = \text{Transition} \) High to Low.

RECOMMENDED OPERATING CONDITIONS

TIEGOWINIETADED OF ETIATING CONDITIONS							
PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT		
Icc	MAX	0.08	0.16	0.16	mA		
Іон	MAX	-4	-4	-4	mA		
lou	MAX	4	4	4	mA		

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SWITCHING CHARACTERISTICS

OTTITO OTTA	NOTEMOTIO			-		_
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
fmax		00 00	MIN	22	20	16
tw	CLK (CP)		MIN	23	24	30
	CLR (I	MR) H	MIN	20	24	30
tsu	CLR iow b	efore CLK	MIN	20	-	(6)76
tPLH	CLK	QA	MAX	30	42	60
tphl.	(CP)	(01)	IVIAX	30	42	60
tplh	CLD (MAD)	0	MAN		51	60
tphl .	CLR (MR)	any Q	MAX	33	51	60

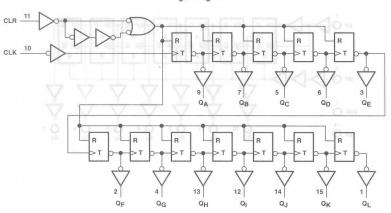
UNIT fmax: MHz, other: ns

# 12-STAGE BINARY COUNTERS

7-STAGE BINARY COUNTERS

- Same Pinouts as CMOS4040
- V<sub>CC</sub>: 2V to 6V

# Logic Diagram



**FUNCTION TABLE** 

CLK	CLR	OUTPUT
1	L	No Change
1	L	Advance to Next State
X	Н	All Outputs Are Low

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care,  $\hat{T}$  = Transition from Low to High Level,  $\hat{J}$  = Transition from High to Low.

RECOMMENDED OPERATING CONDITIONS

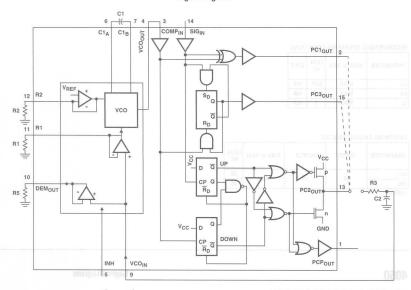
PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
Icc	MAX	0.08	0.16	0.16	2	0.02	mA
Іон	MAX	-4	-4	-4	-6	-12	mA
lou	MAX	4	4	4	6	12	mA

SWITCHING CHARACTERISTICS

1	PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	3V	LV 5V	
fmax				MIN	22	20	16	50	80	
tiv	CLK			MINI	23	24	30	5	5	
LW	CLR high			high	MIN	18	24	30	5	5
su	CLK	CLR inactive	before CLK ↓	MIN	15	-	116/1-	5	5	
PLH		CLK	QA	MAN	38	42	60	17.5	10.5	
PHL		CLK UA		MAX	38	42	60	17.5	10.5	
PHL		CLR	Any	MAX	35	51	60	18.5	12	

UNIT fmax : MHz other : ns

# Logic Diagram



# Pin Descriptions

PIN NUMBER	SYMBOL	NAME AND FUNCTION	
1	PCPOUT	Phase Comparator Pulse Output	
2	PC1 <sub>OUT</sub>	Phase Comparator 1 Output	
3	COMPIN	Comparator Input	
4	VCO <sub>OUT</sub>	VCO Output	
5	INH	Inhibit Input	
6	C1 <sub>A</sub>	Capacitor C1 Connection A	
7	C1 <sub>B</sub>	Capacitor C1 Connection B	
8	GND	Ground (0V)	
9	VCOIN	VCO Input	
10	DEMOUT	Demodulator Output	
11	R <sub>1</sub>	Resistor R1 Connection	
12	R <sub>2</sub>	Resistor R2 Connection	
13	PC2 <sub>OUT</sub>	Phase Comparator 2 Output	
14	SIGIN	Signal Input	
15	PC3 <sub>OUT</sub>	Phase Comparator 3 Output	
16	Vcc	Positive Supply Voltage	

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
lcc	MAX	0.16	0.16	mA
Іон	MAX	-4	-4	mA
lou	MAX	4	4	mA

# SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
tPLH	SIGIN	DOL	MAN	60	68
tPHL	COMPIN	PCIout MAX		60	68
tPLH	SIGIN	PCPout	MAN	90	102
tPHL	COMPIN	PCPOUT	MAX	90	102
tPLH AVGO	SIGIN	РСЗоит	- A44V	74	87
tPHL 37	COMPIN	PU3001	MAX	74	87
ttlh	٨	y y	MAX	22	22
tthl ac	A	Yn Y	IVIAX	22	22
tрzн	SIGIN	DC2 our	MAX	80	90
tPZL	COMPIN	PC2out	IVIAX	80	90
tPLZ	SIGIN	000	1117	95	102
PHZ COMPIN		PC2out	MAX	95	102



Logic Diagram



SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
tPLH	-	V V	MAY	26
tPHL E	nA	nY	MAX	26

4050

Logic Diagram

# **HEX NON-INVERTING BUFFERS**

RECOMMENDED	OPERATING	CONDITIONS	

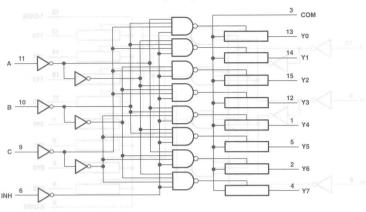
TEOOMINETEDE	D OI LIMITING	CONTO	110140
PARAMETER	MAX or MIN	CD74 HC	UNIT
Icc	MAX	0.04	mA
Іон	MAX	-4	mA
lou	MAX	4	mA

# SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
tPLH .	XALL	nY	MAY	26
tPHL .	nA	ny	MAX	26
UNIT:ns	XXIV	PCtour	COMPU	20

| Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj. | Proj

# Logic Diagram



# **FUNCTION TABLE**

	INP	UTS		ON
INH	С	В	Α	CHANNEL
L	L	L	L	YO
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7
H	X	X	X	None

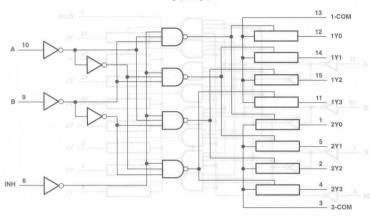
RECOMMENDED	OPERATING CON	DITIONS	5							
PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT				
Icc	MAX	0.16	0.16	(*)	0.02	mA				

# SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V
tPLH .	0011	Yn or COM	MAX	18	18	12	8
tPHL.	COM or Yn	Yn or CUIVI		18	18	12	8
tPZH	18111	COM or Yn	MAX	68	83	25	18
tPZL	INH			68	83	25	18
tPHZ		2011	T 7474	68	68	25	18
tPLZ	INH	COM or Yn	MAX	68	68	25	18

# DUAL 4-CHANNEL ANALOG MULTIPLEXERS / DEMULTIPLEXERS | STEELING BOLIAMA JEMMAHD-8

Logic Diagram



# **FUNCTION TABLE**

- 1	NPUTS	3	ON
INH B		A	CHANNEL
L	L	L	1Y0, 2Y0
L	L	H	1Y1, 2Y1
L	H	L	1Y2, 2Y2
L	H	H	1Y3, 2Y3
H	X	X	None

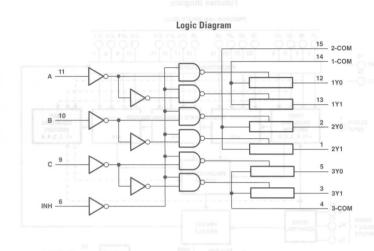
# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74	CD74 HCT	LV 3V	LV 5V	UNIT
Icc	MAX	0.16	0.16		0.02	mA

# SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V	
tPLH .	00M V-	V COM	MAX	18	18	12	8	1
tphL .	COM or Yn	Yn or COM	IVIAA	18	18	12	8	101
tpzh	INH	COM or Yn	MAN	98	105	25	18	1
tPZL	IINH		MAX	98	105	25	18	100
tPHZ	INH	COM or Yn	1447	75	75	25	18	1
tPLZ	шип	COIVI OF TH	MAX	75	75	25	18	10

# TRIPLE 2-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS MID 338AMMARDORS 20MD



**FUNCTION TABLE** 

	INP	UTS		ON CHANNEL
INH	С	В	Α	ON CHANNEL
L	L	L	L	1Y0, 2Y0, 3Y0
L	L	L	H	1Y1, 2Y0, 3Y0
L	L	H	L	1Y0, 2Y1, 3Y0
L	L	Н	H	1Y1, 2Y1, 3Y0
L	H	L	L	1Y0, 2Y0, 3Y1
L	H	L	H	1Y1, 2Y0, 3Y1
L	H	H	L	1Y0, 2Y1, 3Y1
L	H	H	Н	1Y1, 2Y1, 3Y1
Н	X	X	X	None

# RECOMMENDED OPERATING CONDITIONS

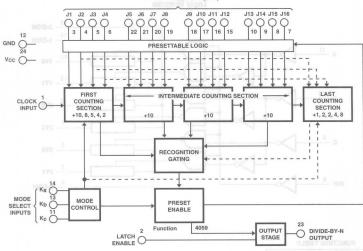
PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
Icc	MAX	0.16	0.16	-	0.02	mA

## SWITCHING CHARACTERISTICS

SWITCHING CHA	RACIERISTICS	1.3H					
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V
tPLH	COM or Yn	Yn or COM	MAX	18	18	12	8
tphl .	CUIVI OF YH	Yn or Culvi	IVIAA	18	18	12	8
tPZH	INH	COM or Yn	MAX	66	72	25	18
tPZL	IIVII	COIVI OI III	IVIAA	66	72	25	18
tPHZ	INH	COM or Yn	MAX	63	66	25	18
tPLZ	IINH	COIVI OI TII	IVIAA	63	66	25	18

# **Function Diagram**

## PROGRAM JAM INPUTS (BCD)



## **FUNCTION TABLE**

MODE	SELECT	INPUT
Ka	Kb	Kc
H	H	Н
L	Н	H
H	L	H
L	L	H
H	Н	L
X	L	L

# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
lcc	MAX	0.16	mA
Іон	MAX	-4	mA
lou	MAX	4	mA

# SWITCHING CHARACTERISTICS

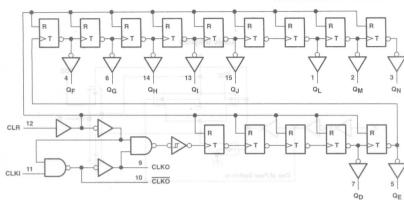
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	
fmax		CP - 4500	MIN	18	
tw	46 (	CP	MIN	27	
tsu	Kb, K	c to CP	MIN	22	
tPLH	CP	0	MAN	60	
tPHL	UP	u	MAX	60	
tPLH	I.E.	0	5.5.5.V	53	
tPHL .	LE	u	MAX	53	



V<sub>cc</sub>: 2V to 6V



# **Logic Diagram**



# **FUNCTION TABLE**

INP	UTS	OUTPL	JTS		
CLKI	CLR	QD to QN	CLKO	CLKO	
1	L	No Change	1	1	
1	L	Advance to Next State	1	1	
X	H	All Outputs are Low	L	H	

# OPERATING CONDITIONS

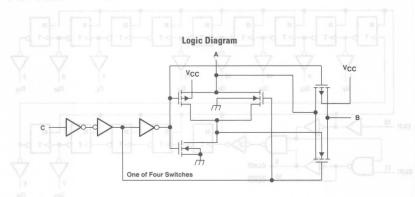
MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
MAX	0.08	0.16	0.16	mA
- MAX	-4	-4	-4	mA
MAX	4	4	4	mA

PARAMETER	INPUT OUTPUT		MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
fmax			MIN	22	20	20
tw	C	LKI	MAIN	23	24	24
	CLR	high	MIN	23	24	38
tsu	CLR inactive before CLK ↓		MIN	40	-	X/S/
tPLH	CLKI	0-	MAN	123	90	100
tphl.	CLKI	ΩD	MAX	123	90	100
tphl.	CLR	Any	MAX	35	53	66

UNIT fmax : MHz other : ns

# QUADRUPLE BILATERAL SWITCHES 20 0MA 2837MU00 YBAMIS 20AT2-AT 2U0MORHORY2A

- Same Pinouts as CMOS4016, 4066
- Low On-State Impedance: 50-Ω TYP at V<sub>CC</sub> = 6V
   A State Impedance: 50-Ω TYP at V<sub>CC</sub> = 6V
   A State Impedance: 50-Ω TYP at V<sub>CC</sub> = 6V
- Individual Switch Controls
- Extremely Low Input Current
- High On-Off Output Voltage Ratio
- Low Crosstalk Between Switches



# **FUNCTION TABLE**

INPUT (C)	SWITCH	
L	OFF	
Н	ON	ī

NOTE: H = High Level L = Low Level

# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
Icc	MAX	0.02	0.04	0.04		0.02	mA

V8 or V5 :20 W

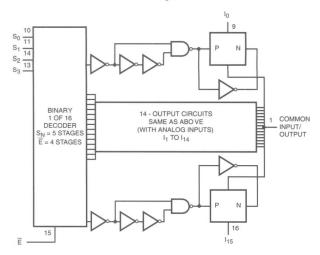
# SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V
tPLH	A D	D A	MAX	15	18	18	12	8
tphl.	A or B	B or A	IVIAA	15	18	18	12	8
tpzh	0	A D		45	30	36	22	16
tPZL	С	A or B	MAX	45	30	36	22	16
tPHZ		C A or B		50	45	53	22	16
tPLZ	C		MAX	50	45	53	22	16

# **16-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER**

7.8.4.7.4

# **Function Diagram**



# **FUNCTION TABLE**

S0	S1	S2	S3	Ē	SELECTED CHANNEL
X	X	X	X	X	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

NOTES: H = High Level L = Low Level

# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
Icc	MAX	0.16	0.16	mA

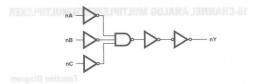
# SWITCHING CHARACTERISTICS

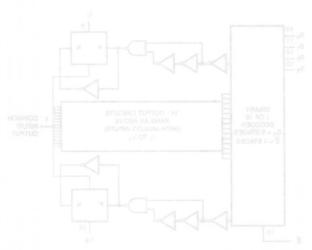
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
tPLH .	Switch In	COMON I/O	MAX	22	22
tphl.	Switch in	COMON I/O	MAX	22	22
tPZH	Ē	E COMON I/O		83	90
tPZL	E	COMON I/O	MAX	83	90
tрzн	Sn		1447	90	90
tPZL	Sn	COMON I/O	MAX	90	90
tPHZ	Ē	COMON I/O	MANY	83	83
tPLZ	E	COMON I/O	MAX	83	83
tPHZ	0-	001401110	1447	87	87
tPLZ	Sn	COMON I/O	MAX	87	87

# 4067

# TRIPLE 3-INPUT OR GATES

 $\bullet$  Y = A + B + C





STATEMENT PARAGE SAMPLE

NO ASSESSMENT AND PROPERTY OF THE

loves i right = 1

	INPUTS	5	OUTPUT
Α	В	С	Y
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

NOTES:
H = High Voltage Level
L = Low Voltage Level
X = Don't Care

RECOMMENDE	DUPERATING	CUNDI	HUNS		
PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
Icc	MAX	0.02	0.04	0.04	mA
Іон	MAX	-4	-4	-4	mA
lou	MAX	4	4	4	mA

## SWITCHING CHARACTERISTICS

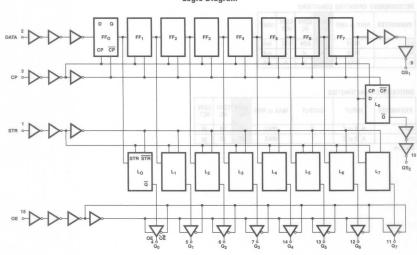
PARAMETER	INPUT	оитрит	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
tPLH	A, B or C	Y	MAX	25	30	36
tPHL	A, B or C	Y	MAX	25	30	36

UNIT:ns

515



Logic Diagram



	INP	UTS		PALALLEL		SERIAL	
CP	OE	STR	D	Qo	Qn	QS <sub>1</sub> ‡	QS2
Ť	L	X	X	Z	Z	Q'6	NC
1	L	X	X	Z	Z	NC	Q'7
1	Н	L	X	NC	NC	Q'6	NC
1	H	Н	L	L	Qn-1	Q'6	NC
1	Н	Н	Н	Н	Qn-1	Q'6	NC
1	Н	Н	Н	NC	NC	NC	Q'7

NOTES:

1. H = High Voltage Level, L = Low Voltage Level, X = Don't Care, NC = No charge, Z = High Impedance Off-state, T = Transition from Low to High Level, L = Transition from High Level, L = Transition from High Low.

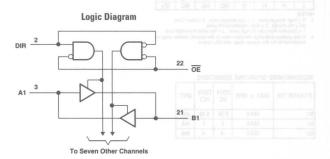
2. At the positive clock edge the information in the seventh resister stage is transferred to the Bith register stage and Sq. output.

# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
Icc	MAX	0.16	0.16	mA
lou	MAX	4	4	mA
Іон	MAX	-4	-4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
tw	(	CP CP	MIN	24	24
twn	S	TR	MIN	24	24
tsu	D	ata	MIN	15	15
	S	TR	MIN	30	30
tH	D	ata	MIN	3	4
	S	TR	MIN	0	0
tPLH	0.0	004		45	-
tPHL	CP	QS1	MAX	45	120
tPLH .	0.0	000		41	1-0
tPHL .	CP	QS2	MAX	41	-,
tPLH .	0.0			59	-
tPHL .	CP	Qn	MAX	59	(4.0
tPLH .	ATR			54	-
tPHL .	STR	Qn	MAX	54	-
tpzH	05	0-	MAN	53	12.0
tPZL	0E	Qn	MAX	53	(*)
tPLZ	OF.	0-	MANY	38	-
tPHZ	0E	Qn	MAX	38	-



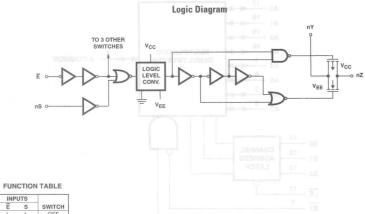
INP	UTS	
OE	DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC	LVCC	UNIT
ICCA	MAX	0.08	0.08	mA
Іссв	MAX	0.05	0.08	mA
Іон	MAX	-24	-24	mA
lou	MAX	24	24	mA

# SWITCHING CHARACTERISTICS

MAX or MIN	LVC	V <sub>CCB</sub> 3.3V
MAY	6.3	7
MAX	6.7	7
MAN	6.1	6.2
MAX	5	5.3
MAN	9	9
IVIAX	8.1	8
MAN	8.8	10
MAX	9.8	10.2
MAN	7	5.2
MAX	5.8	5.2
MAN	7.7	5.4
MAX	7.8	7.4
	MAX or MIN  MAX  MAX  MAX  MAX  MAX  MAX	MAX 6.3 6.7 6.1 5 MAX 9.8 1 MAX 9.8 MAX 7.5 8 MAX 7.7



INP	UTS	
Ē	S	SWITCH
L	L	OFF
L	H	ON
H	×	OFF

# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
Icc	MAX	0.16	0.16	mA

# SWITCHING CHARACTERISTICS

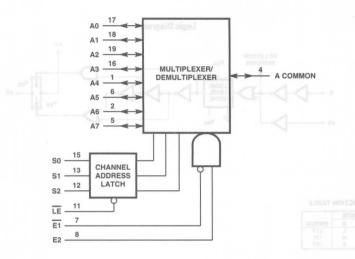
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
tPLH	Switch in	Cuitab aut	MAX	18	18
tPHL .	Switch in	Switch out	IVIAX	18	18
tPZH	Ē	7100	MAX	62	66
tPZL	E	2	MAX	62	85
tPZH	-0	7 1/11/1	MAN	53	60
tPZL	nS	2	MAX	53	75
tPLZ	Ē	ZXAM	MAX	62	75
tPHZ	E		IVIAX	62	-
tPLZ	1277	XAM	MAX	53	11 13
tPHZ	nS	Z	IVIAX	53	66
UNIT:ns	77.0	1AM	25V		3.0

75 75	53 53	MAX	ZIIIM		nS
		IVIAA			
75					
	62	MAX	ZXAM		Ē
- 0	62	MAX	2		E
U.S.	53	gaV	XAM		2017
66	53	MAX	Z		nS
n2		2:5V	10,0,00	- 0	77.
_		53	MAX 53	200 200 200 200 200 200 200 200 200 200	

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters. See www.ti.com/sc/logic for the most current data sheets.

# ANALOG MULTIPLEXERS/DEMULTIPLEXERS WITH LATCH 3/31 HTM H3TIM2 30 JAMA BAUD

# Logic Diagram



**FUNCTION TABLE** 

		INPUTS	3		"ON"†
E1	E2	S2	S1	SO	SWITCCHES LE = H
L	Н	L	L	L	A <sub>0</sub>
L	Н	L	L	Н	A <sub>1</sub>
L	Н	L	Н	L	A <sub>2</sub>
L	Н	L	H	Н	A <sub>3</sub>
L	н	Н	L	L	A <sub>4</sub>
L	Н	Н	L	Н	A <sub>5</sub>
L	Н	Н	Н	L	A <sub>6</sub>
L	Н	Н	Н	Н	A <sub>7</sub>
Н	L	X	X	X	None

NOTES:

† When LE is low S0-S2 data are latched and switches cannot change state
H = High Voltage Level, L = Low Voltage Level, X = Don't Care

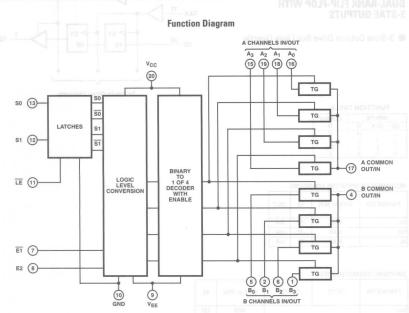
# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
Icc	MAX	0.16	0.16	mA

# SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
tw	ī	E- XAM	MIN	30	28
tsu	Sn t	o LE	MIN	-	
tH	Sn t	to LE	MIN	5	5
tPLH	Switch In	Switch Out	MAX	-11	11
tPHL .	SWITCH III	Switch out	IVIAA	11	11
tPZH	E1, E2, LE	Vos	MAX	90	113
tPZL	E1, EZ, LE	Vos	MAX	90	113
tPZH	Sn	Vos	MAX	90	113
tPZL	Sn	VOS	IVIAX	90	113
tPLZ	E1	Vos	MAX	75	83
tPHZ	EI	VOS	WAX	75	83
tPLZ	E2	Vos	MAX	75	90
tPHZ	EZ	VUS	IVIAX	75	90
tPLZ	LE	Vos	MAX	83	90
tPHZ	LE	VUS	IVIAX	83	90
tPLH .	Sn	Vos	MAN	83	98
tPHL	эП	VOS	MAX	83	98

# ANALOG MULTIPLEXERS/DEMULTIPLEXERS WITH LATCH



# **FUNCTION TABLE**

	INP	UTS		"ON"†
<u>E1</u>	E2	S1	SO	SWITCCHES
L	Н	L	L	A <sub>0</sub> , B <sub>0</sub>
L	Н	L	Н	A <sub>1</sub> , B <sub>1</sub>
L	Н	H	L	A2, B2
L	Н	H	Н	A <sub>3</sub> , B <sub>3</sub>
Н	L	X	X	None

NOTES:

† When LE is low S0-S2 data are latched and switches cannot change state.

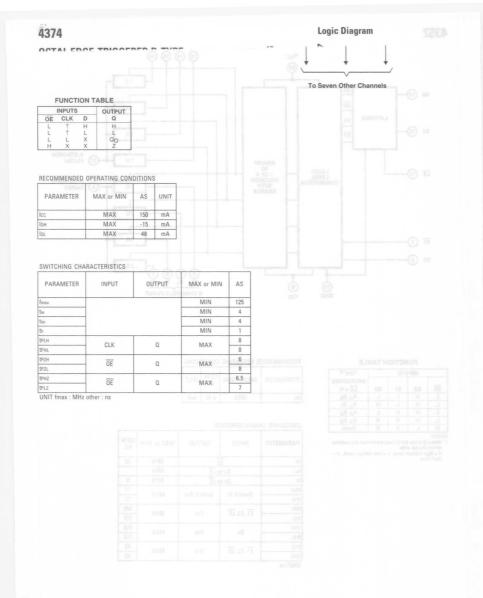
H = High Voltage Level, L = Low Voltage Level, X = Don't Care

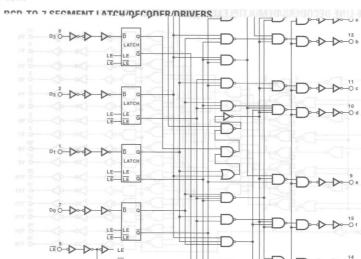
# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
lcc	MAX	0.16	mA

# SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
tw	ī	.E	MIN	30
tsu	Sn t	to LE	MIN	-
th	Sn t	to LE	MIN	5
tPLH	Switch In	Switch Out	MAX	11
tphl.	Switch in	Switch Out	IVIAX	11
tРZH	E1, E2, LE	Vos	MAX	105
tPZL	E1, E2, LE	Vos	MAX	105
tРZH	0		MAX	113
tPZL	Sn	Vos	MAX	113
tPLZ	E1, E2, LE	Man	- NAMA	83
tPHZ	E1, EZ, LE	Vos	MAX	83





LE	Bt	LT	D <sub>3</sub>	$D_2$	D <sub>1</sub>	D <sub>0</sub>	а	b	С	d	е	f	g	Display
X	X	L	X	X	X	X	Н	Н	Н	Н	Н	Н	Н	8
X	L	Н	X	X	X	X	L	L	L	L	L	L	L	Blank
L	Н	Н	L	L	L	L	Н	Н	H	Н	H	Н	L	0
L	Н	Н	L	L	L	H	L	H	H	L	L	L	L	1
L	Н	Н	L	L	H	L	Н	H	L	H	H	H	L	2
L	H	Н	L	L	Н	Н	Н	H	H	H	L	L	H	3
L	Н	Н	L	H	L	L	L	H	H	L	L	H	H	4
L	Н	H	L	H	L	Н	H	L	H	H	L	H	H	5
L	Н	Н	L	H	Н	L	L	L	H	H	H	Н	H	6
L	H	H	L	Н	H	H	Н	Н	H	L	L	L	L	7 8
L	H	Н	H	L	L	L	Н	H	H	H	H	Н	H	8
L	H	Н	H	L	L	H	Н	H	H	L	L	H	H	9
L	H	Н	H	L	H	L	L	L	L	L	L	L	L	Blank
L	H	Н	Н	L	H	Н	L	L	L	L	L	L	L	Blank
L	Н	H	H	Н	L	L	L	L	L	L	L	L	L	Blank
L	Н	Н	Н	H	L	н	L	L	L	L	L	L	L	Blank
L	Н	Н	Н	Н	H	L	L	L	L	L	L	L	L	Blank
L	H	Н	Н	H	H	Н	L	L	L	L	L	L	L	Blank
H	H	Н	X	X	X	X								

NOTES: X = Don't Care

Depends on BCD code previously appied when LE = L Display is blank for all illegal input codes (BCD > HLLH).

# RECOMMENDED OPERATING CONDITIONS

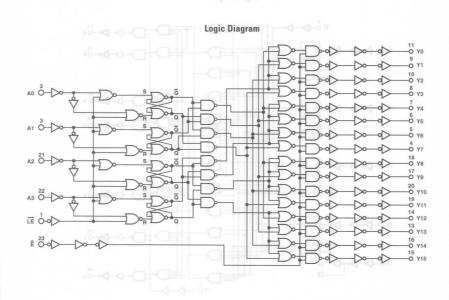
PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
Icc	MAX	0.16	0.16	mA
Іон	MAX	-7.4	-7.4	mA
lou	MAX	4	4	mA

# SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
tw	Latch	Enable	MIN	20	20
tsu	Dn	to LE	MIN	20	20
th	Dn	to LE	MIN	3	5
tPLH	Dn		MAX	75	75
tPHL:	Un	a to g	MAX	75	75
tPLH	TE		MAN	68	68
tphL .	LE	a to g	MAX	68	68
tPLH	BI		MAN	55	55
tPHL .	BI	a to g	MAX	55	55
tPLH	ĪŢ		MANY	40	41
tPHL	LI	a to g	MAX	40	41

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# 4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS WITH INPUT LATCHES THRIMBRE V-01-038





FUNCTION TABLE (LE = H)

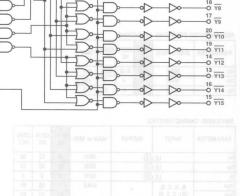
				(LE = H)	
_	D	ECODE	R INPUT	S	ADDRESSED OUTPUT H
Ē	A3	A2	A1	A0	ADDRESSED OUTFUL H
L	L	L	L	L	Y0
L	L	L	L	Н	Y1
L	L	L	H	E.	Y2
L	L	L	Н	Н	Y3
L	L	Н	L	L	Y4
L	L	Н	L	н	Y5
L	L	Н	H	L	Y6
L I	L	Н	Н	н	Y7
L	Н	L	L	L	Y8
L	Н	1	L	1. H.	Y9
L o	Н	L	Н	L	Y10
L	Н	L	H	H	Y11_
57 6		Н	L	L	Y12
L	Н	H	L	н	Y13
L	Н	H	H	L	Y14
L.	Н	Н	Н	H	Y15
Н	X	X	Х	X	All outputs = L

H = high, L = low, X = don't care

# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
Icc	MAX	0.08	0.16	0.08	mA
Іон	MAX	-4	-4	-6	mA
lou	MAX	4	4	6	mA

SWITCHING CH	HARACTERISTIC	S				
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
tw	LE (LE)		MIN	20	22	38
tsu	LE (LE)		MIN	25	30	25
th	LE (LE)		MIN	5	0	5
tPLH	A, B, C, D (A1, 2, 3, 4)	V	MAX	58	83	69
tPHL .		,		58	83	69
tPLH	LE (LE)	Y	MAX	58	68	63
tPHL				58	68	63
tPLH	G (E)	γ	MAX	44	53	50
tPHL .	(E)	Y		44	53	50



				(	
_	E DECODER INPUTS  A3 A2 A1 A0		DECODER INPUTS		
E			ADDRESSED OUTPUT L		
L	L	L	L	L	YO
L	L	L	L	Н	Y1
L	L	L	Н	L	Y2
L	L	L	Н	н	Y3
L	L	Н	L	L	Y4
L	L	Н	L	Н	Y5
L	L	H	Н	L	Y6
L	L	Н	H	н	Y7
L	Н	L	L	L	Y8
L	Н	L	L	Н	Y9
L	Н	L	H	L	Y10
L	Н	L	H	н	Y11
L	Н	H	L	L	Y12
L	н	Н	L	н	Y13
L	н	Н	Н	E	Y14
L	Н	Н	Н	H	Y15
Н	X	Х	х	X	All outputs = H

H = high, L = low, X = don't care

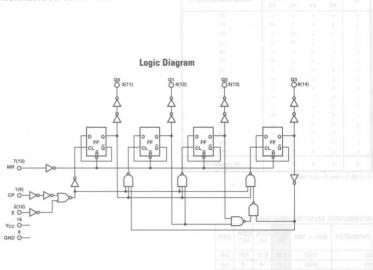
# RECOMMENDED OPERATING CONDITIONS

THE COMMITTEE OF EMPTH OF CONTENTIONS							
PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT		
Icc	MAX	0.08	0.16	0.08	mA		
Іон	MAX	-4	-4	-6	mA		
In	MAX	4	4	6	mA		

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
tw	LE	(LE)	MIN	20	22	38
tsu	LE (LE)		MIN	25	30	25
th	LE (LE)		MIN	5	0	5
tPLH	A, B, C, D	Y	MAX	58	83	69
tphL .	(A1, 2, 3, 4)	(CD74HCT:Y)		58	83	69
tPLH .	LE	Ÿ	MAN	58	68	63
tphl.	(LE)	(CD74HCT:Y)	MAX	58	68	63
tPLH	G (E)	Ÿ	MANY	44	53	50
tPHL .	(Ē)	(CD74HCT:Y)	MAX	44	53	50

# **DUAL SYNCHRONOUS COUNTERS**



# **FUNCTION TABLE**

	NPUT	S	
CP	E	MR	OUTPUT STATE
Ť	Н	L	Increment Counter
L	1	L	Increment Counter
1	X	L	No Change
H	1	L	No Change
1	L	L	No Change
H	1	L	No Change
L	X	Н	$Q_0$ thru $Q_3 = L$

## RECOMMENDED OPERATING CONDITIONS

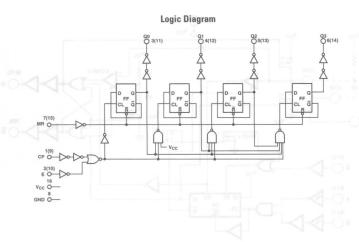
PARAMETER	MAX or MIN	CD74 HC	UNIT
Icc	MAX	0.16	mA
Іон	MAX	-4	mA
lou	MAX	4	mA

# SWITCHING CHARACTERISTICS

SWITCHING CH.	ARACTERISTI	US		
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
fmax			MIN	20
tw	MIN	24		
	N	ИR	1 IVIIIV	30
tsu	Enabl	e to CP	MIN	24
	CP to	Enable	IVIIN	24
tPLH	on.	0-	MAX	72
tphL .	CP	Qn	MAX	72
tPLH	F	0-	MAN	72
tphL .	Enable Qn		MAX	72
tPLH			MAN	45
tphL .	MH	Un	MAX	45
HL	MR	Qn	MAX	4

UNIT fmax: MHz other: ns

# DUAL SYNCHRONOUS COUNTERS WITHUM ALBARA DIROM MODERNAM ALBARADORTER LAUG



# **FUNCTION TABLE**

	S	NPUTS	1
<b>OUTPUT STATE</b>	MR	E	CP
Increment Counter	L	Н	1
Increment Counter	L	4	L
No Change	L	X	1
No Change	L	†	X
No Change	L	L	1
No Change	L	1	H
$Q_0$ thru $Q_3 = L$	H	X	X

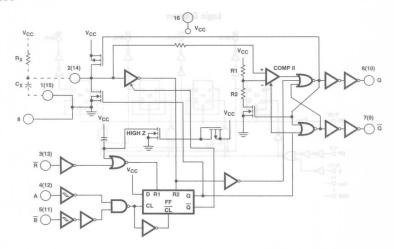
# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
Icc	MAX	0.16	0.16	mA
Юн	MAX	-4	-4	mA
lou	MAX	4	4	mA

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
fmax		MIN	20	17	
tw	CP		MIN	24	30
	MR		IVIIIV	30	30
tsu	Enable to CP		MIN	24	24
	CP to Enable		MIIN	24	(*)
tPLH	CP Qn		MAX	72	80
tPHL .			MAX	72	80
tPLH	Enable Qn		MANY	72	83
tрнL			MAX	72	83
tPLH	MD	0-	MAN	45	53
tPHL	- MR Qn		MAX	45	53

UNIT fmax: MHz other: ns



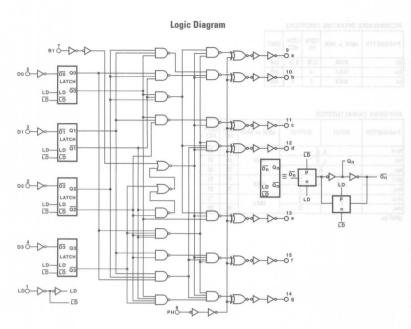
# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
Icc	MAX	0.16	0.16	mA
Іон	MAX	-4	-4	mA
lou	MAX	4	4	mA

# SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
WH A, B		-	10-0-0	24	24
twL	A, B		MIN	24	24
twL		R	80 Kg	24	30
tPLH	A, B	0	MAX	75	83
tPHL	А, В	ā	MAX	75	83
tPLH	R	ā	MANY	-	75
tPHL	ri	Q	MAX	75	60





LD	B1	PH	D3	D2	D1	D0	а	b	С	d	е	f	g	Display
X	Н	L	X	X	X	X	L	L	L	L	L	L	L	Blank
Н	L	L	L	L	L	L	H	H	Н	Н	H	H	L	0
Н	L	L	L	L	L	Н	L	Н	H	L	L	L	L	1
Н	L	L	L	L	H	L	H	Н	L	H	H	L	H	2
Н	L	L	L	L	Н	Н	Н	Н	H	H	L	L	H	3
Н	L	1	L	Н	L	L	L	Н	Н	L	L	H	Н	4
Н	L	L	L	H	L	H	Н	L	Н	Н	L	Н	H	5
Н	L	L	L	Н	Н	L	H	L	Н	Н	Н	H	H	6
H	L	L	L	Н	Н	Н	Н	Н	H	L	L	L	L	7
Н	L	L	Н	L	L	L	Н	Н	H	H	H	H	H	8
н	L	Lon	H	L.	L	H	H	Н	H	H	L	Н	H	9
Н	L	L	H	L	Н	L	L	L	L	L	L	L	L	Blank
Н	L	L	H	L	Н	H	L	L	L	L	L	L	L	Blank
Н	L	L	H	H	L	L	L	L	L	L	L	L	L	Blank
Н	L	L	H	Н	L	Н	L	L	L	L	L	L	L	Blank
Н	L	L	H	Н	Н	L	L	L	L	L	L	L	L	Blank
Н	L	L	H	Н	Н	Н	L	L	L	L	L	L	L	Blank
L	L	L	X	X	X	X								
as a	bove	N		as a	bove	9			inve	rse a	bove	9	inverse above	

Depends open the BCD code previously appled when LE = High

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
Icc	MAX	0.16	0.16	mA
Іон	MAX	10-1	-1	mA
lou	MAX	1	1	mA

# SWITCHING CHARACTERISTICS

OTTITO OII	ANAUTEMOT	00			
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
tw	Latch	Disable	MIN	13	13
tsu	Dn	to LD	MIN	15	15
th	Dn	to LD	MIN	8	10
tPLH	D-	/3.70	MAN	85	100
tphL .	Dn	a to g	MAX	85	100
tPLH	1.0		MANY	93	96
tphl .	LD	a to g	MAX	93	96
tPLH .	B1	020	MAX	66	83
tphl.	ВІ	a to g	MAX	66	83
tPLH	DII		MAN	50	83
tPHL .	PH	a to g	MAX	50	83

Output Ports Have Equivalent 25-Q Series Resistors

# Logic Diagram

## FUNCTION TABLE

INPUTS			INPUT	
OE1	OE2	D	Y	
L	L	L	L	
L	L	H	H	
H	X	X	Z	
X	H	X	Z	

# To Ten Other Channels

# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
Icc	MAX	45	mA
Іон	MAX	-12	mA
lou	MAX	12	mA

# SWITCHING CHARACTERISTICS

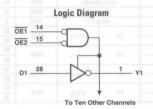
PARAMETER	INPUT	ОИТРИТ	MAX or MIN	ABT
tPLH		Y	AAAV V	6.2
tphl.	D	4-00	MAX	5.6
tPZH	ŌĒ	v	MAN	8.7
tPZL	UE	Y	MAX	7.5
tРHZ	ŌĒ	.,		5.2
tPLZ	ÜE	Y	MAX	6.9

## UNIT: ns

# 5401

# 11-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

 Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABT5401)



# **FUNCTION TABLE**

	INPUTS	UTS OUT			
OE1	OE2	D	Y		
L	L	L	Н		
L	L	H	L		
Н	X	X	Z		
X	H	X	Z		

# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
Icc	MAX	45	mA
Іон	MAX	-12	mA
lou	MAX	12	mA

# SWITCHING CHARACTERISTICS

OVVITORINVO OTIALI	TO TEINOTIOO			
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
tplH	D	- v	MAX	6.9
tPHL .	υ .	T	IVIAX	5.7
tpzh	ŌE	Υ	MAX	8.5
tPZL	UE	Y.	MAX	6.8
tPHZ	ŌE	v	MANY	5.2
tPLZ	OE		MAX	6.9

5402

(SN74ABT5402A)

Logic Diagram

To Eleven Other Channels

# **FUNCTION TABLE**

INPUTS		OUTPUT	
OE1	OE2	D	Υ
L	L	L	L
L	L	H	H
H	X	X	Z
×	H	X	Z

# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
Icc	MAX	48	mA
Іон	MAX	-12	mA
lou	MAX	12	mA

## SWITCHING CHARACTERISTICS

SWITCHING CHAN	ACTENISTICS			_
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
tPLH	D.	V		6.2
tPHL .	OH DUNE TO 3	HAME Y TUSTO	IVIAA	5.6
tPZH	Œ Œ	V	MAX	8.7
tPZL		1 1	MAA	7.5
tPHZ	<u> </u>	ŌE Y	MANY	5.2
tPLZ	ÜE	1	MAX	6.9

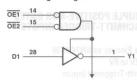
UNIT: ns

# 5403

# 11-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

Output Ports Have Equivalent 25-Ω Series
Resistors, So No External Resistors Are Required
(SN74ABT5403)

# **Logic Diagram**



To 11 Other Channels

# **FUNCTION TABLE**

	INPUTS OU		OUTPUT
OE1	OE2	D	Y
L	L	L	Н
L	L	Н	L
H	X	X	Z
X	H	X	Z

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
Icc	MAX	45	mA
Іон	MAX	-12	mA
lou	MAX	12	mA

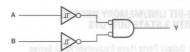
### SWITCHING CHARACTERISTIC

SWITCHING CHAP	RACTERISTICS			_
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
tPLH	Dilling and a	MM Y YUSTU	444V	6.9
tphl.				5.7
tPZH	OE XAM	Y	MAX	8.5
tPZL				6.8
tPHZ	ŌE	Υ	MAX	5.2
tPLZ				6.9

# 7001

# QUADRUPLE POSITIVE-AND GATES WITH SCHMITT-TRIGGER INPUTS

- Same Pinouts as SN74HC08
- V<sub>CC</sub>: 2V to 6V
- Schmitt-Triggered Inputs
- Y = A•B



Logic Diagram

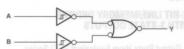
# RECOMMENDED OPERATING CONDITIONS

TIEGOTATIVIETADED	OF ENATING CON	T	
PARAMETER	MAX or MIN	нс	UNIT
Icc	MAX	0.02	mA
Іон	MAX	-4	mA
lou	MAX	4	mA

# SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	нс
tPLH	KAA		MAY 30	33
tPHL	A or B	Y	MAX	33

# Logic Diagram



# 7002

# QUADRUPLE POSITIVE-NOR GATES WITH SCHMITT-TRIGGER INPUTS

- Same Pinouts as SN74HC36
- V<sub>CC</sub>: 2V to 6V
- Schmitt-Triggered Inputs
- $\bullet$  Y =  $\overline{A}$  +  $\overline{B}$

## RECOMMENDED OPERATING CONDITIONS

NECOMMENDED	OF ENATING CON	T	1
PARAMETER	MAX or MIN	нс	UNIT
Icc	MAX	0.02	mA
Іон	MAX	-4	mA
lou	MAX	4	mA

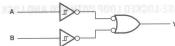
### SWITCHING CHARACTERISTICS

ACTENISTICS	_		_
INPUT	OUTPUT	MAX or MIN	нс
A D	V	MAY	33
AOIB	Y	MAX	33
	A Louis	INPUT OUTPUT	INPUT OUTPUT MAX or MIN

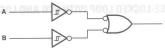
# 536

# **Logic Diagram**

# QUADRUPLE 2-INPUT POSITIVE-OR GATES (1910) WITH SCHMITT-TRIGGER INPUTS



- Same Pinouts as SN74HC32
- V<sub>CC</sub>: 2V to 6V
- Schmitt-Triggered Inputs
- Y = A + B



### RECOMMENDED OPERATING CONDITIONS

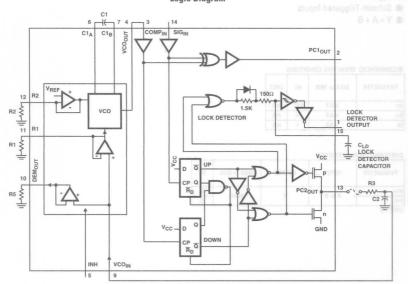
PARAMETER	MAX or MIN	нс	UNIT
Icc	MAX	0.02	mA
Іон	MAX	-4	mA
lor And	MAX	4	mA

# SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	нс
tPLH	A == D	V PC	MAX	33
tPHL TPHL	A or B	Υ	WAX	33



# **Logic Diagram**



# RECOMMENDED OPERATING CONDITIONS

RECOMMENDE	U UPERATING	CUNDI	LIUNS	
PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
lcc	MAX	0.16	0.16	mA
Іон	MAX	-4	-4	mA
lou	MAX	4	4	mA

# SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
tPLH .	SIGIN,	001	MAY	60	68
tPHL	COMPIN	PC1 out	MAX	60	68
tРZH	SIGIN,	000	MAX	84	90
tPZL	COMPIN	PC2out	MAX	84	90
tPHZ	SIGIN,	РС2оит	MAX	98	105
tPLZ	COMPIN	FUZOUT	IVIAX	98	105

Г	INP	UTS	OUTPUT
	Α	В	Y
	L	L	Н
	L	H	L 278
	H	L	L
	H	Н	H

NOTES: H = High Voltage Level L = Low Voltage Level

### RECOMMENDED OPERATING CONDITIONS

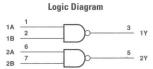
PARAMETER	MAX or MIN	SN74 HC	CD74 HC	UNIT
Icc	MAX	0.02	0.04	mA
Іон	MAX	-4	-4	V
lou	MAX	4	4	V

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC
tPLH	A D	Y	MAX	25	35
tPHL .	A or B	Y	MAX	25	35

# 8003

# **DUAL 2-INPUT POSITIVE-NAND GATES**



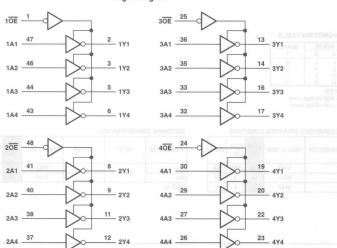
RECOMMENDED OPERATING CONDITIONS

necommended of environe contaminate						
PARAMETER	MAX or MIN	ALS	AS	UNIT		
Icc	MAX	1.5	8.7	mA		
Іон	MAX	-0.4	-2	mA		
lou	MAX	8	20	mA		

SWITCHING CHAR	ACTERISTICS				_
PARAMETER	INPUT	ОИТРИТ	MAX or MIN	ALS	AS
tPLH .	A or B	v	MAX	11	4.5
tphl.	A OF B	1	WAX	8	4

# 16-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS AND ROM-ENGLISMS TUSINES GAMB

# Logic Diagram





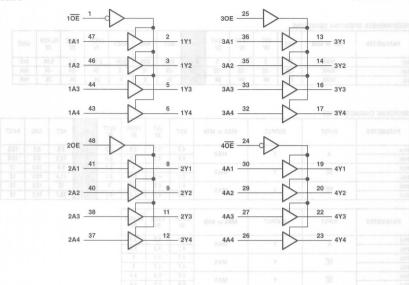
INP	JTS	OUTPUT
OE	Α	Y
L	Н	L
L	L	H
H	X	7

# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVT 3V	LVTH 3V	ALVT 3V	AC	ACT	AHC	AHCT	LVCH 3V	LVCZ 3V	ALVCH 3V	UNIT
Icc	MAX	34	5	5	5	0.08	0.08	0.04	0.04	0.02	0.1	0.04	mA
Іон	MAX	-32	-32	-32	-32	-24	-24	-8	-8	-24	-24	-24	mA
lou	MAX	64	64	64	64	24	24	8	8	24	24	24	mA

SWITCHING CHARA	CIEMISTICS		1740								
PARAMETER	INPUT	ОИТРИТ	MAX or MIN	ABT	LVT 3V	LVTH 3V	ALVT 3V	AC	ACT	AHC	AHCT
tPLH .		V .	MAX	4.7	3.5	3.5	3.3	5.8	8.5	8.5	10.5
tPHL .	A	1	WAX	4.8	3.5	3.5	3.2	7.1	10.2	8.5	10.5
tPZH	<del>OE</del>	V	- May	5.3	4	4	3.7	6.6	9.4	10.5	13
tPZL	UE		MAX	7.1	4.4	4.4	3.1	8.1	11.4	10.5	13
tPHZ	OE OE	V	S MAY	6.1	4.5	4.5	5	8.1	12	10.5	13
tPLZ	TAN OF	< Y	MAX	5.6	4.2	4.2	4.1	7.3	10.7	10.5	13

INPUT	OUTPUT	MAX or MIN	LVCH 3V	LVCZ 3V	ALVCH 3V	
5Y5 - 500	V	1 May	4.2	4.2	3.9	
A	1	MAX	4.2	4.2	3.9	
<u> </u>		1444	4.7	4.7	5	
UE	Y	MAX	4.7	4.7	5	
ŌĒ	V	MAN	5.9	5.9	4.4	
UE	Y	WAX	5.9	5.9	4.4	
	INPUT	A Y 0E Y	NPUT	A	A Y MAX 0 MIN 3V 3V  A Y MAX 4.2 4.2  OE Y MAX 4.7 4.7  OF V MAX 5.9 5.9	A Y MAX 4.2 4.2 3.9  \[ \begin{array}{cccccccccccccccccccccccccccccccccccc



INPU"	rs	OUTPUTS
10E, 40E	1A, 4A	1Y, 4Y
L	Н	L
L	L	Н
H	X	Z

INPU"	OUTPUTS				
20E, 30E	2A, 3A	2Y, 3Y			
Н	Н	H			
Н	L	L			
L	X	Z			



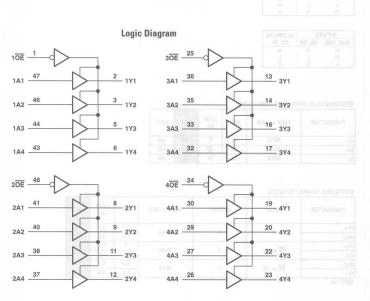


PARAMETER	MAX or MIN	ABT	LVTH 3V	ACT	UNIT
Icc	MAX	34	5	0.08	mA
Гон	MAX	-32	-32	-24	mA
lou	MAX	64	64	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	ACT	
tPLH .	05	v	S COMMAN	3.7	3.5	9.5	
tPHL .	SYA A		MAX	4.5	3.5	9.1	
tPZH	OE or OE	V	MAX	5	4.5	9.4	
tPZL .	UE OF UE	T	MAX	6.9	4.5	10.5	
PHZ	OE or OE	V	MAN	6.2	5.3	11.6	
tPLZ	UE OF UE	T .	MAX	5.6	4.9	10.7	

# 16-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



INPL	JTS	OUTPUT
ŌĒ	Α	Y
L	Н	Н
L	L	L
H	X	Z

RECOMMENDED OPERATING CONDITIONS

NECOMMENDED OF	PENATING CUNDITI	UNS											
PARAMETER	MAX or MIN	ABT	ABTH	LVT 3V	LVTH 3V	ALVTH 3V	AC	ACT	AHC	AHCT	TAC 3A	LVCH 3V	UNIT
Icc	MAX	32	32	- 5	5	5	0.08	0.08	0.04	0.04	0.02	0.02	mA
Юн 85	MAX	-32	-32	-32	-32	-32	-24	-24	-8	-8	-24	-24	mA
lou	MAX	64	64	64	64	64	24	24	8	8	24	24	mA

PARAMETER	MAX or MIN	LVCZ 3V	ALVC 3V	ALVCH 3V	AVC 3V	UNIT
Icc	MAX	0.1	0.04	0.04	0.04	mA
Он	MAX	-24	-24	-24	-12	mA
lor	MAX	24	24	24	12	mA

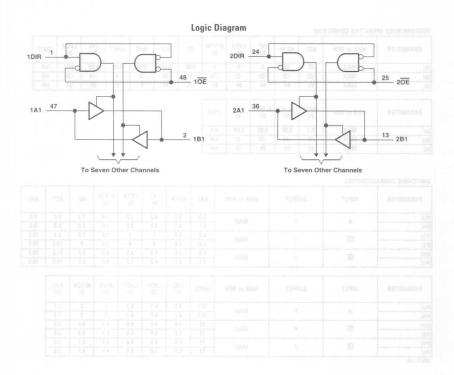
SWITCHING CHARAC	CTERISTICS										
PARAMETER	INPUT	ОИТРИТ	MAX or MIN	ABT	АВТН	LVT 3V	LVTH 3V	ALVTH 3V	AC	ACT	AHC
tPLH	A	v	MAX	3.5	3.5	3.2	3.2	2.4	7.1	9.4	8.5
tPHL	A	1		4.1	4.1	3.2	3.2	2.5	7.9	9.5	8.5
tPZH	ŌĒ			4.8	4.8	4	4	3.8	7.5	8.9	10.5
tPZL	UE	Y	MAX	4.8	4.8	4	4	2.9	9	10.3	10.5
tPHZ	ŌĒ	V	MAN	4.8	4.8	4.5	4.5	4.2	8.4	11.3	10.5
tPLZ	UE	T	MAX	4.1	4.1	4.2	4.2	3.6	7.6	10.3	10.5

PARAMETER	INPUT	ОИТРИТ	MAX or MIN	AHCT	TAC 3A	LVCH	LVCZ 3V	ALVC 3V	ALVCH 3V	AVC 3V
tPLH	Α.	v	MAX	10.5	4.1	4.1	4.1	3	3	1.7
tPHL .	A	т .	IVIAA	10.5	4.1	4.1	4.1	3	3	1.7
tPZH	ŌĒ	v	MAN	13	4.6	4.6	4.6	4.4	4.4	3.5
tPZL	UE	т т	MAX	13	4.6	4.6	4.6	4.4	4.4	3.5
PHZ.	ŌĒ	Y	MAN	13	5.8	5.8	5.8	4.1	4.1	3.5
tPLZ	UE		MAX	13	5.8	5.8	5.8	4.1	4.1	3.5

# 16245

# 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS





### RECOMMENDED OPERATING CONDITIONS

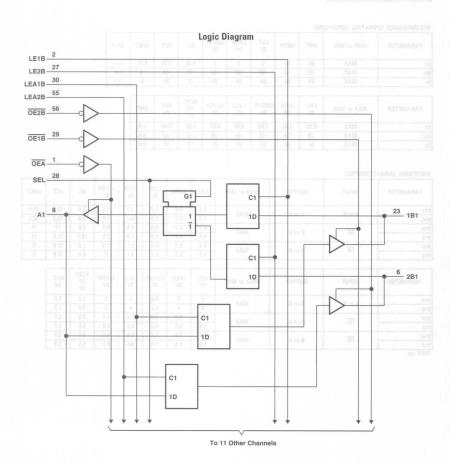
PARAMETER	MAX or MIN	ABT	АВТН	LVT 3V	LVTH 3V	ALVTH 3V	AC	ACT	AHCT	UNIT
Icc	MAX	32	32	5	5	5	0.08	0.08	0.04	mA
Іон	MAX	-32	-32	-32	-32	-32	-24	-24	-8	mA
lou	MAX	64	64	64	64	64	24	24	8	mA

PARAMETER	MAX or MIN	TAC 3A	LVCH 3V	LVCHR 3V	LVCZ 3V	ALVCH 3V	ALVC HR 3V	AVC 3V	UNIT
Icc	MAX	0.02	0.02	0.02	0.06	0.04	0.04	0.04	mA
Іон	MAX	-24	-24	-12	-24	-24	-12	-12	mA
lou	MAX	24	24	12	24	24	12	12	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ABTH	LVT 3V	LVTH 3V	ALVTH 3V	AC	ACT	AHCT
tPLH PS			G:MAX -	3.9	3.9	3.3	3.3	3.1	7.9	10.5	10.5
tPHL	A or B	B or A		4.2	4.2	3.3	3.3	2.9	8.9	10.2	10.5
tPZH	ŌE	B or A	MAX	6.3	6.3	4.5	4.5	4.2	8.6	10	15
tPZL	OE.			6.4	6.4	4.6	4.6	3.5	10.7	11.6	15
tPHZ	ŌĒ			6.3	6.3	5.1	5.1	5.3	9.8	12.6	15
tPLZ	OF.			5.2	5.2	5.1	5.1	5	8.7	11.8	15

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 3V	LVCH 3V	LVCHR 3V	LVCZ 3V	ALVCH 3V	ALVC HR 3V	AVC 3V
tPLH .	A D	D A	MAX	4	4	4.8	4	3	4.2	1.7
tPHL	A or B	B or A	MAX	4	4	4.8	4	3	4.2	1.7
tPZH	ŌĒ	B or A	MAX	5.5	5.5	6.3	5.6	4.4	5.6	3.7
tPZL	UE	B or A	MAX	5.5	5.5	6.3	5.6	4.4	5.6	3.7
tphz	ŌĒ	D A	MANY	6.6	6.6	7.4	6.6	4.1	5.5	3.9
tPLZ	0E	B or A	MAX	6.6	6.6	7.4	6.6	4.1	5.5	3.9



**FUNCTION TABLE** 

B TO A (OEB = H)

		DI	MIOL	.0 - 11)		
		INP	UTS	(5)		OUTPUT
1B	2B	SEL	LE1B	LE2B	OEA	A
Н	X	Н	Н	X	L	H
L	X	Н	H	X	L	L
X	X	H	L	X	L	A <sub>O</sub>
X	H	L	×	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	A <sub>0</sub>
X	X	X	X	X	H	Z

### A TO B (OFA = H)

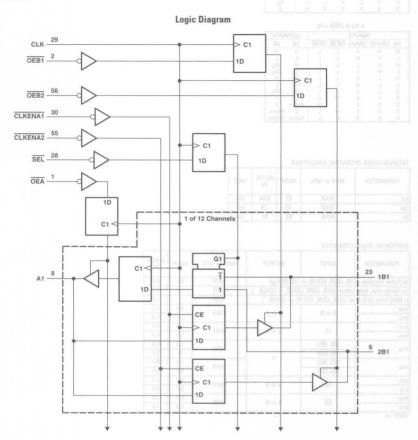
		INPUTS			OUT	PUTS
1B	LEA1B	LEA2B	OE1B	OE2B	1B	2B
Н	Н	Н	L	L	Н	Н
L	H	H	L	L	L	L
Н	H	L	L	L	H	2B <sub>0</sub>
L	H	L	L	L	L	2B <sub>0</sub>
H	L	H	L	L	1B0	H
L	L	H	L	L	1B0	L
X	L	L	L	L	1B0	2B0
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	АВТН	ALVCH 3V	UNIT
lcc	MAX	63	0.04	mA
Іон	MAX	-32	-24	mA
lou	MAX	64	24	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH	ALVCH 3V
tw Pulse duration, LE	1B, LE2B, LEA1B, or	LEA2B high	MIN	3.3	3.3
tsu Setup time, data	before LE1B, LE2B, L	EA1B, or LEA2B ↓	MIN	1.5	1.1
th Hold time, data af	ter LE1B, LE2B, LEA1	B, or LEA2B ↓	MIN	1	1.5
tPLH	A D	D A	MAX	5.6	4.3
tphL .	A or B	B or A	MAX	5.9	4.3
tPLH	15	A D	MAX	5.8	4.4
tphl.	LE	A or B	IVIAX	5.3	4.4
	SEL (B1)		1111	5.3	5.6
tPLH FSIS THE	SEL (B2)		MAX	6	5.6
	SEL (B1)	A	MAN	4.4	5.6
tPHL	SEL (B2)		MAX	5.9	5.6
tPZH	ŌĒ		MAX	5.7	5.4
tPZL	OE	A or B	MAX	5.8	5.4
tphz	ŌĒ		GI GI	6.4	4.6
tPLZ	UE	A or B	MAX	4.8	4.6



OUTDUIT SMADUS -- \-----

INPUTS				OUTI	PUTS
CLKENA1	CLKENA2	CLK	A	1B	2B
Н	Н	X	X	1Bnt	2Bot
L	×		L	L	X
L	×	*	H	H	X
×	L		L	X	L
X	L	*	Н	X	H

† Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE (OEA = L)

	INP	OUTPUT		
CLK	SEL	1B	2B	A
X	Н	X	X	Ant
X	L	X	X	Ant
-	H	H	X	Ĺ
^	H	L	X	H
*	L	X	L	L
1	L	X	H	H

† Output level before the indicated steady-str input conditions were established

RECOMMENDED OPERATING CONDITIONS

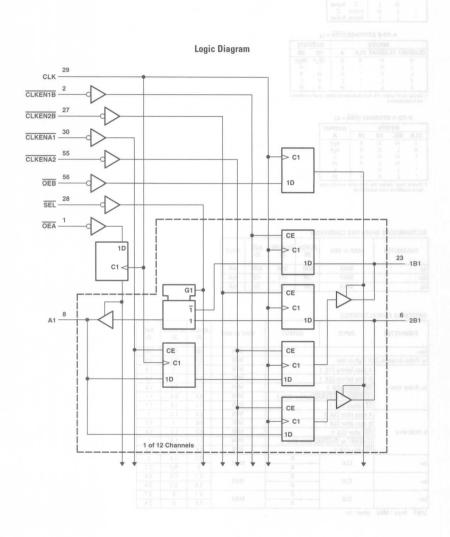
PARAMETER	MAX or MIN	ALVCH 3V	ALVCHR 3V	AVC 3V	UNIT
Icc	MAX	0.04	0.04	0.04	mA
Іон	MAX	-24	-12	-12	mA
lor	MAX	24	12	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V	ALVCHR 3V	AVC 3V
fmax		30	MIN	135	135	175
tw Pulse duration,	CLK high or low		MIN	3.3	3.3	3.5
	A data before CLK ↑	10 4	MIN	1.7	1	1.9
	B data before CLK ↑	01	MIN	1.8	1.1	1.9
tsu Setup time	SEL before CLK ↑		MIN	1.3	1.3	1.3
	CLKENA1 or CLKENA2	before CLK ↑	MIN	0.9	0.8	1.1
	OE before CLK ↑	30	MIN	1.3	1.2	1.1
	A data after CLK ↑		MIN	0.6	1.2	1
	B data after CLK ↑	10 0	MIN	0.6	1	0.7
th Hold time	SEL after CLK ↑	ar -	MIN	0.7	1.7	0.4
	CLKENA1 or CLKENA2	after CLK ↑	MIN	1.1	1.6	1
	OE after CLK ↑	Sam Sam Sam	MIN	0.8	1.2	0.3
	CLK	В	MAX	6.2	5.8	3
tpd	CER	A	IVIAA	5	5.2	2.7
	CLK	В	MAX	6.1	5.8	3.8
ten	ULK	A	IVIAX	5.9	5.3	3.4
	CLK	В	MAN	6.1	6	3.7
tdis CLK		A	MAX	5.6	- 6	3.4

UNIT fmax: MHz other: ns

# 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS



OUTPUT ENABLE

INPUTS			OUTPUTS		
CLK	OEA	OEB	A	1B,2B	
*	Н	Н	Z	Z	
1	H	L	Z	Active	
1	L	H	Active	Z	
	1	1	Activo	Activo	

A-TO-B STORAGE (OEB = L)

INPUTS				OUTI	PUTS
CLKENA1	CLKENA2	CLK	Α	1B	2B
L	H	1	L	L†	2B0‡
L	H		H	H†	2B <sub>0</sub> ‡
L	L	+	L	L†	L
L	L	7	H	H†	H
H	L	1	L	1Bo#	L
Н	L	1	H	1Bo#	H
Н	H	X	X	1B <sub>0</sub> ‡	2B <sub>0</sub> ‡

† Two CLK edges are needed to propagate data. ‡ Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE (OEA = L)

INPUTS						OUTPUT
CLKEN1B	CLKEN2B	CLK	SEL	1B	2B	A
Н	X	X	H	X	X	An‡
×	H	X	L	X	X	An‡
L	X	1	H	H	X	L
L	X	*	H	L	X	H
X	L	1		X	L	L
X	L	1	L	X	Н	H

Output level before the indicated steady-state input conditions were established

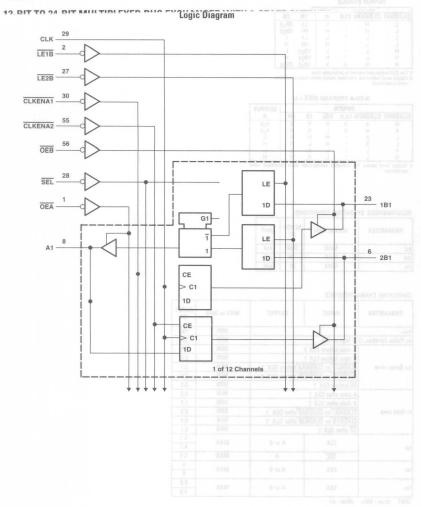
# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
Icc	MAX	0.04	mA
Іон 188	MAX	-24	mA
lou	MAX	24	mA

# SWITCHING CHARACTERISTICS

PARAMETER	INPUT	ОИТРИТ	MAX or MIN	ALVCH 3V
fmax			MIN	150
tw Pulse duration,	CLK high or low		MIN	3.3
	A data before CLK	1	MIN	3.1
	B data before CLK	<b>↑</b>	MIN	0.9
tsu Setup time	CLKENA1 or CLKEN	MIN	2.7	
	CLKEN1B or CLKEN	MIN	2.6	
	OE before CLK ↑	MIN	3.2	
	A data after CLK ↑	MIN	0.2	
	B data after CLK ↑	MIN	1.7	
th Hold time	CLKENA1 or CLKEN	NA2 after CLK ↑	MIN	0.3
	CLKEN1B or CLKEN	MIN	0.6	
	OE after CLK ↑		MIN	0.1
	CLK	A or B	MAX	5.1
tpd	CLK	AUID	IVIAA	4.7
	SEL	A	MAX	5.5
	CLK	A or B	MAX	6
ten	CLK	A OF B	WAX	6
	CIK	A D	MAN	5.8
tdis	CLK	A or B	MAX	5.8

UNIT fmax: MHz other: ns



OUTPUT ENABLE

### A-TO-B STORAGE (OEB = L)

	OUT	PUTS			
CLKENA1	CLKENA2	CLK	Α	1B	2B
Н	Н	X	X	1Bot	2Bnt
L	X	1	L	L	X
L	X	*	H	H	X
×	L	+	L	X	L
X	L		H	An	Н

### B-TO-A STORAGE (OEA = L)

	INPUTS			OUTPUTA
LE	SEL	1B	2B	
Н	X	X	X	Ant
H	X	X	X	Aot
L	H	L	X	L
L	H	H	X	H
L	L	X	L	L
L	L	X	H	H
Dutnut	lovel	hefore the	indical	and stoody, state

† Output level before the indicated steady-state input conditions were established

# RECOMMENDED OPERATING CONDITIONS

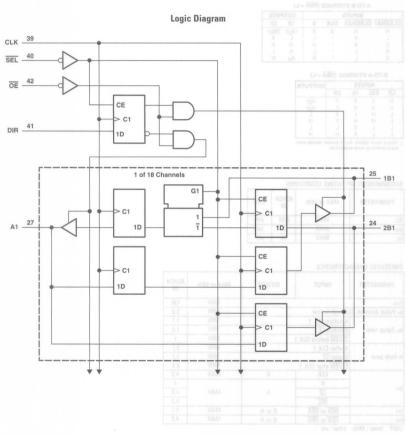
PARAMETER	MAX or MIN	ALVCH 3V	UNIT
Icc	MAX	0.04	mA
Іон	MAX	-24	mA
lou	MAX	24	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
fmax			MIN	130
tw Pulse duration,	CLK high or low	30 -	MIN	3.3
	A before CLK ↑		MIN	1.7
tsu Setup time	B before LE	MIN	1.3	
	CLKEN before CLK ↑	MIN	1	
	A after CLK ↑	MIN	0.7	
th Hold time	B after LE	MIN	1.1	
	CLKEN after CLK †	MIN	0.9	
	CLK	В	MAX	4.3
	В			4
tpd	LE	A	MAX	4.8
	SEL			5.2
ten	OEB or OEA	BorA	MAX	5.1
tdis	OEB or OEA	B or A	MAX	4.2

UNIT fmax: MHz other: ns





#### A-TO-B STORAGE (OE = L, DIR = H)

INPUTS			OUTPUTS	
SEL	CLK	Α	1B	2B
Н	X	X	1Bot	2Bot
L	+	L	L‡	X
		1.1	1.14	V

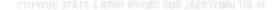
# B-TO-A STORAGE (OE = L, DIR = L)

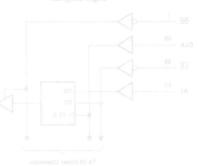
	INP	OUTPUT		
CLK	SEL	1B	2B	A
+	Н	X	L	L§
	H	X	H	H§
	L	L	X	L
+	L	H	X	H

§ Two CLK edges are needed to propagate the data. The data is loaded in the first register when SEL is low and propagates to the second register when SEL is high.

#### OUTPUT ENABLE

INPUTS			OUT	PUTS	
CLK	OE	DIR	Α	1B,2B	
†:	Н	X	Z	Z	
+	L	L	Z	Active	
+	L	H	Active	Z	





RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT	
Icc	MAX	0.04	mA	
Іон	MAX	-24	mA	
lou	MAX	24	mA	

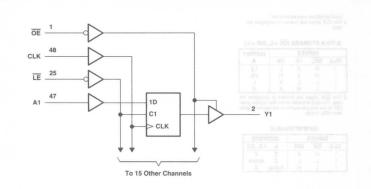
SWITCHING CHA	HACTERISTICS			_
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
fmax			MIN	150
tw Pulse duration,	CLK high or low		MIN	3.3
	A data before CLK	MIN	2	
. 0	B data before CLK	1	MIN	1.8
tsu Setup time	DIR before CLK ↑		MIN	1.7
	SEL before CLK ↑		MIN	1.8
	A data after CLK ↑		MIN	0.7
th Hold time	B data after CLK ↑		MIN	0.6
th Hold time	DIR after CLK ↑		MIN	0.5
	SEL after CLK ↑		MIN	0.8
	OLK	A	MAX	5
tpd	CLK	В	IMAX	5.3
ten	ŌĒ	A	MAN	5.7
	UE	В	MAX	7.4
	ŌĒ	A	MAN	5.7
tdis	UE.	В	MAX	6.4

UNIT fmax : MHz other : ns

L ↑ H H‡ X

† Output level before the indicated steady-state input conditions were established

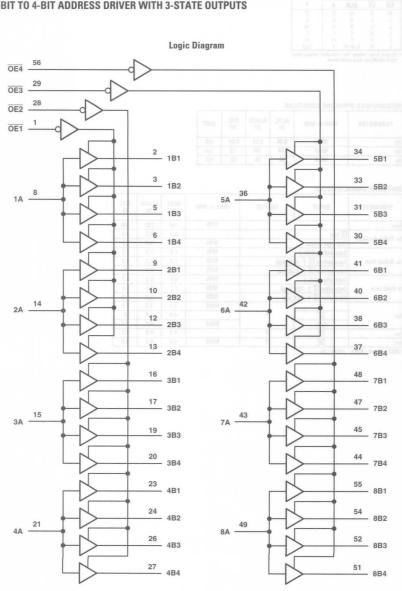
‡ Two CLK edges are needed to propagate the data.



FUNCTION TABLE

	INF	OUTPUT		
OE	OE LE	LE CLK A		Y
Н	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	1	L	L
L	H	1	H	H

L H 1 L H Lo Output level before	L L H H rH X Y0†									
input conditions were	established	,								
DECOMMENDED (	OPERATING CONDITION	NIC								
RECUMINIENDED (	JPERATING CONDITIO	11/1/2								
PARAMETER	MAX or MIN	ALVC 3V	ALVCH 3V	AVC 3V	UNIT					
CC	MAX	0.04	0.04	0.04	mA					
34 но	MAX	-24	-24	-12	mA					
OL TELE	MAX	24	24	12	mA					
SWITCHING CHAP	RACTERISTICS	1		100		182	8			
PARAMETER	INPUT	01	JTPUT	M	AX or MIN	ALVC 3V	ALVCH 3V	AVC 3V		
fmax		4		+	MIN	150	150	150		
20.00	LE low	A	-	+		3.3	3.3	3.3		
w Pulse duration	CLK high or low			+	MIN	3.3	3.3	3.3		
	Data before CLK ↑	N		_	MIN	1.5	1.5	0.7		
su Setup time		I K binb		+	MIN	1.3	1.3	0.9		
taa	Data before LE↑ C		_	+	MIN	1.2	1.2	1		
1.000	Data after CLK ↑		-	+	MIN	0.9	0.9	0.7		
h Hold time			-	+	MIN	1.1	1.1	1.5		
h Hold time	Data after LE ↑ CLM		_	+	MIN	\$1.15	1.1	1.3		
208	A A	low	1		MAX	3.3	3.3	2.5		
lpd	LE		Υ	-	IVIAN	4.4	4.4	4		
EBB	CLK	4	ľ	-	MAX	4.1	4.1	3.1		
ten	OE OE	7	Υ	+	IVIMA	4.6	4.6	6.2		
ten tdis	OE OE	-	Y	+	MAX	4.4	4.4	5.3		
UNIT fmax : MH;		4	-		IVIAA	284	4.4	5.5		
51411 HIIDX . 14111	2 00101 . 113									



# 6-BIT TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

INPL	JTS	OUTPUT
INPUTS OE A L H L L	Bn	
L	Н	Н
L	L	L
1.1	H	7

RECOMMENDED OPERATING CONDITIONS

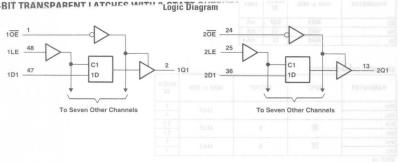
PARAMETER	MAX or MIN	ALVCH 3V	UNIT
Icc	MAX	0.04	mA
Іон	MAX	-24	mA
Ini	MAX	24	mA

Louic Disoram

SWITCHING CHARACTERISTICS

SWITCHING CHARAC	TERISTICS		86 F6	11
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
tplH .	A 100 and 100		MAX	4
tPHL .	elem A Diserio	D	IVIAA	4
tPZH	ŌĒ		1444	5.1
tPZL	UE	В	MAX	5.1
tPHZ	ŌĒ		MAN	4
tPLZ	UE	В	MAX	4

# 16-BIT TRANSPARENT I ATCHES WITH CLOGIC Diagram



### RECOMMENDED OPERATING CONDITIONS

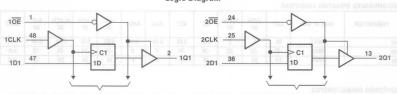
TIEGOTHINETADED OF	ENFITHE CONTENT	0140											
PARAMETER	MAX or MIN	ABT	LVTH 3V	ALVTH 3V	AC	ACT	AHC	AHCT	LVC 3V	LVCH 3V	ALVCH 3V	AVC 3V	UNIT
Icc	MAX	85	-5	5	0.08	0.08	0.04	0.04	0.02	0.02	0.04	0.04	mA
Іон	MAX	-32	-32	-32	-24	-24	-8	-8	-24	-24	-24	-12	mA
lou	MAX	64	64	64	24	24	8	8	24	24	24.	12	mA

#### SWITCHING CHARACTERISTICS

SWITCHING CHAI	ACTEMISTICS	neves or				inniin)	torillO re	10885 01		
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	ALVTH 3V	AC	ACT	AHC	AHCT
tw Pulse duration,	LE high or low		MIN	3.3	3	1.5	4	1	5	6.5
tsu Setup time	Data before LE \$\d d	ata high	MIN	1.5	1	1.4	1.5	1	4	1.5
isa Setup time	Data before LE ↓, d	ata low	MIN	1.5	1	0.9	1.5	1	4	1.5
a. Haldaima	Data after LE 1, dat	ta high	MIN	1	1	0.9	2.4	5	1	3.5
th Hold time	Data after LE ↓, dat	ta low	MIN	1	1	1.4	2.4	5	1	3.5
tPLH	D	Q	MAX	6.3	3.8	3.1	9.7	11.1	10.5	10.5
tphl.	7 0	u	MAX	6.2	3.6	3.3	10.1	12.3	10.5	10.5
tPLH	LE	Q	MAN	6.7	4.3	3.3	11.9	12.8	10.5	10.5
tphl.	LE	u	MAX	6.1	4	3.5	10.9	12.2	10.5	10.5
tpzh	ŌĒ	Q	MAN	6.1	4.3	4	10.8	12.1	11.5	11.5
tPZL	UE UE	u u	MAX	5.6	4.3	3.4	12.8	14.2	11.5	11.5
tPHZ	- OE	0	MAN	8.1	5	4.9	8.8	10.7	11.5	12
tPLZ	- UE	Q	MAX	6.5	4.7	4.5	8.1	9.4	11.5	12

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 3V	LVCH 3V	ALVCH 3V	AVC 3V
tw Pulse duration,	LE high or low		MIN	3.3	3.3	3.3	1.8
	Data before LE 1, d	ata high	MIN	1.7	1.7	1.1	0.8
tsu Setup time	Data before LE 1, d	ata low	MIN	1.7	1.7	1.1	0.8
n Hatel days	Data after LE 1, dat	a high	MIN	1.2	1.2	1.4	1
th Hold time	Data after LE 1, dat	a low	MIN	1.2	1.2	1.4	1
tPLH	D		MANY	4.2	4.2	3.6	2.8
tPHL .	D	ā	MAX	4.2	4.2	3.6	2.8
tplH .	1.5		1441	4.6	4.6	3.9	3.2
tPHL	LE	Q	MAX	4.6	4.6	3.9	3.2
tPZH	ŌE		1447	4.7	4.7	4.7	3.4
tPZL	UE	Ω	MAX	4.7	4.7	4.7	3.4
tPHZ			1447	5.9	5.9	4.1	3.9
tPLZ	OE OE	Q	MAX	5.9	5.9	4.1	3.9

# **Logic Diagram**



TACTERISTICS V		To Seven Other Channels									
Other Channels	To Seven C				n Other	To Seve					

#### FUNCTION TABLE (each fllp-flop)

	INPUTS		OUTPUT
ŌE	CLK	D	Q
L	1	Н	Н
L	7	L	L
L	HorL	X	QO
H	×	X	Z

### RECOMMENDED OPERATING CONDITIONS

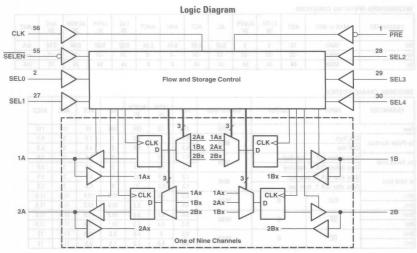
PARAMETER	MAX or MIN	ABT	LVTH 3V	ALVTH 3V	AC	ACT	AHC	AHCT	LVC 3V	LVCH 3V	ALVCH 3V	AVC 3V	UNIT
Icc	MAX	72	5	5	0.08	0.08	0.04	0.04	0.02	0.02	0.04	0.04	mA
Іон пр	MAX	-32	-32	-32	-24	-24	-8	-8	-24	-24	-24	-12	mA
lou	MAX	64	64	64	24	24	8	8	24	24	24	12	mA

# SWITCHING CHARACTERISTICS

SWITCHING CHAR	ACTERISTICS	1		_	_			_	4	73	1
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	ALVTH 3V	AC	ACT	AHC	AHCT	7.
fmax	1		MIN	150	160	250	100	65	110	110	
tw Pulse duration	CLK high	10.10	MIN	3.3	3	1.5	5	7.5	5	6.5	
tw Pulse duration	CLK low		MIN	3.3	3	1.5	5	4.5	5	6.5	
	Data before CLK 1,	data high	X 28x X	1.1	1.8	1	- 5	4.5	3	2.5	A
tsu Setup time	Data before CLK 1,	data low	MIN	1.1	1.8	1.5	5	4.5	3	2.5	
th Hold time	Data after CLK ↑, d	a after CLK ↑, data high		1.3	0.8	0.5	0	6.5	2	2.5	
th Hold time	Data after CLK ↑, d	ata low	MIN	1.3	0.8	11	0	6.5	2	2.5	
tPLH .	CLK	XUS	MAN	6.2	4.5	3.2	10.8	12.4	11.5	11.5	
tPHL .	CLK	0 0	MAX	5.9	4	3.2	10.6	12.2	11.5	11.5	
tPZH	ŌĒ	0	MAX	5.6	4.5	3.8	10.2	11.9	11.5	11.5	D.
tPZL	UE	u	IVIAX	5.3	4.4	3.3	12.1	13.4	11.5	11.5	
tPHZ	ŌĒ	0	MAN	8.2	5	4.6	8.2	10.4	11.5	12	
tPLZ	UE	Q	MAX	6.6	4.6	4.2	7.9	9.8	11.5	12	

PARAMETER	INPUT	OUTPUT	MAX or MIN	3V LVC	3V LVCH	ALVCH 3V	AVC 3V	
fmax			MIN	150	150	150	200	
. D. I I	CLK high		MIN	3.3	3.3	3.3	2.5	
tw Pulse duration	CLK low		Pulse duration CLK low	IVIIN	3.3	3.3	3.3	2.5
. Catao tima	Data before CLK ↑, data high Data before CLK ↑, data low Data after CLK ↑, data high		MIN	1.9	1.9	1.9	1.4	
tsu Setup time			IVIIIV	1.9	1.9	1.9	1.4	
th Hold time			MIN	1.9	1.1	0.5	1.1	
th Hold time	Data after CLK ↑, da	ata low	IVIIIV	1.9	1.1	0.5	1.1	
tplH	CLK	Q	MAX	4.5	4.5	4.2	3.3	
tphl .	CLK	u u	WAX	4.5	4.5	4.2	3.3	
tPZH	ŌE	0	MANY	4.6	4.6	4.8	3.4	
tPZL	UE	u	MAX	4.6	4.6	4.8	3.4	
tPHZ	<u></u>	0	MAN	5.5	5.5	4.3	3.9	
tPLZ	OE Q		MAX	5.5	5.5	4.3	3.9	

UNIT fmax : MHz other : ns



L	X	в <sub>0</sub> †
		ndicated steady-state
input con	ditions were est	ablished

#### DATA-ELOW CONTROL

				ATA-F	LOW C	ONTE	OL	
L	L	1	0	0	1	0	0	Not used
L	L	1	0	0	1	0	1	Not used
L	L	1	0	-0	1	1	0	Not used
L	L	1	0	0	1	1	1	Not used
L	L	1	0	1	0	0	0	2A to 1A and 1B to 2B
L	L	1	0	1	0	0	1	2A to 1A
L		1	0	1	0	1	0	2B to 1B
L	L	1	0	1	0	1	1	2A to 1A and 2B to 1B
L	-	1	0	1	1	0	0	1A to 2A and 1B to 2B
L	L	1	0	1	1	0	1	1A to 2A
L	L	1	0	1	1	1	0	1B to 2B
L	L	1	0	1	1	1	1	1A to 2A and 2B to 1B
L	L	1	1	0	0	0	0	1A to 1B and 2B to 2A
L	L	1	1	0	0	0	1	1A to 1B
L	L	1	1 .	- 0	0	1	0	2A to 2B
L	L	1	1	0	0	1	1	1A to 1B and 2A to 2B
L	L	1	1	0	1	0	0	1B to 1A and 2A to 2B
L	L	1	1	0	1	0	1	1B to 1A
L	L	1	1.	0	1	1	0	2B to 2A
L	L	1	1	0	1	1	1	1B to 1A and 2B to 2A
L	-L	1	1	1	0	0	. 0	2B to 1A and 2A to 1B
L	L	1	1	1	0	0	1	1B to 2A
-1	L	1	1	1	0	1	0	2B to 1A
L	L	1	1	1	0	1	1	2B to 1A and 1B to 2A

1A to 2B and 1B to 2A 1A to 2B 2A to 1B 1A to 2B and 2A to 1B

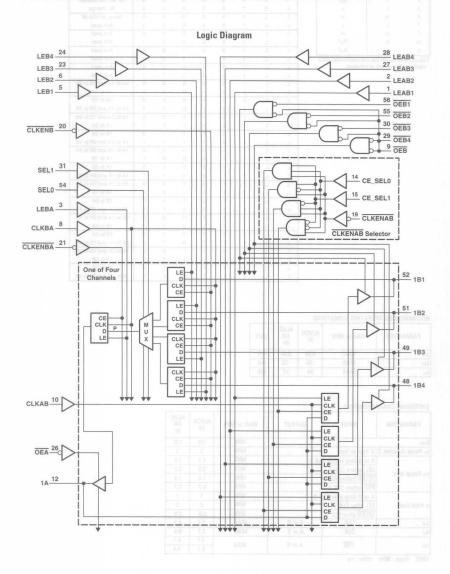
### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	ALVC HR 3V	UNIT
Icc	MAX	0.04	0.04	mA
Іон	MAX	-24	-12	mA
lou	MAX	24	12	mA

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V	ALVO HR 3V
fmax	11-17-22	TI II	MIN	120	120
tw Pulse duration,	CLK high or low	19	MIN	3	3
	A or B data before CLF	< †	MIN	1.4	1.4
	SEL before CLK ↑	-6	MIN	3.5	3.5
tsu Setup time	SELEN before CLK ↑		MIN	1.8	1.8
	PRE before CLK ↑		MIN	0.7	0.7
	A or B data after CLK	1	MIN	1	- 1
th Hold time	SEL after CLK ↑	-0	MIN	0	0
	SELEN after CLK ↑	J.	MIN	0.8	0.8
tpd	CLK	A or B	MAX	5.1	6.2
ten	CLK	A or B	MAX	5.7	6.8
. i	PRE	A D	BAAV	5.7	6.1
tdis	PHE	A or B	MAX	6.1	6.4

UNIT fmax: MHz other: ns

# 4-TO-1 MULTIPLEXED/DEMULTIPLEXED TRANSCEIVERS WITH 3-STATE OUTPUTS



# A-TO-B OUTPUT ENABLE (assuming OEB = L, OEBn = L) ‡

A-10	-B UUTPI	JI ENABLE
IN	IPUTS	OUTPUT
OE	B OEBn	Bn
H	H	Z
H	L	Z
L	H	Z
L	L	Active

INP	UTS	OUTPUT
OEB	OEBn	Bn
Н	Н	Z
H	L	Z
L	H	Z
L	L	Active

INPUTS							OUT	PUTS			
CLKENAB	CE_SEL1	CE_SEL0	CLKAB	LEAB1	LEAB2	LEAB3	LEAB4	B1	B2	B3	B4
X	X	X	HorL	Н	L	L	L	Α	Ao	Ao	Ao
X	X	X	HorL	H	H	H	L	A	A	A	An
L	X	X	L	L	L	L	L	An	An	An	An
L.	L	L	4	L	L	L	L	A	Ao	Ao	Ao
L	L	H	1	L	L	L	L	Ao	A	An	An
L	H	L	1	L	L	L	L	Ao	An	A	An
L	Н	H	1	L	L	L	L	Ao	Ao	Ao	A
H	X	X	*	L	L	L	L	An	An	An	An

#### B-TO-A STORAGE (after point P)

B-TO-A STORAGE (after point P)

			INPUT	S				_
CLKENB	CLKBA	LEB1	LEB2	LEB3	LEB4	SEL1	SEL0	Р
X	X	Н	L	L	L	L	L	B1
X	X	L	H	L	L	L	H	B2
X	X	L	L	H	L	H	L	B3
X	X	L	L	L	H	H	Н	B4
L	†	L	L	L	L	L L H	L H L	B1 B2 B3
L	L	L	L	L	L	L L DH H	H L H L	B10† B20† B30† B40†

	OUTPUT				
CLKENBA	CLKBA	LEBA	OEA	В	A
X	X	X	Н	X	Z
X	X	H	L	L	Land Land
X	X	H	L	Н	H
H	X	L	L	X	Ant
L	1.5	L	L	L	L.
L	1	L	L	H	Н
L	L	L	L	X	Ant

# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABTH	UNIT
Icc	MAX	32	mA
Іон	MAX	-32	mA
lou	MAX	64	mA

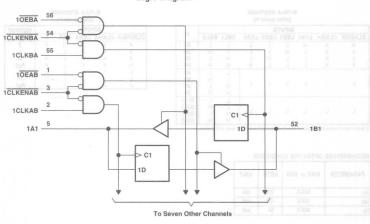
# SWITCHING CHARACTERISTICS

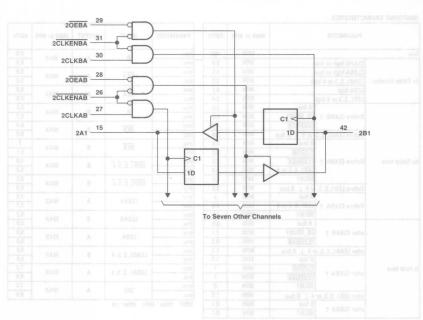
	PARAMETER		MAX or MIN	ABTH
fmax			MIN	160
	CLKAB high or lov	LKAB high or low	3.8	
	CLKBA high or lov	N	MIN MIN MIN MIN MIN MIN MIN MIN MIN MIN	4.5
tw Pulse duration	LEAB1, 2, 3 or 4 high		MIN	2.2
	LEBA high	MIN   MIN	2.1	
	LEB1, 2, 3 or 4 hig	h	MIN MIN MIN MIN MIN MIN MIN MIN MIN MIN	2.4
		A bus	MIN	2.5
	Before CLKAB ↑	CE_SEL0/1	MIN	3.2
w Pulse duration	Sh	CLKENAB	MIN	3.2
	Before LEAB1, 2, 3, or 4 ↓ A bus		MIN	3.6
		B bus	MIN	3.8
	Before CLKBA ↑	CLKENB	MIN	2.3
tsu Setup time		CLKENBA	MIN	2.5
		LEB1, 2, 3 or 4	MIN	4.3
		SEL0/1	MIN	4.5
	Before LEB1, 2, 3,	MIN   MIN	3.2	
		B bus	MIN	4
tsu Setup time	Before CLKBA ↑	LEB1, 2, 3 or 4	MIN	4.4
		SEL0/1	MIN MIN MIN MIN MIN MIN MIN MIN MIN MIN	4.3
		A bus	MIN	0.5
after CLK	after CLKAB ↑	CE_SEL0/1	MIN	1.1
	The state of the s	CLKENAB	MIN	0.5
	after LEAB1, 2, 3,	or 4 ↓ A bus	MIN	1.2
			MIN	1.3
ı Hold time	-6 CI VDA A	CLKENB	MIN	1
	Before CLKBA ↑  after CLKAB ↑  after LEAB1, 2, 3,  Hold time after CLKBA ↑	CLKENBA	MIN	1
		SEL0/1	MIN MIN II MIN II MIN II MIN MIN MIN MIN	0
	after LEB1, 2, 3, or 4 ↓ B bus		MIN	1.5
	after CLKBA ↑	B bus	MIN	0.4
		SEL0/1	MIN	0.1

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH
tPLH	В	08 A		6.5
tPHL .	В	AASX	MAX MAX MAX	6.5
tРZH	0EA	80 A	NAMA	5.6
tPZL	UEA	A	MAX MAX MAX MAX MAX MAX MAX MAX MAX MAX	5.2
tPHZ	0EA	85 A	MAN	5.9
tPLZ	UEA	AHAM	MAX or MIN  MAX  MAX  MAX  MAX  MAX  MAX  MAX  MA	6.5
tPLH		27	MAN	5.7
tphl .	A		IVIAX	5.7
tрzн	OFF	2f n	MAN	6.4
tPZL	UEB	BIAS	IVIAX	6.3
tPHZ	OFF	A B MAX  DEB B MAX  T, 2, 3, 4 B MAX	7	
tPLZ	UED		IVIAX	6.1
tPZH	OED1 2 2 4	В	MAY	5.8
tPZL	UEB1, 2, 3, 4	В	MAX	5.6
tPHZ	OFD1 2 2 4	n	MANY	6.1
tPLZ	UEB1, 2, 3, 4	В	MAX or MIN  MAX  MAX  MAX  MAX  MAX  MAX  MAX  MA	5.3
tPLH	CINBV	Α.	MAX MAX MAX MAX MAX MAX MAX MAX MAX MAX	7.4
tPHL .	CLKBA	A	IVIAX	7.7
tPLH	CLKAB	В	MAX MAX MAX MAX MAX MAX MAX MAX MAX MAX	6.2
tPHL	CLKAB	В	IVIAX	5.9
tPLH	LEBA	А	MAN	5.6
tphl .	LEDA	A	IVIAX	5.3
tplh	LEAB1, 2, 3, 4	В	A RANG	5.8
tphl.	LEAD1, 2, 3, 4	Ь	IVIAX	5.6
tPLH	LEBA1, 2, 3, 4	А	MAN	7.2
tphl.	LLDM1, 2, 3, 4	A	IVIAA	6.8
tplh	SEL	A	MAN	7.5
tPHL.	OEL	A	IVIAX	6.9

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty, Production processing does not necessarily include testing of all parameters. See www.ti.com/sc/logic for the most current data sheets.







INPUTS			OUTPUT	
CLKENA	CLKAB	OEAB	Α	В
Н	X	X	X	Z
X	×	H	X	Z
L	L	L	X	Bo#
L	1	L	L	Ĺ
1		1	H	H

† A-to-B data flow is shown; B-to-A flow is similar but uses CLKENBA, CLKBA, and OEBA.

† Output level before the indicated steady-state input conditions were established.

# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ACT	UNIT
Icc	MAX	35	0.08	mA
Іон	MAX	-32	-24	mA
lor	MAX	64	24	mA

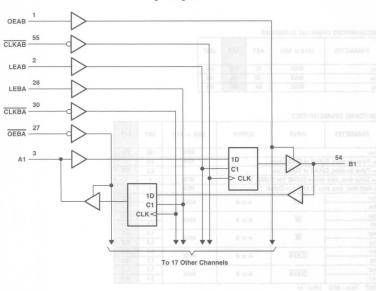
### SWITCHING CHARACTERISTICS

	71211101100			_	
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT
fmax			MIN	150	55
tw Pulse duration, CL	KAB or CLKBA high	01	MIN	3.3	4
tw Pulse duration, CL	KAB or CLKBA low	10		3.3	8.5
tsu Setup time, data b	efore CLKAB † or C	LKBA ↑	MIN	4	6
th Hold time, data afte	er CLKAB † or CLKE	BA ↑	MIN	1	1
tPLH	CLK	A or B	MAX	4.9	11.8
tPHL	CLK	AorB		4.9	11.7
tрzн	ŌĒ	A or B	MAN	4.9	11.9
tPZL	UE	AorB	MIN MIN MIN	6.8	13.4
tPHZ	ŌE	A or B	MAX	5.5	9.9
tPLZ	UE	AorB		5.3	9.5
tPZH	CLKEN	A or B	MAX	5.7	12.5
tPZL.	CLKEN	A OF B		7.2	14.3
tPHZ	CLKEN A or B MAX	MAX	5.8	11.2	
tPLZ	CLKEN	A or B	IVIAX	5.4	10.9

UNIT fmax: MHz other:ns



### Logic Diagram



#### FUNCTION TABLE

	OUTPUT			
OEAB	LEAB	CLKAB	Α	В
L	X	X	X	Z
H	H	×	L	L
H	H	X	H	H
Н	L	4	L	L
H	L	j.	H	H
H	L	H	X	Bo‡
H	1	1	V	Bo8

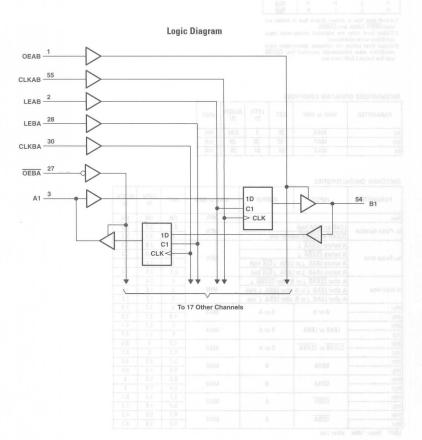
† A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA. Cutput level befor the indicated steady-state input conditions were established. Soutput level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVTH 3V	ALVCH 3V	UNIT
Icc	MAX	36	5	0.04	mA
Іон	MAX	-32	-32	-24	mA
lou	MAX	64	64	24	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	ALVCH 3V
fmax		XLID <	MIN	150	150	150
tw Pulse duration	LEAB or LEBA high		MIN	2.5	3.3	3.3
tw Pulse duration	CLKAB or CLKBA high	or low	IVIIIV	3	3.3	3.3
	A before CLKAB ↓		9-1	3	2.9	1.3
. C	B before CLKBA ↓		MIN	3	2.9	1.3
tsu Setup time	A before LEAB ⊥ or LEBA ⊥ CLK high		MIN	1	1.4	1
	A before LEAB 1 or LE	BA J CLK low		2.5	2.9	1.4
	A after CLKAB ↓ or B	after CLKBA 1	99 99	0	0.4	1.3
	A after LEAB ↓ or B after LEBA ↓ high		MIN	2	1.6	1.5
	A after LEAB 1 or B at	A after LEAB ↓ or B after LEBA ↓ low		2	1.6	1.2
tPLH	4 - 0	2 4	MAX	- 4	3.7	3.9
tphL .	A or B	B or A	MAX	4.9	3.7	3.9
tPZH	1540 1504	D A	MAN	5	5.1	4.7
tPZL	LEAB or LEBA	B or A	MAX	5	5.1	4.7
tphz.	CLKAB or CLKBA	D A	MAN	5.3	5	5.5
tPLZ	CLKAB OF CLKBA	B or A	MAX	5.3	5	5.5
tpzh	0510	В	1111V	5.1	4.8	4.6
tPZL	- OEAB	В	MAX	5.4	4.8	4.6
tрнz	0540	В	MAX	6.5	5.8	5
tPLZ	0EAB	В	MAX	5.4	5.8	5
tpzh	0504		MAN	5.1	4.8	5.2
tPZL	OEBA	A	MAX	5.4	4.8	5.2
tPHZ	OFDA		MAN	6.5	5.8	4.3
tPLZ	OEBA	A	MAX	5.4	5.8	4.3



† A-to-B data flow is shown: B-to-A flow is similar but uses ØEBÄ, LEBA, and CLKBA.

2 Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

3 Output level before the indicated steady-state input conditions were established.

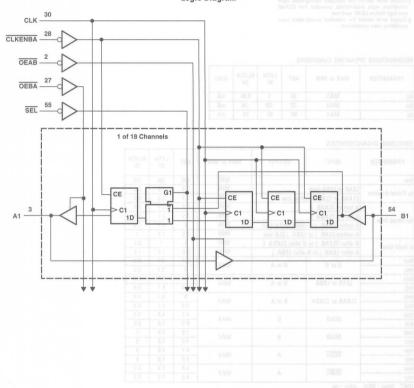
#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVTH 3V	ALVCH 3V	UNIT
Icc	MAX	- 76	5	0.04	mA
Іон	MAX	-32	-32	-24	mA
lou	MAX	64	64	24	mA

#### CIMITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	ALVCH 3V
fmax			MIN	105	150	150
tw Pulse duration	LEAB or LEBA high		MIN	3.3	3.3	3.3
tw Pulse duration	CLKAB or CLKBA high	h or low	MIN	4.7	3.3	3.3
as 1	A before CLKAB ↑		MIN	3.5	2.1	1.7
	B before CLKBA ↑	10-	MIN	3.5	2.1	1.7
tsu Setup time	A before LEAB ↓ or L	EBA J CLK high	MIN	4	2.4	1.5
	A before LEAB 1 or L	EBA J CLK low	MIN	1.5	1.4	1
	A after CLKAB ↑ or B	after CLKBA ↑	MIN	1	1	0.7
th Hold time	A after LEAB ↓ or B a		MIN	2.5	1.7	1.4
tPLH			EAAV.	3.7	3.7	3.9
TPHL	A or B	B or A	MAX	4	3.7	3.9
tPZH	1540 1504		1117	5.1	5.1	4.6
tPZL .	LEAB or LEBA	B or A	MAX	4.4	5.1	4.6
tPHZ	CIVAD CIVDA	D A	MAN	5	5.1	4.9
tPLZ	CLKAB or CLKBA	B or A	MAX	4.4	5.1	4.9
tPZH	0510	В	1111	4.7	4.8	4.6
tPZL	- OEAB	В	MAX	6.5	4.8	4.6
tPHZ	0510		1447	5.8	5.8	5
tPLZ	- OEAB	В	MAX	4.9	5.8	5
tPZH	0504		1117	4.7	4.8	5
tPZL	OEBA	A	MAX	6.5	4.8	5
tPHZ	0504		MAN	5.8	5.8	4.2
tPLZ	OEBA	A	MAX	4.9	5.8	4.2

**Logic Diagram** 



**FUNCTION TABLE** B-TO-A STORAGE (OEBA = L)

INPUTS			OUTPUT	
CLKENBA	CLK	SEL	В	A
Н	X	X	X	Ant
L		Н	L	Ľ
L	+	H	Н	H
L	*	L	L	L‡
L	+	L	Н	H±

Output level before the indicated steady-state input conditions were established
 Four positive CLK edges are needed to propagate data from B to A when SEL is low.

#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
Icc	MAX	0.04	mA
Іон	MAX	-24	mA
lou	MAX	24	mA

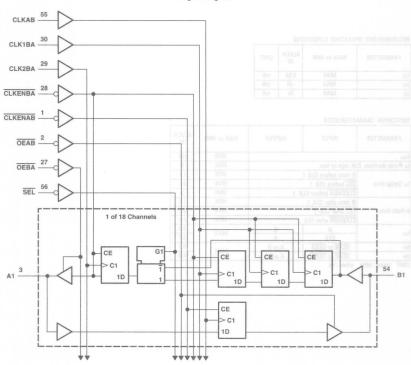
#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
fmax			MIN	150
tw Pulse duration, CLK high or low			MIN	3
	B data before CLK ↑	MIN	1.1	
tsu Setup time	SEL before CLK ↑	MIN	2.1	
	CLKENBA before CLK	MIN	2	
	B data after CLK ↑	MIN	1.2	
th Hold time	SEL after CLK ↑	MIN	0.8	
	CLKENBA after CLK	MIN	0.3	
	A	В	MAX	3.2
tpd	CLK	A	MAX	5.2
ten	OEAB or OEBA	A or B	MAY	5.1
tdis	OEAB or OEBA	A or B	MAX	4.9

### 18-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS







B-TO-A STORAGE (OEBA = L)

	IN	PUTS			OUTPUT
CLKENA	CLK2BA	CLK1BA	SEL	В	A
Н	X	X	X	X	Ant
L	*	×	H	L	L
L	1	X	H	H	H
L			L	L	L‡
L	1	1.00	L	H	H±

#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
Icc	MAX	0.04	mA
Іон	MAX	-24	mA
lor	MAX	24	mA

#### SWITCHING CHARACTERISTICS

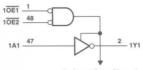
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
fmax			MIN	150
tw Pulse duration, CLK high or low			MIN	3
	A data before CLKAB	1	MIN	1.3
tsu Setup time	B data before CLK2BA	1	MIN	1.7
	B data before CLK1BA	MiN	1.1	
	SEL before CLK2BA 1	MIN	3.3	
	CLKENAB before CLK	MIN	1.6	
	CLKENBA before CLK	MIN	2.1	
	CLKENBA before CLK	2BA ↑	MIN	2.2
	A data after CLKAB ↑		MIN	0.9
	B data after CLK2BA	MIN	0.6	
	B data after CLK1BA	MIN	1	
th Hold time	SEL after CLK2BA ↑		MIN	0.1
	CLKENAB after CLKA	Β ↑	MIN	0.3
	CLKENBA after CLK18	BA ↑	MIN	0.1
	CLKENBA after CLK2BA ↑		MIN	0
tpd	CLKAB or CLK2BA	A or B		4.2
ten	OEAB or OEBA	A or B	MAX	5.1
tdis	OEAB or OEBA	A or B	1 23	4.9

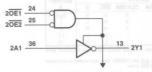
Output level before the indicated steady-state input conditions were established.
 Three CLK1BA edges and one CLK2BA edge are needed to propagate data from B to A when SEL is low.

### 16540

### 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS







To Seven Other Channels

To Seven Other Channels

**FUNCTION TABLE** (each 8-bit section)

	INPUTS	OUTPUT	
OE1	OE2	A	Υ
L	L	L	Н
L	L	Н	L
H	X	X	Z
X	H	X	Z

OE1	OE2	A	Y	
L	L	L	Н	
L	L	H	L	
H	X	X	Z	
X	H	X	Z	

RECOMMENDED	OPERATING CONDIT	IONS	
PARAMETER	MAY or MIN	ART	ACT

PARAMETER	MAX or MIN	ABT	ACT	AHC	AHCT	LVCH 3V	UNIT
Icc	MAX	34	0.08	0.04	0.04	0.02	mA
Іон	MAX	-32	-24	-8	-8	-24	mA
lou	MAX	64	24	8	8	24	mA

SWITCHING CHARAC	CTERISTICS		5.0	114191			T BANK	TOUR DE
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT	AHC	AHCT	LVCH 3V
tPLH .	А	V	MAN	4.1	7.5	8.5	10.5	3.7
tPHL .		T	MAX	4.3	9.5	8.5	10.5	3.7
tPZH	ŌĒ	Y	MAX	5.1	8.9	10.5	13	4.8
tPZL	UE			5.9	10.5	10.5	13	4.8
tPHZ	ŌĒ	γ γ	MAX	5.7	11.9	10.5	13	5.9
tPLZ	UE			4.7	11.1	10.5	13	5.9

### 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS HTIM 28-34/3328/AST 083T21938 TIR-81

### Logic Diagram



FUNCTION TABLE (each 8-bit section)

1	INPUTS	ê	OUTPUT
OE1	OE2	Α	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	7

RECOMMENDED OPERATING CONDITIONS

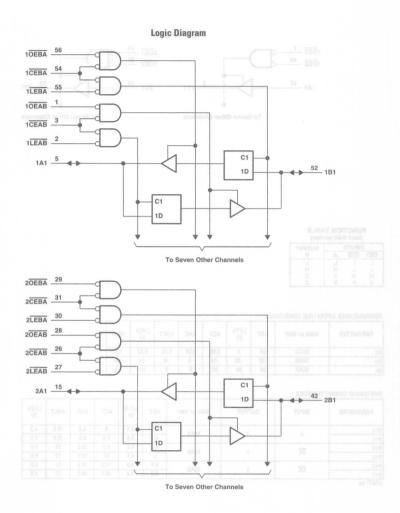
PARAMETER	MAX or MIN	ABT	LVTH 3V	ACT	AHC	AHCT	LVCH 3V	UNIT
Icc	MAX	34	5	0.08	0.04	0.04	0.02	mA
Іон	MAX	-32	-32	-24	-8	-8	-24	mA
lou	MAX	64	64	24	8	8	24	mA

SWITCHING CHARACTERISTICS

SWITCHING CHARAC	TERISTICS								-
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	ACT	AHC	AHCT	LVCH 3V
tPLH .	А	Α Υ	MAX	3.4	3.5	9	8.5	10.5	4.2
tPHL .				4.2	3.5	9.2	8.5	10.5	4.2
tPZH		v	MAX	5.2	4.6	9.7	10.5	13	5.6
tPZL	ŌĒ	Υ		6	4.6	11	10.5	13	5.6
tPHZ	ŌĒ	Y	MAN	5.4	5.9	11.3	10.5	13	6.8
tPLZ			MAX	4.3	5.4	10.7	10.5	13	6.8

UNIT: ns

### 16-BIT REGISTERD TRANSCEIVERS WITH 3-STATE OUTPUTS



#### FUNCTION TABLE (each 8-bit section)

	INP	OUTPUT		
OEAB	LEAB	OEAB	A	В
Н	X	X	X	Z
X	×	H	X	Z
L	H	L	X	Bo‡
L	L	L	L	Ľ
L	L	L	H	H

† A-to-B data flow is shown: B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA. ‡ Output level before the indicated steady-state input conditions were established.

Logic Disgram

#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVTH 3V	AC	ACT	TAC 3A	LVCH 3V	ALVCH 3V	UNIT
Icc	MAX	35	5	0.08	0.08	0.04	0.02	0.04	mA
Іон .	MAX	-32	-32	-24	-24	-24	-24	-24	mA
lou	MAX	64	64	24	24	24	24	24	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	AC	ACT	3V LVC	TACH 3A	ALVCH 3V
tw Pulse duration,	LEAB or LEBA low		MIN	4	3.3	4	7.5	4	3.3	3.3
	Data before LEAB	↑ or LEBA ↑, high	MIN	1.5	0.5	1	2.5	2	1.1	1.2
	Data before LEAB	Data before TEAB ↑ or TEBA ↑, low  Data before CEAB ↑ or CEBA ↑, high		3.5	0.8	1	2.5	2	1.1	1.2
tsu Setup time	Data before CEAB			-	0		V.F	2	1.1	1.2
	Data before CEAB ↑ or CEBA ↑, low		MIN	-	0.6		-	2	1.1	1.2
0.9	Data after LEAB ↑	Data after LEAB ↑ or LEBA ↑, high		1.5	1.5	3	4	2	1.9	1.3
th Hold time	Data after LEAB ↑ or LEBA ↑, low		MIN	2	1.2	3	4	2	1.9	1.3
n Hold tille	Data after CEAB ↑	or CEBA ↑, high	MIN	-	1.7		-	2	1.9	1.3
	Data after CEAB ↑	Data after CEAB ↑ or CEBA ↑, low		an-	1.6		-	2	1.9	1.3
tPLH	A or B	B or A	MAX	3.8	3.2	8.8	10.5	8	5.4	4.3
tphl.	AUID	B OF A	IVIAA	5.1	3.2	9.2	11.6	8	5.4	4.3
tplh	LE A or B	A or B	MAX	5.2	3.9	11.5	13.8	9	6.1	5
tphL	- LE	AUID	WAX	5.6	3.9	10.9	13.5	9	6.1	5
tpzh	- OE	A or B	MAX	5.2	4.3	9.6	11.4	8.5	6.3	5.3
tPZL	UE W	AUID	IVIAA	7	4.3	11.3	13.2	8.5	6.3	5.3
tPHZ	ŌĒ	A or B	MAX	5.7	4.7	8.9	11.1	8.5	6.3	4.6
tPLZ	UE	AUID	IVIAA	4.6	4.4	8.4	9.6	8.5	6.3	4.6
tpzh	CE	A and D	MAX	6.2	4.5	9.8	11.7	9	6.6	5.6
tPZL	7	CE A or B	IVIAA	7.8	4.5	11.5	13.5	9	6.6	5.6
tPHZ	CE	A or B	MAX	6.6	4.9	9.3	11.6	9	6.6	5.1
tPLZ	7 05	M OF B	IVIAA	5.4	4.7	8.8	10.5	9	6.6	5.1

UNIT: ns

# Logic Diagram OEAB 1 CLKENAB 56 CLKAB 55 LEAB 2 LEBA 28 CLKBA 30 CLKENBA 29 OEBA 27 CE 1D C1 > CLK CE 1D C1 CLK< To 17 Other Channels

#### **FUNCTION TABLE**

		INPUTS			OUTPUT
CLKENAB	OEAB	LEAB	CLKAB	A	В
X	Н	X	X	X	Z
X	L	H	X	L	L
X	L	H	×	H	H
H	L	L	X	X	Bo‡
H	Ĺ.	L	X	X	Bo‡
L	L	L	1	L	L
L	L	L	4	H	H
L	L	L	Н	X	B <sub>0</sub> ‡
1	L	L	L	X	Bn6

† A-to-B data flow is shown: B-to-A flow is similar but uses ŌĒBĀ, LEBA, CLKBĀ and CLKENBĀ. ‡ Output level before the indicated steady-state input conditions were established.

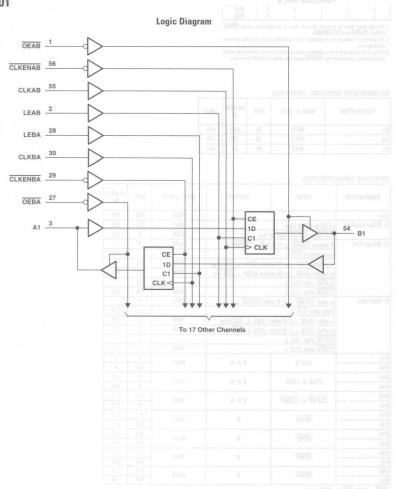
§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ALVCH 3V	UNIT
Icc	MAX	36	0.04	mA
Іон	MAX	-32	-24	mA
loL	MAX	64	24	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ALVCH 3V
fmax			MIN	150	150
tw Pulse duration	LEAB or LEBA high	777	MIN	2.5	3.3
	CLKAB or CLKBA high or I	low	MIN	3	3.3
tsu Setup time	A before CLKAB ↓ or B b		MIN	3	-
	Data before CLK ↑	0-30		1.2	
	A before LEAB ↓ or B before	MIN	2.5	1.1	
	A before LEAB ↓ or B before	MIN	2.5	1.5	
	CLKEN after CLK 1	0	2.5	-	
	CLKEN after CLK ↑		MIN	2.5	0.8
th Hold time	A after CLKAB ↓ or B after	er CLKBA 1	MIN	0	-
	Data after CLK ↑			-	1.5
	A after LEAB ↓ or B after	LEBA J, CLK high	MIN	2	1.6
	A after LEAB ↓ or B after	MIN	2	1.3	
	CLKEN after CLK ↓		1	(=0)	
	CLKEN after CLK ↑		MIN	-	1.4
tPLH .	A or B	B or A	MAX	4	4
tphl.	A OF B	B OF A	WAX	4.9	4
tplH .	LEAB or LEBA	B or A	MAX	5	4.8
tphl.	LEAB OF LEBA	B or A	WAX	5	4.8
tPLH	CLKAB or CLKBA	B or A	MAX	5.3	5.7
tphl.	- CLKAB OF CLKBA	BOLY	MAX	5	5.7
tpzH	OEAB	В	MAX	5.1	5.2
tPZL	UEAD	D	IVIAA	5.4	5.2
tPHZ	- OEAB	В	MAX	6.2	4.4
tPLZ	UEAD	D	IVIAA	5.4	4.4
tPZH	- OEBA	A	MAX	5.1	5.2
tPZL	OLDA	m	IVIMA	5.4	5.2
tPHZ	OEBA	A	MAX	6.2	4.4
tPLZ	J.JA	-	m/A/A	5.4	4.4



L .	L	1		H	н
L	L	L	L	X	B <sub>0</sub> ‡
L	L	L	Н	X	Bo§

<sup>†</sup> A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, CLKBA and CLKENBA 2 Output level before the indicated steady-state input conditions were established.

#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ALVTH 3V	ALVCH 3V	ALVCHR 3V	UNIT
Icc	MAX	36	5	0.04	0.04	mA
Іон	MAX	-32	-32	-24	-12	mA
lou	MAX	64	64	24	12	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ALVTH 3V	ALVCH 3V	ALVCHR 3V
fmax			MIN	150	150	150	150
tw Pulse duration	LEAB or LEBA high		MIN	2.5	1.8	3.3	3.3
tw ruise duration	CLKAB or CLKBA high or	low	MIN	3	2.3	3.3	3.3
	Data before CLK † high		MIN	4	2.4	2.1	2.1
	Data before CLK † low		IVIIIV	4	3.8	2.1	2.1
tsu Setup time	A before LEAB ↓ or B be	fore LEBA ↓, CLK high	MIN	2.5	1	1.6	1.6
Isu Setup time	A before LEAB ↓ or B be	fore LEBA ↓, CLK low	MIN	1	0.6	1.1	1.1
	CLKEN before † high		MIN	2.5	1.4	1.7	1.7
	CLKEN before † low		IVIIIV	2.5	1.9	1.7	1.7
	Data after CLK † high		MIN	0	0.5	0.8	0.8
	Data after CLK ↑ low		IVIIN	0	0.5	0.8	0.8
th Hold time	A after LEAB ↓ or B after LEBA ↓, CLK high A after LEAB ↓ or B after LEBA ↓, CLK low CLKEN after ↑ high CLKEN after ↑ low		MIN	2	2	1.4	1.4
th Hold time			MIN	2	2.3	1.7	1.7
			MAIN	0	0.6	0.6	0.6
			MIN	0	0.5	0.6	0.6
tPLH	A or B	D A	MAY	4	3.9	4.1	4.4
tphl.	A or B	B or A	MAX	4.9	3.9	4.1	4.4
tPLH .	LEAB or LEBA	D 4	MAX	5	4.6	4.7	5.1
tphL	LEAB OF LEBA	B or A	MAX	5.2	4.6	4.7	5.1
tplH	CLKAB or CLKBA	D A	MAX	4.7	4.5	5	5.4
tphL .	CLKAB OF CLKBA	B or A	MAX	4.6	4.6	5	5.4
tPZH	- OEAB	В	MAX	5.5	4.2	5.2	5.6
tPZL	UEAB	В	MAX	5.8	4.4	5.2	5.6
tPHZ	- OEAB	В	MAN	6.2	5.3	4.4	4.7
tplz	UEAB	В	MAX	5.4	4.6	4.4	4.7
tPZH	OEBA	Α.	MAY	5.5	4.2	5.2	5.6
tPZL.	UEBA	A	MAX	5.8	4.4	5.2	5.6
tphz	OEBA	Δ.	MAN	6.2	5.3	4.4	4.7
tPLZ	UEBA	A	MAX	5.4	4.6	4.4	4.7

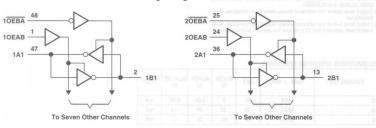
<sup>§</sup> Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

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### 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



Logic Diagram



#### **FUNCTION TABLE**

	INPUTS		
OPERATIO	OEAB	OEBA	
B data to A	L	L	
B data to A I A data to B	Н	L	
Isolation	L	Н	
A data to B	н	н	

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RECOMMENDED OPERATING CONDITIONS

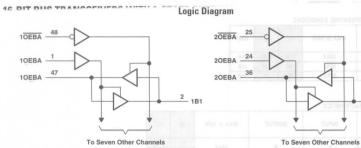
PARAMETER	MAX or MIN	AC	ACT	UNIT
lcc	MAX	0.08	0.08	mA
Іон	MAX	-24	-24	mA
lot	MAX	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AC	ACT
tPLH .	Other Channe	B To Sevin	MAY	6.8	8.5
tphl.	A	В	MAX	8.2	10.5
tPLH	D.		MAN	6.8	8.5
tPHL	В	A	MAX	8.2	10.5
tPZH	OEBA		MANY	7.9	9.1
tPZL	UEBA	A	MAX	9.4	10.9
tPHZ	0504		DOM:	9.2	11.9
tPLZ	OEBA	A	MAX	8.3	10.6
tPZH	0515	В	14434	7.3	8.9
tPZL	OEAB	В	MAX	9.1	10.5
tPHZ	OFAR		BAAN/	9	10.8
tPLZ	OEAB	В	MAX	8	9.6

UNIT: ns

FUNCTION TABLE



## FUNCTION TABLE (each 8-bit section)

INPUTS				
BA	OEAB	OPERATION		
	L	B data to A bus		
	Н	B data to A bus A data to B bus		
H	L	Isolation		
4	Н	A data to B bus		

### RECOMMENDED OPERATING CONDITIONS

KECOMMENDED OF	PERATING CONDITI	UNS		
PARAMETER	MAX or MIN	ABT	ACT	UNIT
Icc	MAX	35	0.08	mA
Іон	MAX	-32	-24	mA
lou	MAX	64	24	mA

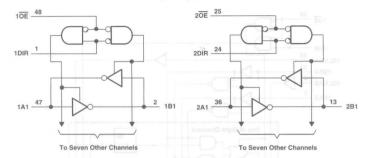
### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT
tPLH	A or B	D A	MAX	3.6	7.7
tphl.	A or B	B or A	MAX	4.3	8.6
tpzH	OEBA		MAX	4.9	9.5
tPZL	UEBA	A	MAX	6	11.1
tPHZ	OEBA		MAX	6	12
tPLZ	UEBA	A	MAX	5.4	10.7
tpzh	OEAB	В	MAX	4.9	9.3
tPZL	UEAB	В	MAX	6	10.6
tphz	OEAB	В	MAX	6	10.4
TPLZ	UEAB	В	IVIAX	5.4	9.5

UNIT: ns

## 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS ITZEGER AND REGISTRANSCEIVER WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE (each 8-bit section)

INP	UTS		
OE	DIR	OPERATION	
L	L.	B data to A bus	
L	H	A data to B bus	
H	×	Isolation	

RECOMMENDED OPERATING CONDITIONS

		T		I Commission	
PARAMETER	MAX or MIN	ABT	AC	ACT	UNIT
Icc	MAX	32	0.08	0.08	mA
Іон	MAX	-32	-24	-24	mA
lou	MAX	64	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	AC	ACT
tplh	4		1447	4.3	7.3	9.1
tphL .	A or B	B or A	MAX	3.9	8.6	10.5
tPZH	<u>OE</u>	4 0	MANY	5.5	8	9.8
tpzl	UE	A or B	MAX	6.3	9.9	11.5
tрнz	- OE	A or B	MAX	6.3	9.9	12.5
tPLZ	- UE	A OF D	IVIAA	4.2	9	11

# **Logic Diagram** 10E 1DIR 1CLKBA 55 1SBA 54 1CLKAB 2 1SAB One of Eight Channels 1D C1< 52 1B1 1D To Seven Other Channels 2DIR 2CLKBA 2SBA 31 2CLKAB 27 One of Eight Channels 1D C1< <u>42</u> 2B1 1D 1111

To Seven Other Channels

#### **FUNCTION TABLE**

	I/O	DATA		INPUTS					
OPERATION OR FUNCTION	B1 THRU B8	A1 THRU A8	SAB SBA		CLKBA	CLKAB	DIR	OE	
Store A, B unspecitied † Store B, A unspecitied †	Unspecified † Input	Input Unspecified †	X	X	X	X	X	X	
Store A and B data Isolation, hold storage	Input Input disabled	Input Input disabled	X	X	↑ H or L	↑ H or L	X	Н	
Real-time B data to A bus Stored B data to A bus	Input Input	Output Output	L	X	X H or L	X	L	L	
Real-time A data to B bus Stored A data to B bus	Output	Input	X	L	X	X H or I	Н	L	

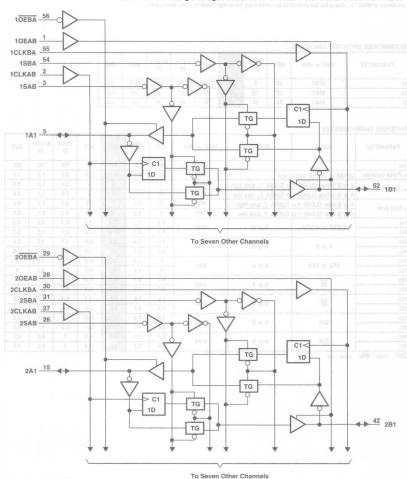
† The data output functions may be enabled or disabled by various signals at the  $\overline{OE}$  and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVTH 3V	AC	ACT	LVCH 3V	ALVCH 3V	AVC	UNIT
Icc	' MAX	32	5	0.08	0.08	0.02	0.04	0.04	mA
Іон	MAX	-32	-32	-24	-24	-24	-24	-12	mA
lou	MAX	64	64	24	24	24	24	12	mA

#### SWITCHING CHARACTERISTICS

SWITCHING CHAR	ACTERISTICS								- 6	
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	AC	ACT	LVCH 3V	ALVCH 3V	AVC
fmax			MIN	125	150	75	90	150	150	350
tw Pulse duration	CLKAB or CLKBA high o	rlow	MIN	4.3	3.3	6.5	5.5	3.3	3.3	1.4
. C	A or B before CLKAB ↑	B before CLKAB † or CLKBA †, data high		3	1.2	5	4	2.9	1.4	0.8
tsu Setup time	A or B before CLKAB ↑	or CLKBA ↑, data low	MIN	3	2	5	6	2.9	1.4	0.8
th Hold time	A or B after CLKAB ↑ or CLKBA ↑, data high		MIN	0	0.5	1	1.5	0.3	0.7	0.6
u noid time	A or B after CLKAB † or	or B after CLKAB ↑ or CLKBA ↑, data low		0	0.5	1	1.5	0.3	0.7	0.6
tplh	CLKAB or CLKBA	B or A	MAX	4.9	4.2	12.1	12.2	6.7	4.5	3.3
tphl.	CLAND OF CLANDA		IVIAA	4.7	4.2	11.9	12.3	6.7	4.5	3.3
tplh	A or B	B or A	MAN	3.9	3.4	9.5	10.6	5.7	3.9	2.6
tphL .	AOIB	B OF A	IVIAA	4.6	3.4	9.7	11.4	5.7	3.9	2.6
tplH	SAB or SBA	B or A	MAX	5	4.5	12.5	15.6	7.7	5.3	4
tphL .	SAB OF SBA	D OF A		5	4.5	13.1	16.7	7.7	5.3	4
tPZH	ŌĒ	A or B	MAX	5.5	4.3	10.5	11.9	6.9	5.1	4
tPZL	OE .	AUID	IVIAA	5.7	4.3	12.2	13.5	6.9	5.1	4
tPHZ	- OE	A or B	MAX	5.4	5.6	8.9	10.2	6.9	4.7	4.2
tPLZ	UE UE	AUID	IVIAA	4.5	5.4	8.6	9.9	6.9	4.7	4.2
tpzh	DIR	A or B	MAX	5.4	4.4	10.9	15.2	7.2	5.1	4.3
tPZL	JIN JIN	M Uf B	WAX	5.6	4.4	12.2	13.1	7.2	5.1	4.3
tPHZ	DIR	A or B	MAX	6.7	5.7	9.4	10.8	7	5.3	4.3
tPLZ	DIN >10	A UF B	IVIAX	5.9	5.2	8.8	10.4	7	5.3	4.3



#### **FUNCTION TABLE**

	1/0 †	DATA			JTS	INP		
OPERATION OR FUNCTION	B1-B8	A1-A8	SBA	SAB	CLKBA	CLKAB	OEBA	OEAB
Isolation Store A and B data	Input Input	Input Input	X	X	L	L	H	L
Store A, hold B Store A in both registers	Unspecified‡ Output	Input Input	X	X X‡	Ļ	÷	H	Х
Hold A, store B Store B in both registers	Input Input	Unspecified‡ Output	X X‡	X	<b>^</b>	L	X	L
Real-time B data to A bus Store B data to A bus	Input Input	Output Output	L	X	X L	X	L	L
Real-time A data to B bus Store A data to B bus	Output Output	Input Input	X	L H	×	X	H	H
Store A data to B bus and Store B data to A bus	Output	Output	Н	Н	L	L	L	Н

The data-output functions may be enabled or disabled by a variety of level combinations at DEAB or DEBA. Data-input functions are always enabled; i.e., data at the bus terminats is stored on every low-to-high transition of the clock inputs.

\$ select contril = L. clocks can occur simultaneously.

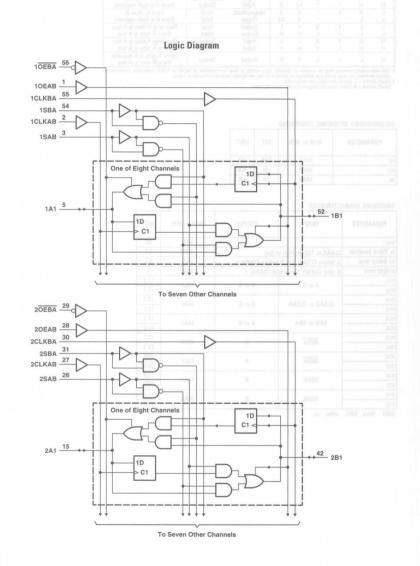
Select control = I. clocks must be staggered to load both registers.

#### RECOMMENDED OPERATING CONDITIONS

THE OUTTHE THE OT ET	T TOTAL TOTAL	_	_
PARAMETER	MAX or MIN	ACT	UNIT
Icc	MAX	0.08	mA
Іон	MAX	-24	mA
lor	MAX	24	mA

SWITCHING CHAP				
PARAMETER	INPUT	OUTPUT	MAX or MIN	ACT
fmax	<del></del>		MIN	90
tw Pulse duration	CLKAB or CLKBA high or	low	MIN	5.5
tsu Setup time	A before CLKAB ↑ or B b	efore CLKBA ↑	MIN	5.3
th Hold time	A after CLKAB † or B after	er CLKBA ↑	MIN	1
tPLH	A or B	B or A	MAX	11.3
tPHL .	M UT D	D OF A	MAX	11.9
tplh	CLKAB or CLKBA	A or B	MAX	13.7
tphl.	CLNAD UI CLNDA	AUID	IVIAA	13.6
tplh	SAB or SBA	A or B	MAX	17.3
tphl .	SAD UI SDA	AUID	IVIAA	17.8
tрzн	- OEBA	A	MAX	12.3
tPZL	UEDA	A	IVIAA	13.9
tphz	DEBA	А	MAX	10.6
tPLZ	UEDA	A	IVIAA	10.8
tPZH	OEAB	В	MAX	11.9
tpzi	UEAD	В	MAX	13.5
tрнz	OEAB	В	MAX	11.4
tPLZ	UEAD	В	MAX	11.6

## 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS



#### **FUNCTION TABLE**

		INP	UTS			DATA	I/O†	
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
L	H	HorL	HorL	X	X	Input	Input	Isolation
L	H	+	1	X	X	Input	Input	Store A and B data
X	H	+	HorL	X	X	Input	Unspecified ‡	Store A, hold B
H	H	+	1	X±	X	Input	Output	Store A in both registers
L	X	HorL	1	X	X	Unspecified ‡	Input	Hold A, store B
L	L	+	+	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	HorL	X	Н	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	HorL	X	H	X	Input	Output	Store A data to B bus
Н	L	H or L	H or L	Н	Н	Output	Output	Stored A data to B bus and stored B data A bus

<sup>†</sup> The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or  $\overline{\text{OEBA}}$  inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition of the clock

inputs.

\$ Select control = L; clocks can occur simultaneously.

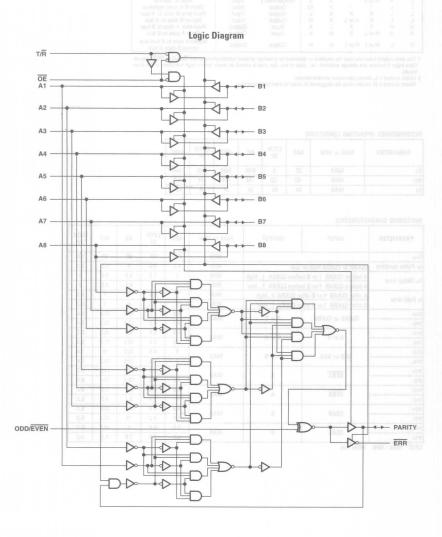
Select control = H; clocks must be staggered in order to load both registers.

#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVTH 3V	AC	ACT	LVCH 3V	UNIT
Icc	MAX	32	5	0.08	0.08	0.02	mA
Гон	MAX	-32	-32	-24	-24	-24	mA
lor	MAX	64	64	24	24	24	mA

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	AC	ACT	LVCH 3V
fmax			MIN	125	150	95	90	150
tw Pulse duration	CLKAB or CLKBA high or I	ow	MIN	4.3	3.3	5	5.5	3.3
. Catua tima	A before CLKAB † or B be	fore CLKBA ↑, high	MIN	3	1.2	4.5	4.5	3
tsu Setup time	A before CLKAB ↑ or B be	fore CLKBA ↑, low	MIN	3	2	4.5	4.5	3
th Hold time	A after CLKAB ↑ or B afte	MIN	0	0.5	0	1	0.2	
th mold time	A after CLKAB ↑ or B afte	MIN	0	0.5	0	1	0.2	
tplh	CLKAB or CLKBA	A or B	MAX	4.9	4.2	12.2	12.3	6.4
tphl .	CLKAB OF CLKBA	A or B	IVIAX	4.7	4.2	12.3	12.3	6.4
tPLH	A or B	B or A	MAX	3.9	3.4	9.9	10.5	6.3
tphl.	A OF B	B or A	IVIAX	4.6	3.4	10.2	11.6	6.3
tplh	SAB or SBA	A or B	MANY	5	4.5	13.8	16	7.4
tphL .	SAB OF SBA	A or b	MAX	5	4.5	13.8	16.9	7.4
tPZH	OEBA	А	MAN	5	4.3	10.7	11.7	6.3
tPZL	UEBA		MAX	5.3	4.3	13.2	13.4	6.3
tPHZ	OEBA	A	MAY	4.9	5.6	8.8	9.5	6.2
tPLZ	UEBA	A	MAX	4	5.4	8.7	9.2	6.2
tpzh	OEAB	D.	MAN	4.2	4.2	10.5	10.8	6.3
tpzl	UEAB	В	MAX	4.6	4.2	13	12.4	6.3
tPHZ	OFAR	D	MAY	5.9	5.5	8	10.5	6.2
tPLZ	OEAB B		MAX	5.2	5.5	7.8	9.9	6.2

### 16-BIT TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS



#### FUNCTION TABLE (each 8-bit section)

NUMBER OF A OR B		INI	PUTS	INF	UT/OUTPUT		OUTPUTS
NPUTS THAT ARE HIGH	ŌE	T/R	ODD/EVEN	-	PARITY	ERR	OUTPUT MODE
	L	Н	Н	-	Н	Z	Transmit
	L	H	L	1	Las	Z	Transmit
00100	L	L	H		H	JOH	Receive
0, 2, 4, 6, 8	L	L	H	-	L	L	Receive
	L	L	L		H	L	Receive
	L	L	L		L 82	H	Receive
	L	Н	Н		L	Z	Transmit
	L	H	L	-	H	Z	Transmit
1 2 5 7	L	L	H		H	L	Receive
1, 3, 5, 7	L	L	. Н		Ľ od	H	Receive
	L	L	L		H	H	Receive
	L	L	L		L	L	Receive
Don't care	Н	X	X		Z	Z	Z

#### RECOMMENDED OPERATING CONDITIONS

		1	_	
PARAMETER	MAX or MIN	ABT	ACT	UNIT
Icc	MAX	36	0.08	mA
Іон	MAX	-32	-24	mA
lou	MAX	64	24	mA

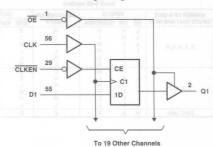
#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT
tplh	A D	D A	1447	4.1	10.7
tphl .	A or B	B or A	MAX	4.3	10.6
tplh	A D	DADITY	MAN	6.7	14.3
tphl .	A or B	PARITY	MAX	6.1	14.3
tplh	ODD / EVEN	PARITY, ERR	MAN	6.7	13.7
tрнL	ODD / EVEN	PARILY, ERR	MAX	6.1	14.1
tPLH	В	ERR	MAN	6.7	14.6
tphl.	В	ERR	MAX	6.1	14.7
tPLH .	DADITY	ERR	MAN	6.7	13.8
tphl.	PARITY	ERR	MAX	6.1	14.2
tPZH	ŌĒ	A D	MAN	5.6	11.3
tPZL	UE	A or B	MAX	6	13
tрнz	ŌĒ	A or B	EANY	5.4	11.2
tplZ	UE	AOFB	MAX	4.3	10.5
tpzh	ŌE	PARITY, ERR	1467	5.6	11.3
tPZL	UE	FARILY, ERR	MAX	6	13
tphz	ŌĒ	DADITY FDD	1 1/2	5.4	11.2
tPLZ	UE	PARITY, ERR	MAX	4.3	10.5

UNIT: ns

	10.5	4.3	181

### 20-BIT FLIP-FLOP WITH 3-STATE OUTPUTS



#### FUNCTION TABLE (each filp-flop)

	INPL	OUTPUT		
ŌE	CLKEN	CLK	D	Q
L	Н	X	Н	90
L	L	<b>†</b>	H	H
L	L	1	L	L
L	L	L	X	90
Н	X	X	X	Z

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
Icc	MAX	0.04	mA
Іон	MAX	-24	mA
lou	MAX	24	mA

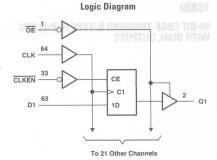
### SWITCHING CHARACTERISTICS

SWITCHING CHAI	ACTEMISTICS		1 1 1 1 1	
PARAMETER	R INPUT OUTPUT		MAX or MIN	ALVCH 3V
fmax		5.0	MIN	150
tw Pulse duration	CLK high or low		MIN	3.3
. C-1 1	Data before CLK ↑	MIN	3.1	
tsu Setup time	CLKEN before CLK	MIN	2.7	
th Hold time	Data after CLK ↑		MIN	0
to Hold time	CLKEN after CLK ↑	MIN	0	
tPLH .	CLK	0	MAX	4.3
tPHL .	CLK	u	IVIAA	4.3
tPZH	ŌĒ	0	MAX	4.8
tPZL	UE	u	IVIAX	4.8
tPHZ	ŌĒ	0	MAN	4.4
tPLZ	Z OE		MAX	4.4

### 16722

### 22-BIT FLIP-FLOP WITH 3-STATE OUTPUTS





FUNCTION TABLE (each filp-flop)

	INPL	INPUTS				
ŌĒ	CLKEN	CLK	D	Q		
L	Н	X	X	QO		
L	L	1	H	Н		
L	L	1	L	L		
L	L	LorH	X	Qo		
Н	×	X	X	Z		



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AVC 3V	UNIT
Icc	MAX	0.04	mA
Іон	MAX	-12	mA
lou	MAX	12	mA

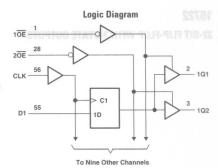
#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT OUTPUT		MAX or MIN	AVC 3V
fmax			MIN	150
tw Pulse duration	CLK high or low		MIN	2.8
	Data before CLK 1	MIN		
tsu Setup tîme	CLKEN before CLK 1	MIN		
th Hold time	Data after CLK ↑		MIN	0
th Hold time	CLKEN after CLK ↑	MIN	1.2	
tplh .	CLK	211		2.6
tPHL .	ULK	a	MAX	2.6
tpzh	ŌE	0	MAX	4.3
tpzl	- UE	۵	IVIAX	4.3
tPHZ	ŌĒ	Q	MAX	3.4
tPLZ	DE OE		WAX	3.4

### 16820

# 10-BIT EDGE-TRIGGERD D-TYPE FLIP-FLOPS WITH DUAL OUTPUTS





FUNCTION TABLE (each filp-flop)

1	NPUTS	OUTPUT	
OE <sub>n</sub> †	CLK	D	Qn†
L	*	Н	Н
L	*	L	L
L	L	X	Qn
LF	V	V	7

† n = 1, 2

UNCTION TABLE

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
lcc	MAX	0.04	mA
Іон	MAX	-24	mA
lou	MAX	24	mA

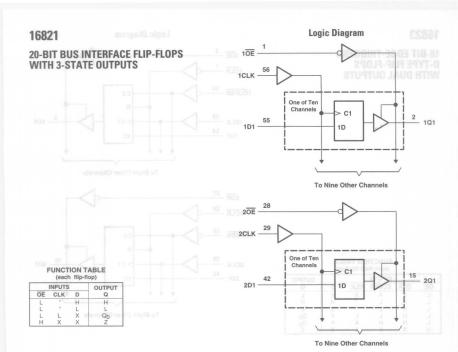
RECOMMENDED DESATING CONDITIONS

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V	
fmax		7.0	MIN	150	
tw Pulse duration	CLK high or low	-	MIN	3.3	
tsu Setup time	Data before CLK ↑	MIN	1.4		
th Hold time	Data after CLK ↑		MIN	1	
tPLH	CLK	_	MAX	4.8	
tPHL .	ULK	Q	WAX	4.8	
tpzh	ŌĒ		35,444	5	
tPZL	UE	۵	MAX	5	
tPHZ	ŌĒ		MAX	4.5	
tPLZ	UE	a	MAX	4.5	

Tac Sergy time CAREN Serger CAR T CAREN Serger CAR T CAREN Serger CAR T CAREN Serger CAR T CAREN SERV CAR T CAREN CAR T CAREN CAR T CAREN CAR T CAREN CAR T CAREN CAR T CAREN CAR T CAREN CAREN CAREN CAREN CAREN CAREN CAR

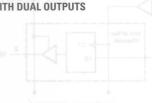
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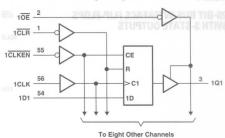


RECOMMENDED OF	PERATING CONDITI	ONS							
PARAMETER	MAX or MIN	ABT	ALVTH 3V	ACT	ALVCH 3V	UNIT			
Icc	MAX	89	5	0.08	0.04	mA			
Іон	MAX	-32	-32	-24	-24	mA			
lou	MAX	64	64	24	24	mA			

PARAMETER	INPUT	ŧΙΑ	OUTPUT	нтва	MAX or MIN	ABT	ALVTH 3V	ACT	ALVCH 3V	TORNO	
fmax	621	00	dr.	00	MIN	150	150	70	150		
tw Pulse duration	CLK high or low	1.5	N. Call	2.5	MIN	3.3	1.5	7	3.3	well RUD	
. C-t ti	Data before CLK †	, low		8.8	MIN	1.8	1.5	7.5	3.4	wol to right XUD	
tsu Setup time	Data before CLK ↑	, high	DEV.	8.1	MIN	1.8	1.5	7.5	3.4	CLS inactive	
	Data after CLK ↑,	Data after CLK ↑, high			MIN	1.3	1	0.5	0.0	Data high helps	
th Hold time	Data after CLK ↑, low			11	MIN	1.3	1	0.5	0 13	Data low bators	
tplh	CLK	ε	a		MAX	6.1	3.5	13.4	4.5	and with MSSUS	
tphl .	CLK	i i	u	5.1	WAX	5.4	3.5	14	4.5	Data High after I	
tpzh	ŌĒ	0	Ω	5.1	MAX	5.7	4.1	11.9	5.1	Data low after D	
tPZL	1.3	1.3	u	3.0	WAX	5.6	3.6	14.7	5.1	enter seed M35/15	
tPHZ	ŌĒ	121	Q	3.1	MAX	6.5	4.8	10.7	4.6		
tPLZ	UE	120	u	3	IVIAA	7.1	4.8	10	4.6	2.13	
UNIT fmax: MHz	other: ns									100	

18-BIT EDGE-TRIGGERD **D-TYPE FLIP-FLOPS** WITH DUAL OUTPUTS





FUNCTION TABLE (each 9-bit filp-flop) INPUTS OUTPUT

20E -	27			-d>	1
	28				
2CLKEN	30		CE		
2CLK -	42		− R −>C1		15 2Q1
2D1 —	,	ļ	1D	000	1098 10 80
		To Eig	ht Other Ch	annels	

CLKEN Q<sub>0</sub> Q<sub>0</sub> Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ABTH	AC	ACT	ALVCH 3V	UNIT
Icc	MAX	80	80	0.08	0.08	0.04	mA
Іон	MAX	-32	-32	-24	-24	-24	mA
lor	MAX	64	64	24	24	24	mA

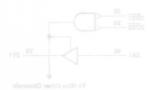
SWITCHING CHARACTERISTICS

SWITCHING CHAP	ACTERISTICS			_				GH
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ABTH	AC	ACT	ALVCH 3V
fmax		180	MIN	150	150	115	90	150
tw Pulse duration	CLR low	E.E	MIN	3.3	3.3	3.3	3.3	3.3
tw Pulse duration	CLK high or low	4.5	MIN	3.3	3.3	4.4	5.5	3.3
	CLR inactive	3.5	MIN	1.6	1.6	0.6	0.5	0.8
	Data high befor	e CLK ↑	MIN	1.7	1.7	5	7	111
tsu Setup time	Data low before CLK ↑	CLK ↑	MIN	1.7	1.7	5	7	1.3
CLKEN low before CL		ore CLK ↑	MIN	2.8	2.8	4.2	3.5	1.5
	Data high after	Data high after CLK ↑		1.2	1.2	1.3	0.5	0.8
th Hold time	Data low after (	CLK ↑	MIN	1.2	1.2	1.3	0.5	0.5
	CLKEN low after	r CLK ↑	MIN	0.6	0.6	1.4	2.5	0.4
tplH	OLK	8	MANY	6.8	6.8	12	12.1	4.5
tphl.	CLK	۵	MAX	6	6	12.7	12.9	4.5
tPLH .	CLR	0	1447	-	-		-	4.6
tphl.	CLR	u	MAX	6.1	6.7	11	12.5	4.6
tPZH	ŌĒ		1441/	4.9	4.9	9.7	10.7	4.8
tPZL	OE OE	a	MAX	5.5	5.5	11.8	12.8	4.8
tPHZ	ŌĒ	0	MANY	6.1	6.1	9.3	10.3	4.5
tPLZ	I OF	Q	MAX	8.7	8.7	8.6	9.4	4.5

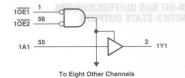
### 16825

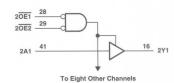
# 18-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS





**Logic Diagram** 





FUNCTION TABLE (each 9-bit section)

- 10	INPUTS		OUTPUT
OE1	OE2	Α	Υ
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

PUNCTION TABLE

#### RECOMMENDED OPERATING CONDITIONS

HEGGINITE TABLE O	LIBITING GOITBITI	0140			
PARAMETER	MAX or MIN	ABT	ACT	ALVCH 3V	UNIT
Icc	MAX	32	0.08	0.04	mA
Іон	MAX	-32	-24	-24	mA
lo <sub>L</sub>	MAX	64	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT	ALVCH 3V
tplH			MAN	3.9	10.5	3.4
tPHL .	A	Y	MAX	4.4	10.3	3.4
tPZH	ŌĒ		MAX	6.1	11	4.7
tPZL	UE	WIA HT		6	13.2	4.7
tPHZ	ŌĒ	E v	MAX	6.9	11.5	4.5
tPLZ	UE	Y	MAX	6.6	10.6	4.5

UNIT: ns

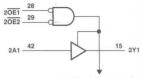


Logic Diagram

6825

To Nine Other Channels





To Nine Other Channels

FUNCTION TABLE (mich 9-bit section)

#### FUNCTION TABLE (each 10-bit section)

INPUTS			OUTPUT
OE1	OE2	Α	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	Н	X	Z

ECONOMERATION DESIGNATIONS CONDITION

#### RECOMMENDED OPERATING CONDITIONS

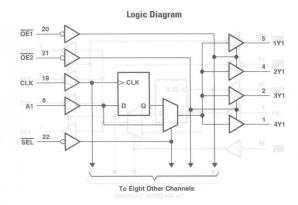
PARAMETER	MAX or MIN	ABT	ALVTH 3V	ACT	ALVCH 3V	AVC	UNIT
Icc	MAX	32	6	0.08	0.04	0.04	mA
Іон	MAX	-32	-32	-24	-24	-12	mA
lor	MAX	64	64	24	24	12	mA

SWITCHING CHARACTERISTICS

SWITCHING CHARAI	TERISTICS	1.3	1.0					
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ALVTH 3V	ACT	ALVCH 3V	AVC
tPLH			MAY	3.4	3	-11	3.4	1.7
tphl .	A	Y	MAX	4.2	2.8	10.8	3.4	1.7
tPZH	ŌE	v	MAX	5.6	3.9	11.7	4.7	5.1
tPZL	ÜE	UE Y		5.5	3.4	14	4.7	5.1
tPHZ	ŌE			6.6	5.8	12.4	4.5	4.7
tPLZ	0E	Y Y	MAX	6.1	4.6	11.5	4.5	4.7

UNIT: ns

### 1-TO-4 ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS INCOME 223600A 4-07-1



**FUNCTION TABLE** 

INPUTS				OUTPUT	
OE	SEL	CLK	A	Y	
Н	X	X	X	Z	
L	H	X	L	L	
L	H	X	H	H	
L	L	1	L	L	
L	L		H	H	

RECOMMENDED OPERATING CONDITIONS

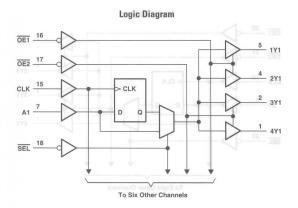
PARAMETER	MAX or MIN	ALVCH 3V	UNIT
lcc	MAX	0.04	mA
1он	MAX	-24	mA
lou	MAX	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
fmax			MIN	150
tw Pulse duration	CLK high or low		MIN	3.3
tsu Setup time	A data before CLK ↑		MIN	1.6
th Hold time	A data after CLK ↑		MIN	1.1
tPLH .	A	Y	MAX	3.6
tphl .				3.6
tPLH	CLK	Y	MAX	3.9
tphl .				3.9
tPLH	SEL	Y	MAX	4.4
tPHL	SEL			4.4
tРZH	ŌĒ	Υ	MAX	4.3
tPZL	UE			4.3
tрнz	ŌĒ	Y	MAX	4.5
tPLZ	OE OE			4.5

# 16831

# 1-TO-4 ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS MORST 2038 223800A N-DT-1

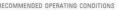


SUBJECT MORTHWAY

SUBCRISTON DULY STON ASSURANCE

manufacture and the state of the second

	INP	OUTPUT		
OE	SEL	CLK	Α	Υ
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	Н
L	L	+	L	L
L	L		Н	Н



RECOMMENDED OF	PERATING CONDIT	IONS		
PARAMETER	MAX or MIN	ALVCH 3V	UNIT	
Icc	MAX	0.04	mA	
Іон	MAX	-24	mA	
lou	MAX	24	mA	

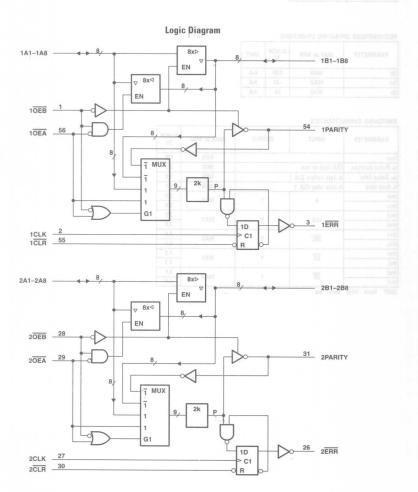


# SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
fmax			MIN	150
tw Pulse duration	CLK high or low		MIN	3.3
tsu Setup time	A data before CLK	( †	MIN	1.6
th Hold time	A data after CLK 1		MIN	8 1.1
tPLH	A	V	MAX	3.6
tphl.	7 A	1	IVIAA	3.6
tplh	CIV	ν	MAX	3.9
tphl .	CLK	of a	IVIAA	3.9
tplh	SEL	v 10-4	MAX	4.4
tphl.	SEL	La al	IVIAA	4.4
tPZH	ŌĒ	V	MAX	4.3
tPZL.	UE	1	IVIAX	4.3
tPHZ	ŌĒ	Y	MAN	4.5
tPLZ	UE	1	MAX	4.5

# UNIT fmax: MHz other: ns





п	п	H	↑ ↑	Odd	^	1	_	_	H	isolations		
Н	Н	Н	1	Odd	×	X	X	4	2	2	н	Isolation§

NA = not applicable, NC = no change, X = don't care

† Output states shown assume ERR was previously high.

† Summation of high-level inputs includes PARITY along with Bi inputs.

§ In this mode, ERR (when clocked) shows inverted pannity of the A bus.

### **ERROE-FLAG FUNCTION TABLE**

INP	UTS	INTERNAL TO DEVICE	OUTPUT PRE-STATE	ОИТРИТ	FUNCTION	
CLR	CLK	POINT P	ERR <sub>n-1</sub> †	ERR		
Н	1	Н	Н	Н		
H	1	X ster	Other Johnson	A OF	Sample	
H	T	L	X	L		
L	X	X	X	Н	Clear	

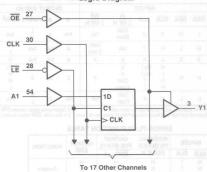
† State of ERR before any changes at CLR, CLK, or point P

# RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ACT	UNIT
Icc	MAX	36	0.08	mA
Іон	MAX	-32	-24	mA
lou	MAX	64	24	mA

INPUT					BE VE		
000000000000000000000000000000000000000	OUTPUT	MAX or MIN	ABT	ACT	0.0 40.0		
					1. 35-		
		MIN	-	To the same of the	7 1 kg		
2007			-				
				MEDICAL PROPERTY.	1		
		R MIN		1.5	1		
A data before CLK ↑	, OEA		-				
A data after CLK ↑,	A port or OEA	O MIN	100 0000000	(ASTRONOMICS)	BUTPUT		
A or B	B or A	MAX	10000	NUMBER OF STREET			
7010	DUIA	041	4.3				
۸	PARITY	MAY	6.7	13.5			
^	1 Aut 1	I I I I	6.1	13.8			
OFR as OFA	A and D	MANY	5.6	11.2			
UEB OF UEA	AUID	IVIAA	6	13	Heart St.		
0FD 0FA	A D	CARAN	5.4	10.8			
UED OF UEA	AUID	WIAA	4.3	10.1			
CLK, CLR	<u> </u>	CAAN	4.6	15.8	Medid		
CLK	Enn	IVIAA	3.9	11.6			
OFP.	DADITY	MAN	6.7				
UEB	PARITY	MAX	6.1		1		
054	DADITY	Takes .	6.7	13.2			
UEA	PARITY	MAX	6.1	13.6	1 Y		
		10	5.7	9.5			
OFR	PARITY	MAX	6.5	10.7	Y		
-	and an annual of the	1	4.7	10.2	1		
UEB	PARITY	MAX	4.1	9.7	Y		
		24	5.7	-	1		
OEA	PARITY	MAX	6.5		Υ		
			4.7		1		
OEA	PARITY	MAX	4.1		1		
	A data before CLK ↑ A data before CLK ↑ A data after CLK ↑ A or B  A  OEB or OEA  CLK, CLR	CLR   low	CLR low         MIN           A data before CLK ↑, A port         A data before CLK ↑, CLR           A data before CLK ↑, DEA         MIN           A data sefore CLK ↑, DEA         MIN           A data sefore CLK ↑, A port or OEA         MIN           A or B         B or A         MAX           A         PARITY         MAX           OEB or OEA         A or B         MAX           OEB or OEA         A or B         MAX           CLK, CLR         ERR         MAX           OEB         PARITY         MAX           OEA         PARITY         MAX           OEB         PARITY         MAX	CLR   Iow	CLR   CLK   CLK   CLK	CLK high or low         MIN         3         4           CLR low         -         4         4           A data before CLK ↑, A port         MIN         1         1.5           A data before CLK ↑, CLR         MIN         0         0           A data after CLK ↑, A port or OEA         MIN         0         0           A or B         B or A         MAX         4.1         10.4           A. OR B         B or A         MAX         6.7         13.5           6.1         13.8         6.1         13.8           0EB or OEA         A or B         MAX         5.6         11.2           6         13         4.3         10.1         10.8           0EB or OEA         A or B         MAX         4.3         10.1           CLK, CLR         ERR         MAX         4.6         15.8           CLK         ERR         MAX         3.9         11.6           OEB         PARITY         MAX         6.7         -           0EB         PARITY         MAX         6.7         13.2           0EB         PARITY         MAX         6.5         10.7           0EB         PARITY	CLK high or low         MIN         3         4           CLR low         4.5         -         4           A data before CLK ↑, CLR         MIN         1         1.5           A data after CLK ↑, CER         5         -           A data after CLK ↑, A port or OEA         MIN         0         0           A or B         B or A         MAX         4.1         10.4           A or B         B or A         MAX         6.7         13.5           6.1         13.8         0.1         13.8           0EB or OEA         A or B         MAX         5.6         11.2           6         13         0.1         13.8         0.1         13.8           0EB or OEA         A or B         MAX         5.4         10.8         0.1         10.8           0EB or OEA         A or B         MAX         4.3         10.1         0.1         10.8         0.1         10.8         0.1         10.8         0.1         10.8         0.1         10.8         0.1         10.8         0.1         10.8         0.1         10.8         0.1         10.8         0.1         10.8         0.1         10.8         0.1         10.8         0.1

# **16-BIT UNIVERSAL BUS DRIVER** WITH 3-STATE OUTPUTS



## **FUNCTION TABLE**

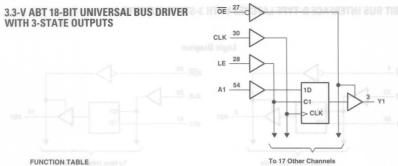
	INP	OUTPUT		
OE	LE	CLK	Α	Y
Н	X	X	X	Z
L	L	X	L	L
L	L	X	H	Н
L	H	1	L	L
L	H	+	H	H
L	H	H	X	Yot
L	H	L	X	Yo‡

Output level before the indicated steady-state input conditions were established, provided that CLK is high before LE goes high
 Output level before the indicated steady-state input conditions were established

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVC 3V	AVC 3V	UNIT
Icc	MAX	0.04	0.04	mA
Іон	MAX	-24	-12	mA
lor	MAX	24	12	mA

PARAMETER	INPUT	ОИТРИТ	MAX or MIN	ALVC 3V	AVC 3V
fmax			MIN	150	150
tw Pulse duration	LE low		MIN	3.3	3.3
tw ruise duration	CLK high or low		MIN	3.3	3.3
	Data before CLK ↑		MIN	1.7	0.7
tsu Setup time	Data before LE ↑, C	LK high	MIN	1.9	1
	Data before LE ↑, C		IVIIIV	1.5	1
	A data after CLK ↑	201	MIN	0.7	0.9
th Hold time	Data after LE ↑, CLI	K high	TAIN!	0.9	1.4
	Data after LE ↑, CLI	K low	MIN	0.9	1.3
tPLH		Y		3.6	2.5
tPHL .	Α	T	MAX	3.6	2.5
tPLH	LE	Y	100	4.9	4
tPHL .	- LE	Y	MAX	4.9	4
tPLH	0114		1111	4.6	3.1
tphL .	CLK	Y	MAX	4.6	3.1
tPZH	ŌE	Y	1444	5	6.2
tPZL	OE OE	Y	MAX	5	6.2
tPHZ	ŌĒ		1 1 1 1	4.5	5.3
tPLZ	- UE	Y	MAX	4.5	5.3



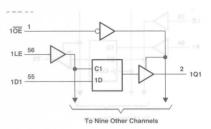
	INP	UTS		OUTPUT
OE	LE	CLK	Α	Y
Н	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	*	L	L
L	L	+	H	H
L	L	H	X	Yot
L	L	L	X	Yo‡

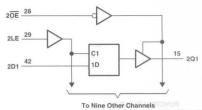
Output level before the indicated steady-state input conditions were established, provided that CLK was high before LE went low.
 Output level before the indicated steady-state input conditions were established

PARAMETER	MAX or MIN	LVTH 3V	ALVC 3V	ALVCH 3V	AVC 3V	UNIT
Icc	MAX	5	0.04	0.04	0.04	mA
Іон	MAX	-32	-24	-24	-12	mA
lor	MAX	64	24	24	12	mA

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	ALVC 3V	ALVCH 3V	AVC 3V
fmax			MIN	150	150	150	150
tw Pulse duration	LE low		MIN	3.3	3.3	3.3	3.3
tw ruise duration	CLK high or low		MIN	3.3	3.3	3.3	3,3
	Data before CLK ↑	HSMIA	MIN	2.1	1.7	1.7	0.7
tsu Setup time	Data before LE 1, CI	K high	MIN	2.3	1.5	1.5	0.8
	Data before LE ↓, CI	K low	MIN	1.5	1	1	0.5
	A data after CLK ↑		MIN	1	0.7	0.7	1.3
th Hold time	Data after LE 1, CLK	high	MIN	0.8	1.4	1.4	1.6
	Data after LE 1, CLK	low	MIN	0.8	1.4	1.4	1.4
tplh -	A	Y	MAX	3.7	3.6	3.6	2.5
tрнL	7 A	1		3.7	3.6	3.6	2.5
tPLH .	LE	E y	MAX	5.1	4.2	4.2	3.8
tphl.			IVIAA	5.1	4.2	4.2	3.8
tplh	CLK	8 y 8	MAX	5.1	4.5	4.5	3.1
tPHL	ULK	44	1417-04	5.1	4.5	4.5	3.1
tpzh	ŌĒ	Ty	MAX	4.6	4.6	4.6	6.2
tPZL	UE	1 -	1417-07	4.6	4.6	4.6	6.2
tPHZ	ŌĒ	Y	MAX	5.8	3.9	3.9	5.3
tPLZ	UE UE	Y	MAX	5.8	3.9	3.9	5.3

UNIT fmax: MHz other: ns





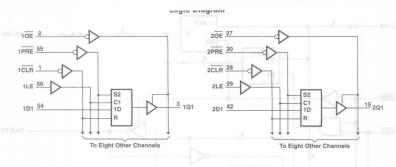
### **FUNCTION TABLE** (each 10-bit latch)

	NPUTS		OUTPUT
ŌĒ	LE	D	Q
L	Н	Н	Н
L	H	L	L
L	L	X	Qn
H	X	X	Z

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ACT	ALVCH 3V	UNIT
lcc	MAX	89	0.08	0.04	mA
Іон	MAX	-32	-24	-24	mA
lou	MAX	64	24	24	mA

INPUT	OUTPUT	1.5	MAX or MIN	ABT	ACT	ALVCH 3V
LE high or low			MIN	4	4	3.3
Data before LE ↓	1.00	10	MIN	1	1.5	1.1
Data after LE ↓, high		211	MIN	2	3	1.1
Data after LE 1, low	7.1	200	MIN	2	4.5	1.1
D D	10 ax	MAN	5	11.8	3.9	
			IVIAA	5.1	12.2	3.9
15			MAN	5	12.7	4.3
- LE	s u	5,5	IVIAX	5	12.7	4.3
05	0	-	MAN	5.7	11.3	4.9
UE	g u	2.5	MAX	5.6	13.7	4.9
OE .	0	9.9	MANY	6.5	10.2	4.1
T UE	U	0,0	IVIAX	7.1	9.6	4.1
	LE high or low  Data before LE ↓  Data after LE ↓, high  Data after LE ↓, low	LE high or low Data before LE 1 Data after LE 1, high Data after LE 1, low D LE Q OE Q	INPUT OUTPUT  LE high or low Data before LE ↓ Data after LE ↓, high Data after LE ↓, low  D  LE  Q  OE  Q	INPUT	INPUT	INPUT   OUTPUT   MAX or MIN   ABT   ACT



# FUNCTION TABLE (each 9-bit latch)

	INPUTS							
PRE	CLR	OE	LE	D	Q			
L	X	L	×	×	Н			
Н	L	L	X	×	L			
H	H	L	H	L	L			
H	H	L	H	H	Н			
Н	H	L	L	X	Qn			
X	X	H	X	X	Z			

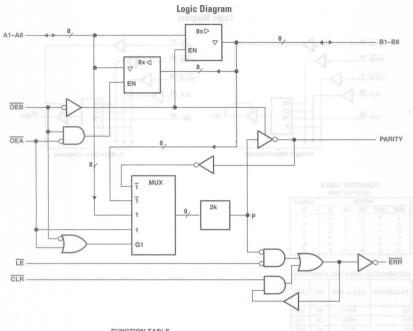
## RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
Icc	MAX	85	mA
Іон	MAX	-32	mA
lou	MAX	64	mA

### SWITCHING CHARACTERISTICS

SWITCHING CHARA	300,011 0000			
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
tw Pulse duration	CLF	Rlow	VI 100 NO. 10	3.3
	PRE	low	MIN	3.3
	LE	high		3.3
tsu Setup time	Data befor	e LE ↓, high	MIN	0.9
	Data befor	re LE ↓, low	IVIIIV	0.6
th Hold time	Data after	r LE ↓, high	MIN	1.7
	Data afte	r LE ↓, low	MILIA	1.8
tplh	D	0	MAX	4.8
tPHL .	U	u	IVIAX	4.8
tPLH .	LE	0	MAX	5.9
tPHL .	LE	u	WAX	5.3
tPLH .	PRE	0	MAX	6.1
tPHL .	FNE	u	IVIAX	5
tPLH	CLR	0	MAX	5.4
tPHL .	CLN	u	IVIAA	6
tP2H	0E	0	MAX	5.4
tPZL	UE	u u	WAX	5.8
tPHZ	0E	0	MAX	6.3
tPLZ	UE	u	IVIAA	5.2

# DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS AN ASHATAL BEYT-G SOARRETM AUS TIB-BE



### **FUNCTION TABLE**

		- 1	NPUT	S		0	UTPU	IT AND I/O	Os	
OEB	ŌEĀ	CLR	LE	Ai Σ OF H	Bi† Σ OF H	Α	В	PARITY	ERR‡	FUNCTION
L	Н	X	X	Odd Even	NA	NA	Α	L	NA	A data to B bus and generate parity
Н	L	Н	L	NA	Odd Even	В	NA	NA	H	B data to A bus and check parity
Н	L	H	Н	NA	X	X	NA	NA	NC	Store error flag
X	X	L	Н	X	X	X	NA	NA	Н	Clear error flag register
Н	Н	H L X	H	X X L Odd H Even	×	Z	Z	Z	NC H H L	Isolation§ (parity check)
L	L	X	×	Odd Even	NA	NA	Α	H	NA	A data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
² Cutput states shown assume ERR was previously high.
§ In this mode, ERR (when clocked) shows inverted panrity of the A bus.

# ERROR-FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT	OUTPUT	FUNCTION
CLR	LE	POINT P	ERR <sub>n-1</sub> †	ERR	
L	L	L H	×	L H	Pass
Н	L	L X H	X L H	L L H	Sample
L	Н	X	X	Н	Clear
н	Н	X	L	L	Store

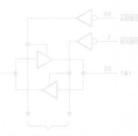
† State of ERR before changes at CLR, LE, or point P

PARAMETER	MAX or MIN	ABT	UNIT
Icc	MAX	40	mA
Іон	MAX	-32	mA
lou	MAX	64	mA

O-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUT

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
tw Pulse duration	LE high or low			8.5
tw ruise duration	CLR low		- BA301	4
tsu Setup time	A, B and PARITY befo	re LE ↓	MIN	10
tsu Setup time	CLR before LE ↓			0
th Hold time	A, B and PARITY after LE ↓		MIN	0
in nota time				0
tplh	A or B	B or A	MAX	4.1
tPHL .	AOIB	D OF A		4.3
tPLH	A or OE	PARITY	MAX	7.1
tPHL .	AOFUE		IVIAX	7.2
tPLH	CLR	ERR	MAX	5.7
tPZH	OE OE	A or B	MAX	5.6
tpzl	UE	AUID	WAX	6
tPHZ	ŌĒ	A or B	MAX	5.4
tPLZ	7 05			4.3
tpzh	ŌĒ	PARITY	MAX	5.7
tPZL	J 0E	PARITY	WAA	6.5
tPHZ	ŌĒ	DADITY	MAX	4.7
tPLZ	UE	PARITY	IVIAA	4.1
tPLH	LE	ERR	MAX	4.8
tPHL .	LE		MAX	4.9
tPLH	A. B or PARITY	ERR	MAX	7.2
tPHL .	A, D UI PARIIT	ENN	WAX	7.4



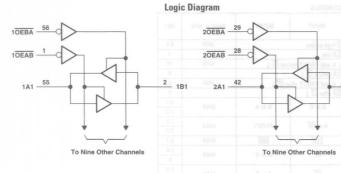
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# FUNCTION TABLE

### AND DESCRIPTION OF THE PARTY OF

### SOUTHWISE SERVICE SERVICES

# 16861



15

# FUNCTION TABLE (each 10-bit section)

OEAB	OEBA	OPERATION
L. L		Latch A and B (A = B)
L	H L	A to B B to A
H	H	Isolation

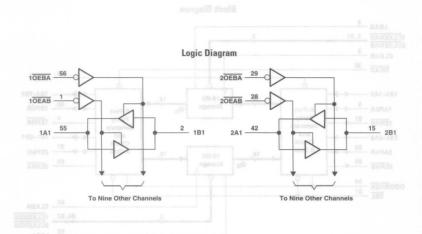
### RECOMMENDED OPERATING CONDITIONS

TIEGOTHITIETOED OF	LIBATING GONDIN	1	_
PARAMETER	MAX or MIN	ACT	UNIT
Icc	MAX	0.08	mA
Іон	MAX	-24	mA
lo <sub>L</sub>	MAX	24	mA

### SWITCHING CHARACTERISTICS

SWITCHING CHAR	ACTERISTICS			_
PARAMETER	INPUT	OUTPUT	MAX or MIN	ACT
tPLH .	A or B			10.4
tphl.	AOFB	B or A	MAX	11.1
tPZH	OEBA or OEAB		1449	10
tPZL	UEBA OF UEAB	A or B	MAX	12.7
tphz	OEBA or OEAB	A or B	MAX	10.7
tPLZ	UEDA OF UEAD	AOFB	IVIAA	10

# 18-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS / REVIEW AND LARGE VIEW TIGHT



### FUNCTION TABLE (each 9-bit section)

	langua			
INP	UTS	Ci Santa and James de North		
OEAB	OEBA			
Н	L	B data to A bus		
L	H	A data to B bus		
H	H	Isolation		
		A or state a		

## STREET MOLLONG

### RECOMMENDED OPERATING CONDITIONS

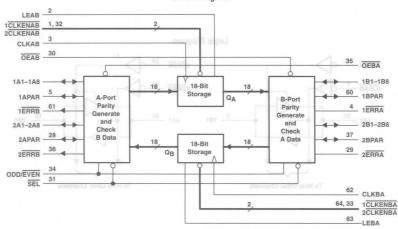
PARAMETER	MAX or MIN	ABT	ACT	ALVCH 3V	UNIT
Icc	MAX	32	0.08	0.04	mA
Іон	MAX	-32	-24	-24	mA
lou	MAX	64	24	24	mA

### SWITCHING CHARACTERISTICS

SVVII CHING CHAN	ACTEMISTICS			4.034		
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT	ALVCH 3V
tPLH .	A D	D as A	MAN	3.5	11.1	3.4
tPHL .	A or B	B or A	MAX	3.9	11.8	3.4
tPZH	OEBA or OEAB	H AW	H	5.4	10.6	4.7
tPZL	UEBA OF UEAB	A or B	MAX	4.8	13.6	4.7
tPHZ	OEBA or OEAB	4 0	MAX	. 6	11.6	4.2
tPLZ	UEBA OF UEAB	A or B	MAX	5	11	4.2

# 18-BIT UNIVERSAL BUS TRANSCEIVER WITH PARITY GENERATORS/CHECKERS AT 2018 TIR-BIT

# **Block Diagram**



**FUNCTION TABLE** 

	OUTPUT				
CLKENAB	OEAB LEAB		CLKAB	Α	В
X	Н	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	Bo‡
L	L	L	1	L	L
L	L	L	1	H	H
L	L	L	L	X	Bo‡
L	L	L	H	X	B <sub>0</sub> §

## PARITY-ENABLE FUNCTION TABLE

INPUTS		3	OPERATION	OR FUNCTION
SEL	OEBA	OEAB	OFERATION	ON PONCTION
L	Н	L	Parity is checked on port A a	and is generated on port B.
L	L	H	Parity is checked on port B a	and is generated on port A.
L	H	H	Parity is checked on port B a	and port A. A of all a
L	L	L	Parity is generated on port A	and B if device is in FF mode.
Н	L	L	Parity funcions are	QA data to B, QB data to A
H	L	H	disabled; device acts as a	Q <sub>B</sub> data to A
H	H	L	standard 18-bit registered	Q <sub>A</sub> data to B
Н	H	H	transceiver.	Isolation

PARITY FUNCTION TABLE

1888	PUTS	OUT	100	1100			INPUTS				
ERRB	BPAR	ERRA	APAR	BPAR	APAR	Σ OF INPUTS B1-B8 = H	Σ OF INPUTS A1-A8 = H	ODD/EVEN	OEAB	OEBA	SEL
Z	L	H	N/A	N/A	L	N/A	0, 2, 4, 6, 8	L	L	H	L
	H	L	N/A	N/A	L	N/A	1, 3, 5, 7	L	L	H	L
Z	L	S L	N/A	N/A	H	N/A	0, 2, 4, 6, 8	L	L	H	L
Z	H	Н	N/A	N/A	H	N/A	1, 3, 5, 7	L	L	H	L
Н	N/A	Z	L	L	N/A	0, 2, 4, 6, 8	N/A	L	Н	L	L
L	N/A	Z	H	L	N/A	1, 3, 5, 7	N/A	L	H	L	L
L	N/A	Z	L	Н	N/A	0, 2, 4, 6, 8	N/A	L	H	L	L
H	N/A	Z	H	H	N/A	1, 3, 5, 7	N/A	L	H	L	L
Z	Н	L	N/A	N/A	L	N/A	0, 2, 4, 6, 8	H	L	H	L
Z	LIST	H	N/A	N/A	BAL	N/A	1, 3, 5, 7	H	L	H	L
Z	H	H	N/A	N/A	H	N/A	0, 2, 4, 6, 8	H	L	H	L
Z	L	L	N/A	N/A	H	N/A	1, 3, 5, 7	H	L	H	L
8 L	N/A	Z	H	L 100	N/A	0, 2, 4, 6, 8	N/A	Н	Н	L	L
Н	N/A	Z	L	L	N/A	1, 3, 5, 7	N/A	H	H	L	L
H	N/A	Z	Н	Н	N/A		N/A	H	H	L	L
AL	N/A	Z	W. L.	H X	N/A	1, 3, 5, 7	N/A	H	H	L	L
Н	Z	Н	Z	L	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	L	Н	Н	L
L	Z	L	Z	L	a L	1, 3, 5, 7		L	H	H	L
AL	Z	L		HX	H		0, 2, 4, 6, 8	L	H	H	L
H	Z	Н	Z	H	H	1, 3, 5, 7	1, 3, 5, 7	L	H	H	L
L	Z	L	Z	L	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	Н	Н	Н	L
H	Z Z	H	Z	L	L	1, 3, 5, 7	1, 3, 5, 7	H	H	H	L
H	Z	Н	Z	H	H	0, 2, 4, 6, 8	0, 2, 4, 6, 8	H	H	H	L
L	Z	L	Z	H	H	1, 3, 5, 7	1, 3, 5, 7	H	Н	Н	L
Z	PE†	Z	PE†	N/A	N/A	N/A	N/A	L	L	L	L
z	POİ	Z	PO±	N/A	N/A	N/A	N/A	H	L	L	L

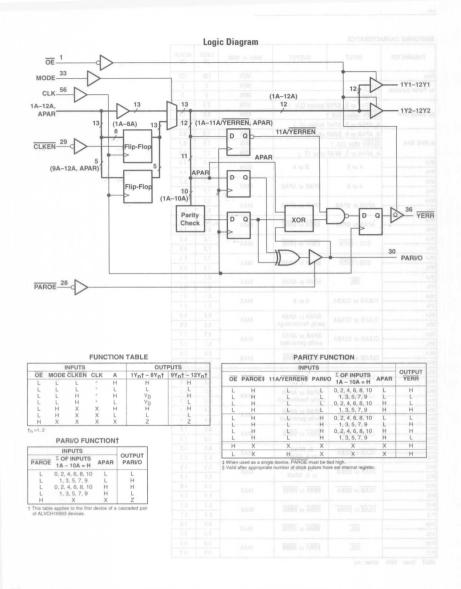
<sup>†</sup> Parity output is set to the level so that the specific bus side is set to even parity ‡ Parity output is set to the level so that the specific bus side is set to odd parity.

<sup>‡</sup> Output level before the indicated steady-state input conditions were established
§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

PARAMETER	MAX or MIN	LVCH 3V	ALVCH 3V	UNIT
Icc	MAX	0.02	0.04	mA
Іон	MAX	-24	-24	mA
lou	MAX	24	24	mA

### SWITCHING CHARACTERISTICS

SWITCHING CHAR	ACTERISTICS		communit :	looir.		
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVCH 3V	ALVCH 3V	
fmax			MIN	125	125	
rygr-ryr	CLK †		MIN	3	3	
tw Pulse duration	LE high	180161	MIN	3	3	
	A, APAR or B, BPAR	R hefore CLK ↑	MIN	2.5	1.7	
tsu Setup time	CLKEN before CLK		MIN	2.5	1.7	
	A, APAR or B, BPAR		MIN	2	1.2	
	A, APAR or B, BPAR		MIN	1.3	0.5	
th Hold time	CLKEN after CLK ↑	Tuttor out	MIN	1.5	0.7	
	A, APAR or B, BPAR	Rafter LE J	MIN	1.7	0.9	
tPLH .				5.4	4.4	
tphl.	A or B	B or A	MAX	5.4	4.4	
tPLH				7.7	6.7	
tPHL	A or B	BPAR or APAR	MAX	7.7	6.7	
tPLH .	-			5.7		
tPHL	APAR or BPAR	BPAR or APAR	MAX	5.7	4.7	
tPLH .	9 9 0	may I	0.0	8.5	7.5	
TPHL	APAR or BPAR	ERRA or ERRB	MAX	8.5	7.5	
TPLH TPLH			4 4	7.8	6.8	
270200	ODD / EVEN	ERRA or ERRB	MAX	7.8	6.8	
tPHL OR		4		7.5	6.5	
tPLH DAIRAG	ODD / EVEN	BPAR or APAR	MAX	7.5	6.5	
tPHL				6.1	5.1	
tPLH	SEL	BPAR or APAR	MAX	6.1	5.1	
tPHL				6.1	5.1	
tPLH .	CLKAB or CLKBA	A or B	MAX	6.1	5.1	
tPHL .					5.6	
tPLH	CLKAB or CLKBA	BPAR or APAR parity feedthrough	MAX	6.6	_	
tPHL .				6.6 8.7	7.7	
tPLH	CLKAB or CLKBA	BPAR or APAR parity generated	MAX		7.7	
tPHL .		parity generated		8.7	7.9	
tPLH	CLKAB or CLKBA	ERRA or ERRB	MAX	8.9	7.9	
tPHL .		chine		2.0	4.8	
tPLH	LEAB or LEBA	A or B	MAX	5.8	1000	
tpht.	H = A01 - A1			5.8	5.3	
tPLH .	LEAB or LEBA	BPAR or APAR	MAX	6.3	1,500.00	
tPHL .	H 1 01 B B A 3 D	parity feedthrough	18 4	6.3	5.3	
tplH H	LEAB or LEBA	BPAR or APAR	MAX	8.4	7.4	
tPHL .	VI. (1) (1) (1)	parity generated		8.4	7.4	
tPLH	LEAB or LEBA	ERRA or ERRB	MAX	8.5	7.5	
tPHL .	833523		7 1	8.5 6.3	7.5	
tPZH	OEAB or OEBA	B, BPAR or A, APAR	MAX		2.2	
tPZL		-		6.3	5.3	
tPHZ	OEAB or OEBA	B, BPAR	MAX	5.9		
tPLZ		or A, APAR		5.9	4.9	
tРZH	OEAB or OEBA	ERRA or ERRB	MAX	5.9	4.9	
tPZL	100000000000000000000000000000000000000			5.9	4.9	
tPHZ	OEAB or OEBA	ERRA or ERRB	MAX	6.7	5.7	
tPLZ				6.7	5.7	
tрzн	SEL	ERRA or ERRB	MAX	6.5	5.5	
tPZL		100000000000000000000000000000000000000	0.000.0000	6.5	5.5	
tPHZ	SEL	ERRA or ERRB	MAX	5.9	4.9	
tPLZ				5.9	4.9	



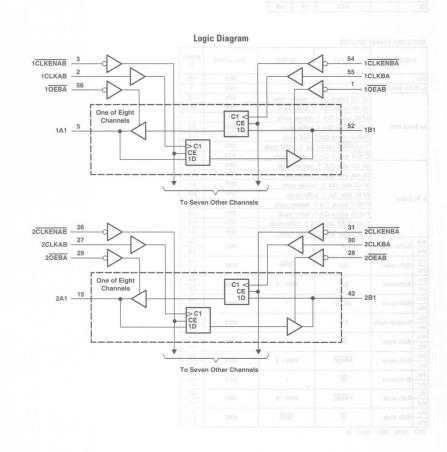
### SWITCHING CHARACTERISTICS

SWII	CHING CHARA	CTERISTICS			1
Р	ARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
fmax	ABAJ	J1 - 10		MIN	125
tw Pt	Pulse duration  CLK ↑  1A-12A before CLK ↑, resist  1A-10A before CLK ↑, suffer  APAR before CLK ↑, buffer  APAR before CLK ↑, buffer  PARI/O before CLK ↑, buffer  11A/YERREN before CLK ↑, resiste  1A-12A after CLK ↑, resiste  1A-12A after CLK ↑, resiste  1A-10A after CLK ↑, resiste  APAR after CLK ↑, buffer  APAR after CLK ↑, buffer  APAR after CLK ↑, buffer  APAR after CLK ↑, buffer  APAR after CLK ↑, buffer  APAR after CLK ↑, buffer  APAR after CLK ↑, buffer  APAR after CLK ↑, buffer  CLKEN after CLK ↑, vesister  Buffer mode  A  Buffer mode  CLK  Buffer mode  CLK  Buffer mode  CLK  Buffer mode  CLK  FELH  Both mode  CLK  FELH  Both mode  CLK  FELH  Both mode  CLK  FELH  Both mode  CLK  FELH  Both mode  CLK  FELH  Both mode  CLK  FELH  Both mode  CLK  FELH  Both mode  CLK  FELH  Both mode  CLK  FELH  Both mode  CLK  FELH  Both mode  CLK  FELH  Both mode  CLK  FELH  Both mode  CLK  FELH  Both mode  CLK  FELH  Both mode  CLK  FELH  Both mode		>	MIN	3
		1A-12A before CLK ↑	, resister mode	MIN	1.45
				MIN	4.4
		APAR before CLK 1,	resister mode	MIN	1.3
tsu Se	etup time	APAR before CLK 1,	buffer mode	MIN -	3.1
				MIN	1.7
		The second secon		MIN	1.6
		CLKEN before CLK ↑	, resister mode	MIN	2.2
				MIN	0.55
				MIN	0.25
				MIN	0.7
				MIN	0.25
th Ho	ld time		MIN	0.4	
				MIN	0.5
			MIN	0.4	
				MIN	0.4
tPLH	n // 2521	_ 08 P			3.8
tPHL.	Buffer mode	A A	Υ	MAX	3.8
tPLH	ERE	200	VEDD		4.4
tPHL.	Both mode	CLK	YERR	MAX	4.4
tPLH		214	212110	****	6.6
tPHL	Both mode	CLK	PARI / 0	MAX	6.6
tPLH	2 11 1	MODE	v	- OF	4.9
tPHL	Both mode	MODE	Y	MAX	4.9
tPLH		011/	Y	AAAV	4.8
<b>TPHL</b>	Resister mode	CLK	The state of the s	MAX	4.6
tPZH	B	ŌĒ.	V	MAX	5.4
tPZL	Both mode	UE	Υ	MAX	5.4
tPZH	D 41 1	PAROE	DARLLO	MAX	4.8
tPZL	Both mode	PARUE	PARI / 0	IVIAX	4.8
tPHZ	Both mode	ŌE	Y	MAX	5
tPLZ	Both mode	UE	, r	WAX	5
tPHZ	Dath made	PAROE	DADL / O	MAX	3.8
tPLZ	Both mode	PARUE	PARI / 0	IVIAA	3.8
tPLH	Both mode	ŌE	YERR	MAX	4
<b>TPHL</b>	Tour mode	UE	IENN	IVIAA	4.2

UNIT fmax: MHz other: ns



# 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS



### FUNCTION TABLE

	OUTPUT			
CLKENAB	CLKAB	OEAB		
Н	X	L	X	Bo‡
×	L	L	X	B <sub>0</sub> ‡
L	1	L	L	L
L	TYR -	L	H	Н
Н	X	Н	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses CEKENBA, CLKBA, and OEBA.

‡ Level of B before the indicated steady-state input conditions were established.

# S-Ω OCTAL BUS BUFFERS/DRIVERS

High Output Drive Correct

Distributed V<sub>CC</sub> and GND Pins Minimize Noise

1A3 20

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	AC	LVTH 3V	LVCH 3V	ALVCH 3V	UNIT
Icc	MAX	35	0.08	5	0.02	0.04	mA
Іон	MAX	-32	-24	-32	-24	-24	mA
lou	MAX	64	24	64	24	24	mA

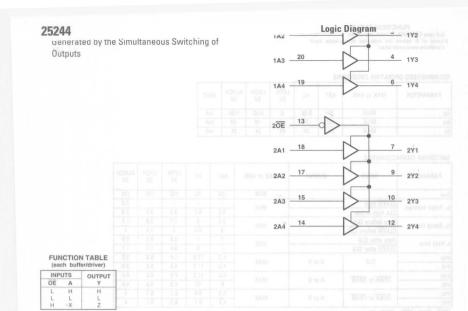
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	AC	LVTH 3V	LVCH 3V	ALVCH 3V
fmax	ne II	- 87	MIN	150	75	150	150	150
tw Pulse duration	CLKEN high		MIN	-	-	-	-	3.3
tw ruise duration	CLK high or low	IVIIN	3.3	6.7	3.3	3.3	3.3	
tsu Setup time	Data before CLK  CLKEN before CLK		MIN	3.5	5	1.7	2.8	1.5
			MIN .	3	6.5	2	1.4	1
	Data after CLK  CLKEN after CLK		MIN	1	1	0.8	0.5	0.8
th Hold time			IVIIIN	1	0	0.4	1.9	1.1
tPLH	CLK	A B	AAAW	4.3	11.8	4.4	6.6	3.9
tPHL .	CLK	A or B	MAX	4.5	11.7	4.4	6.6	3.9
tPZH	OEBA or OEAB	4 D	MAN	4.6	11.2	4.9	6.6	4.4
tPZL	OEBA or OEAB A or B		MAX	6	13	4.9	6.6	4.4
tPHZ	OEBA or OEAB A or B		MANY	5.5	9.4	6.2	6.7	4
tPLZ			MAX	4.2	8.7	5.3	6.7	4

UNIT fmax: MHz other:ns

DAMENDED OPERATING CONDITIONS

PAYTRICETA CO AND DISCOTTO



RECOMMENDED OF	PERATING CONDIT	IONS		
PARAMETER	MAX or MIN	SN74 BCT	SN64 BCT	UNIT
Icc	MAX	119	119	mA
Тон	MAX	-80	-80	mA
lou	MAX	188	188	mA

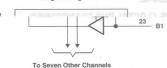
## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT	SN64 BCT
tPLH				5.5	5.5
tphL .	A	, ,	MAX	6	6.3
tpzH	ŌĒ	V	MAN	9.3	9.7
tPZL.	UE	1	MAX	10.2	10.4
tPHZ	ŌE	v	MAX	6.3	6.5
tPLZ	UE	Y	WAX	8.4	9.5





# **Logic Diagram**



FUNCTION TABLE

			INPUTS		
HON	KAI	OPER		DIR	OE
A bus	to	data	В	L	L
B bus	to	data	A	H	L
on	Isolation				H

### FUNCTION TABLE

### RECOMMENDED OPERATING CONDITIONS

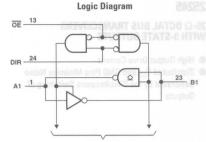
PARAMETER	MAX or MIN	SN74 BCT	АВТН	UNIT
Icc	MAX	125	20	mA
loн (A port)	MAX	-80	-80	mA
loн (B port)	MAX	-3	-32	mA
lot (A port)	MAX	188	188	mA
lot (B port)	MAX	24	64	mA

### COMMENDED OPERATING CONDITIONS

## SWITCHING CHARACTERISTICS

SWITCHING CHARAC	CIENISTICS					1		
PARAMETER	INPUT	ОИТРИТ	MAX or MIN	SN74 BCT	ABTH	מעדרט		
tPLH	A	В	MAX 5.7 3.9 7.2 4.3	5.7 3.9	5.7 3.9	3.9	5.7 3.9	
tPHL .	А	В		7.2	4.3	8.		
tPLH .	В		MAX	5.5	3.9	A		
TPHL	В	A	IVIAX	6.2	4.3	- 2.		
tPZH	ŌE	A	MAX	9.6	6.5	A		
tPZL	UE	_ ^	A THINA	10.3	6.8	^		
tPHZ	ŌE	A	MAX	6.2	7.2	8		
tPLZ	OE.	A	8 IVIAA	8.3	6.4	- 0		
tРZH	OE B	MAX	8.9	6.5	0			
tPZL	UL.	Б	OL SINAX 9.	9.7	6.8			
tPHZ	ŌE	В	MAX	6.9	7.2			
tPLZ	UE	UE B WI	WAA	7.5	6.4			

- High Output Drive Current
- Distributed V<sub>CC</sub> and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs



To Seven Other Channels

# **FUNCTION TABLE**

INPUTS		0050171011
ŌĒ	DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	UNIT
Icc	MAX	125	mA
loн (B port)	MAX	-3	mA
lot (A port)	MAX	188	mA
lot (B port)	MAX	24	mA
Von (A port)	MAX	5.5	V

SWITCHING CHARAC	CTERISTICS					
PARAMETER	INPUT	OUTPUT HEE	MAX or MIN	SN74 BCT		
tPLH	A	В	MAX	6.2		
tPHL .	A	D 8.4	IVIAA	4		
tPLH .	В	A	MAX	6.3		
tPHL	D	A 8.3	IVIAX	5.9		
tPLH	ŌĒ	A	MAX	11.6		
tPHL .	UE	A 9.8	IVIAX	11.3		
tPZH	ŌĒ	В 5.0	MAX	9.1		
tPZL	UE	D 9.3	IVIAA	9.8		
tPHZ	ŌĒ	В	MAX	7.3		
tPLZ	UE	B	WAX	7.3		
UNIT: ns		1.5	6.8	KAM		

# 29821 **Logic Diagram** 10-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS 3-State Outputs > C1 Data Flow-Through Pinout 1D 1D -To Nine Other Channels FUNCTION TABLE (each filp-flop) INPUTS OUTPUT CLK D Q HorL 00

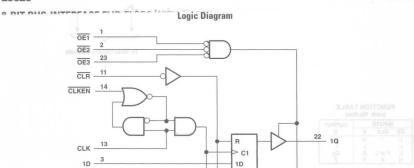
### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 BCT	UNIT
Icc	MAX	115	35	mA
Іон	MAX	-24	-24	mA
lor	MAX	48	48	mA

### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 BCT
fmax		- 2	CHAIRCTCAILST	RO AWA	125
tw Pulse duration	CLK high or low		MIN	7	7
tsu Setup time	Data before CLK ↑	UO FO	MIN	4	7
th Hold time	Data after CLK ↑		MIN	2	1
tPLH .	CIV	0	MAY	10	12
tPHL .	CLK	а	MAX	10	10
tpzh	ŌĒ			14	12
tPZL	UE UE	ngmansb 1-2	MAX	14	13
tPHZ	0.5	VIOLETTIA T. 7	MAN	14	8
tPLZ	- OE	Q.	MAX	12	8

UNIT fmax : MHz other : ns



To Seven Other Channels

**FUNCTION TABLE** 

		INPUTS			OUTPUT
OE†	CLR	CLKEN	CLK	D	Q
L	L	X	X	X	L
L	H	L	1	H	H
L	H	L		L	L
L	H	H	HorL	X	Qn
H	X	X	X	X	Z

 $\uparrow \overline{OE} = H$  if any of the output-enable inputs is high.  $\overline{OE} = L$  if all of the output-enable inputs are low.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	UNIT
Icc	MAX	40	mA
Іон	MAX	-24	mA
lou	MAX	48	mA

PARAMETER	INPUT		MAX or MIN	SN74 BCT
fmax		1.303.4	MIN	125
7.0	CLK low	2. 7.	MIN	4
tw Pulse duration	CLK high or low		MIN	4
- XI	Before CLK ↑, data	high	MIN	6
	Before CLK †, data	MIN	3.5	
tsu Setup time	CLR	MIN	1.	
	CLKEN before CLK	MIN	8	
	After CLK ↑, data h	MIN	1.5	
th Hold time	After CLK ↑, data lo	MIN	0	
	CLKEN after CLK ↑	MIN	0.5	
tPLH	0111			9
tphL .	CLK	Q.	MAX	8.4
tphl.	CLR	Q	MAX	9.5
tрzн	- OE			10.3
tPZL	UE	Q	MAX	10.2
tрнZ	- OE	0	MAX	9
tPLZ	1 UE	u u	WAX	8.2

UNIT fmax: MHz other:ns

2093 Tate Outputs

Data Flow-Through Pinout



To Nine Other Channels

**FUNCTION TABLE** 

	INPUT		OUTPUT
OE1	OE2	Α	Y
L	L	L	L
L	L	H	H
L	X	X	Z
H	H	X	2

†n = 1,2

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 BCT	UNIT
lcc	MAX	40	40	mA
Іон	MAX	-24	-24	mA
lou	MAX	48	48	mA

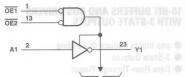
						1	
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 BCT	BUTFUS	
tPLH .		7 5.5					
tPHL .	_ A	,	MAX	7.5	7.5	Y	
tPZH	ŌE	V MAY 15 9.	9.1				
tPZL	- UE	1	MAX	15	12.8	1 7	
tрнz	ŌE	- <del> </del>	8.8				
tPLZ -	] UE	7	MAX	12	8.4	7	
UNIT: ns							

# 29828

# **10-BIT BUFFERS AND BUS DRIVERS** WITH 3-STATE OUTPUTS

- pnp Inputs Reduce dc Loading
- 3-State Outputs
- Data Flow-Through Pinout





To Nine Other Channels

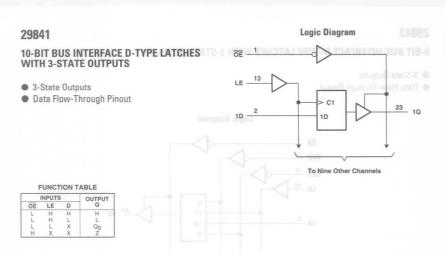
RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	UNIT
Icc	MAX	40	mA
Гон	MAX	-24	mA
lou	MAX	48	mA

SWITCHING CHARAC	CTERISTICS								
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS					
tPLH .		V I	MAX	7					
tPHL .	A	Yaz	MAX	7.5					
tPZH	ŌĒ	v		15					
tPZL	UE	Y 8.5	MAX	15					
tPHZ	ŌĒ	8.8	8.8	17					
tPLZ	UE	Ψ 0,1	WAX	MAX 12		12			

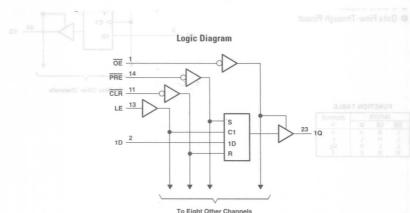
UNIT: ns

**NOTICE: ALS IS NOT RECOMMENDED FOR NEW DESIGNS** 



PARAMETER	MAX or MIN	ALS	SN74 BCT	UNIT
lcc	MAX	85	35	mA
Іон	MAX	-24	-24	mA
lou	MAX	48	48	mA

SWITCHING CHAP	ACTERISTICS				
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 BCT
tw Pulse duration	LE high or low		MIN	6	4
tsu Setup time	Data beforeLE ↓		MIN	2.5	2
th Hold time	Data after LE 1, hig	h	MIN	4.5	1.5
	Data after LE 1, lov	V	MIN	4.5	3.5
tplh	D	Q	MAX	9.5	7.5
tphl .		u u	IVIAA	9.5	8.6
tplH	LE	Q	MAX	12	8.6
tPHL	_ LE	u u	IVIAA	12	8.1
tPZH	ŌE	0	MAX	14	9.2
tPZL	UE	u	MAX	14	12.8
tPHZ	ŌĒ	0	MAX	15	6.9
tPLZ	7 06	l u	IVIAX	12	6.9



To Eight Other Channels

## **FUNCTION TABLE**

		INPUTS		OUTPUT	
PRE	CLR	ŌĒ	E LE		Q
L	X	L	X	X	Н
H	L	L	X	×	L
H	H	L	H	L	L
H	H	L	Н	H	Н
Н	H	L	L	X	Qn
X	X	H	X	X	Z

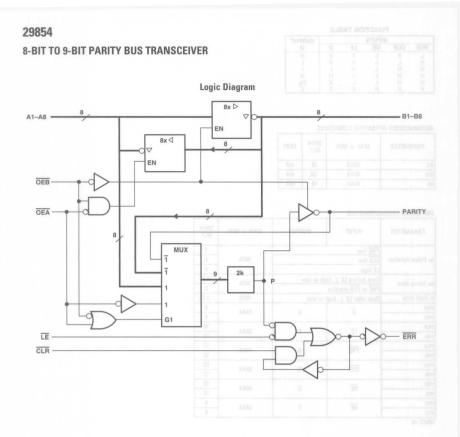
## BIT TO 9-BIT PARITY BUS TRANSCRIVER

Logic Diagram

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	UNIT
Icc	MAX	35	mA
Іон	MAX	-24	mA
lor .	MAX	48	mA

OTTITUDE OFFICE	0.1012111011100			
PARAMETER	INPUT	ООТРОТ	MAX or MIN	SN74 BCT
	PRE low			7
tw Pulse duration	CLR low		MIN	5
	LE high		Je	4
4 C-4 1	PRE low CLR low LE high Data before LE ↓, h PRE or CLR inactive Data after LE ↓, high	high or low	MIN	1.5
tsu Setup time			IVIIIV	2
th Hold time	Data after LE 1, his	gh or low	MIN	3.5
tPLH		Δ.	MAX	8
tPHL	D	u u	IVIAX	9
<b>TPLH</b>	Si se	- 0	MAX	10
tPHL .	C b L	u	IVIAX	10
tplh	DDE	0	MAX	12
tphL .	PRE	۵	MAX	12
tplH .	010	0	MAX	12
tphL .	CLR	u	MAX	12
tpzh	<u> </u>	0	MAX	15
tPZL	UE	u	IVIAX	15
tPHZ	05	Q.	MANY	8
tou a	- UE	1 4	MAX	0



### FUNCTION TABLE

	0	T AND I/	UTPU	0			UTS	INP		
OPERATION	TA SA	PARITY	В	A	Bi† Σ of Ls	Ai Σ of Hs	LE	CLR	OEA	OEB
A data to B bus and generate parity	NA	H	Ā	NA	NA	Odd Even	X	X	Н	L
B data to A bus and check parity	H	NA	NA	B	Odd Even	NA	L	Χ	L	Н
Store error flag	N-1	NA	NA	X	X	NA	Н	Н	L	Н
Clear error-flag register	Н	NA	NA	X	X	X	H	L	Х	X
Isolation§	NC H L H	Z	z	Z	х	X X L Odd H Even	HHLL	H L X	Н	Н
Ā data to B bus and generate inverted parity	NA	L H	Ā	NA	NA	Odd Even	X	X	L	L

NA = not applicable, NC = no change, X = don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
† Output states Shown assume ERR was previously high.
§ in this mode, ERR, when enabled, shows inverted parity of the A bus.

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 BCT	UNIT
Icc	MAX	100	80	mA
Іон	MAX	-24	-24	mA
lou	MAX	48	48	mA

### WITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 BCT	08
	LE high		MIN	10		
tw Pulse duration	LE low		MIN	10	10	
	CLR low		MIN	10	10	
	Before LE 1, Bi and	PARITY	MIN	10	18	1
tsu Setup time	Before LE ↓, CLR his	gh	MIN	15	-	1
th Hold time	Bi and PARITY after	LE ↓	MIN	3	8	
tplh	A or B	B or A	MANY	8	8	
tphL .	A OF B B OF A		MAX	8	8	שהייטו
tplh	A	DARITY	MANY	15	15	1
tphL.	A	PARITY	MAX	18	15	A so 8
tpzh	OEA or OEB	A D	MAX	17	17	]
tPZL	UEA OF UEB	A or B	MAX	17	19	8 10 /
tPHZ	OEA or OEB			15	15	
tPLZ	UEA OF UEB	A or B	MAX	8	17	B to A
tPHL .	LE	ERR	MAX	12	9	
tplh	CLR	ERR	MAX	12	15	1
tplh	OEA	DADITY	MAN	17	15	
tphl.	UEA	PARITY	MAX	19	16	1
tplH	D: / DADITY	Bi / PARITY ERR			20	1
tPHL .	Bi / PARITY	ERR	MAX	20	15	1

# 29863

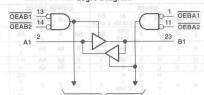
# 9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

True Outputs

### **FUNCTION TABLE**

	INP	- Janeary		
OEAB1	OEAB2	OEBA1	OEBA2	OPERATION
L	L	L	L	Latch A and B
L	L	H	X	A to B
L	L	X	Н	AIOB
H	X	L	L	B to A
X	Н	L	L	DIOA
Н	X	Н	X	
H	X	X	H	Installed
X	H	X	H	Isolation
X	H	H	X	

# Logic Diagram



To Eight Other Channels

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 BCT	UNIT
lcc	MAX	65	45	mA
Іон	MAX	-24	-24	mA
lou	MAX	48	48	mA

### SWITCHING CHARACTERISTICS

SWITCHING CHAIL	ACTEMISTICS			MIN		
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 BCT	Ang 8
tPLH	A D	2 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4		8	5	PARITY
tPHL .	A or B	B or A	MAX	8	7.5	
tPZH	054D 05D4	A D	MANY	15	8.4	8 to A
tpzi	OEAB or OEBA	A or B	MAX	15	12.6	1
tPHZ	OF A D OF D A		1447	17	8.8	8 an A
tPL7	OEAB or OEBA	A or B	MAX	12	8.1	-

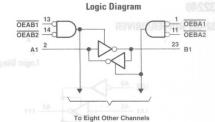
1	. 0	CI.	12	8.1	

# 9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

Inverted Outputs



	INPUTS				
OPERATION	OEBA2	OEBA1	OEAB2	OEAB1	
Latch A and B	L	L	L	E	
Ā to B	X	H	L	L	
AIOO	Н	X	L	L	
B to A	L	L	X	Н	
DIOA	LIST	L	Н	X	
	X	H	X	Н	
Do Catalon	H	X	X	H	
Isolation	H	X	H	X	
	X	H	H	X	



179 SO 80 1

RECOMMENDED OPERATING CONDITIONS

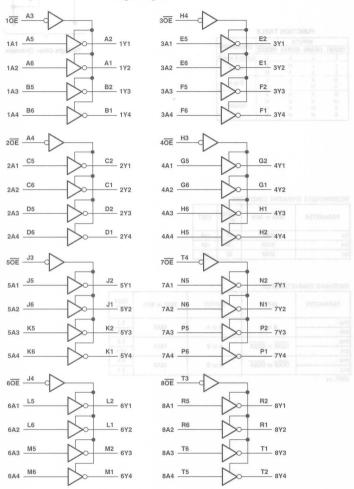
PARAMETER	MAX or MIN	SN74 BCT	UNIT
lcc	MAX	45	mA
Іон	MAX	-24	mA
lou	MAX	48	mA

SWITCHING CHAIL	ACTEMOTIO			
PARAMETER	INPUT	ОИТРИТ	MAX or MIN	SN74 BCT
tPLH -	A or B	D A	MAX	6.1
tPHL .	AOLD	B or A	IVIAA	4.8
tpzH	OF A D OF D A		MANY	8.4
tpzl.	OEAB or OEBA	A or B	MAX	12.5
tphz	OFAD OFDA	A D	MAN	8.4
tPLZ	OEAB or OEBA	A or B	MAX	8.2



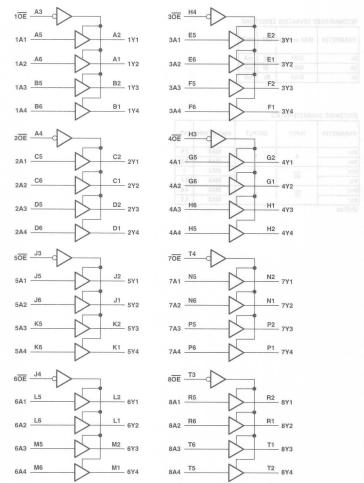
BIT BUS TRANSCEIVERS

Logic Diagram



INP	JTS	OUTPUT
ŌĒ	Α	Υ
L	Н	L
L	L	H
Н	×	Z

TEOO!	D OPERATING	COND	ITIONS				
PARAMETER	MAX or MIN	LVT	UNIT				
lcc	MAX	10	mA				
Іон	MAX	-32	mA				
lou	MAX	64	mA				
	378	201	$\vdash$				
SWITCHING C	HARACTERISTI	CS	_<	1	NAE NAE		
PARAMETER	INPUT	00	TPUT	MAX or MIN	LVT		
tPLH			V	MAX	3.5	7	
tphl .	A sya -	(SE)	Y	MAX	3.5		
tpzh	- OE		Υ	MAX	4		
tPZL		10		MAX	4.4		
tPHZ	OE OE		Y	MAX	4.5		
tPLZ UNIT:ns	£Y8 -			MAX	4.2		

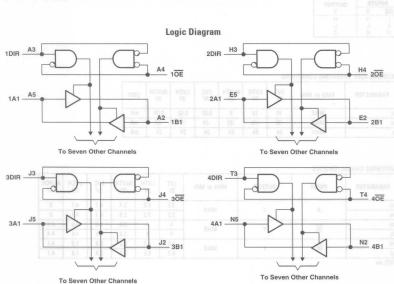


PARAMETER	MAX or MIN	LVT 3V	LVTH 3V	ALVTH 3V	LVC	LVCH 3V	ALVCH 3V	UNIT
lcc	MAX	10	10	5	0.02	0.02	0.04	mA
но!	MAX	-32	-32	-32	-24	-24	-24	mA
lor	MAX	64	64	64	24	24	24	mA

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVT 3V	LVTH 3V	ALVTH 3V	3V LVC	LVCH 3V	ALVCH 3V
PLH	A	v	MAX	3.2	3.2	2.4	4.1	4.1	3
tPHL .		1		3.2	3.2	2.5	4.1	4.1	3
PZH	<u> </u>	Y	MAX	4	4	3.8	4.6	4.6	4.4
tPZL	OE			4	4	2.9	4.6	4.6	4.4
tPHZ	or.	V	MAY	4.5	4.5	4.2	5.8	5.8	4.1
PLZ	0E	Y	MAX	4.2	4.2	3.6	5.8	5.8	4.1

## 32245

# 36-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

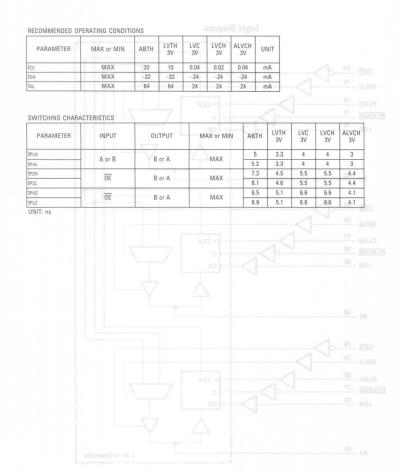


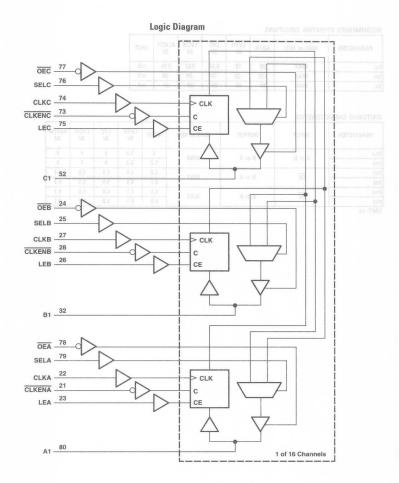
FUNCTION TABLE (each 9-bit section)

AFFCE

## 6-BIT TRI-PORT UNIVERSAL BUS EXCHANGERS

	OPERATION		INPUTS		
TION			DIR	OE	
A bus	to /	data	В	L	L
B bus	to I	data	A	H	L
on	latio	Iso		×	Н





# FUNCTION TABLE STORAGE†

	INPU	TS		
CLKENA	CLKA	LEA	Α	OUTPUT
Н	X	L	X	Qn‡
L	1	L	L	L
L		L	H	H
X	H	L	X	Qn‡
X	L	L	X	Qn‡
X	X	H	L	L
×	X	H	H	H

† A-port register shown, B and C ports are similar but use CIKENB, CIKENC, CIKB, CIKC, LEB, and LEC † Output level before the indicated steady-state input conditions were established.

A-PORT OUTPUT					
INP	UTS	OUTDUT A			
OEA	SELA	OUTPUT A			
Н	X	Z			
L	H	Output of C register			
L	L	Output of B register			

#### B-PORT OUTPUT

INPUTS		CHEMIN D	
OEB	SELB	OUTPUT B	
Н	X	Z	
L	H	Output of A register	
L	L	Output of C register	

#### C-PORT OUTPUT

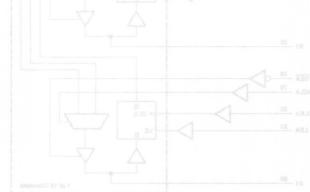
INP	UTS	оитрит с			
OEC	SELC				
H >	X	H X	X Z	Z	
L	H	Output of B register			
L	L	Output of A register			

## RECOMMENDED OPERATING CONDITIONS

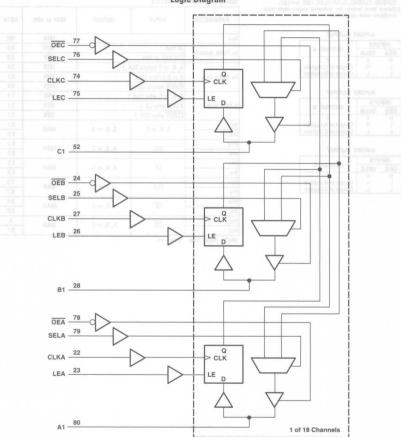
PARAMETER	MAX or MIN	ABTH	UNIT
Icc	MAX	40	mA
Іон	MAX	-32	mA
lou	MAX	64	mA

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH
fmax		1	MIN	150
. Dulas duradas	LE high		MIN	3.3
tw Pulse duration	CLK high or low	-	MIN	3.3
	A, B, or C before CL	K ↑	MIN	2.4
tsu Setup time	A or B before LE ↓		MIN	2.1
	CLKEN before CLK		MIN	3.2
31	A, B, or C after CLK	Î	MIN	1.4
th Hold time	A or B after LE ↓		MIN	2.1
	CLKEN after CLK ↑		MIN	1.1
tPLH	A D C	C D A	MAX	6.1
tPHL	A, B, or C	C, B, or A	MAX	6.6
tPLH .	SEL	A D C	MAN	6.5
tPHL .	SEL	A, B, or C	MAX	6.5
tPLH	LE	A D C	MAX	7.5
tPHL	LE	A, B, or C	IVIAA	6.9
tPLH .	CLK	A P os C	MAX	7.5
tPHL	- CLK	A, B, or C	IVIAX	6.7
tPZH	ŌĒ	A B az C	MAX	6.4
tPZL	UE	A, B, or C	IVIAA	6.8
tPHZ	- OE	A, B, or C	MAX	6
tPLZ	J. J.	M, D, 01 C	IVIAA	6.1

UNIT fmax : MHz other : ns



Logic Diagram



#### FUNCTION TABLE STORAGET

	0.10.10.0001					
INPUTS						
CLKA	LEA	Α	OUTPUT			
1	L	L	L			
1	L	H	Н			
H	L	X	Qo‡			
L	L	X	Q <sub>0</sub> ‡			
X	H	L	L			

† A-port register shown, B and C ports are similar but use CLKB, CLKC, LEB, and LEC. ‡ Outpu level befor the indicated steady-state input conditions were established.

## A-PORT OUTPUT

INPUTS			
OEA	SELA	OUTPUT A	
Н	X	Z	
Low	H	Output of C register	
L	L	Output of B register	

## B-PORT OUTPUT

	INPUTS	
OUTPUT B	SELB	OEB
Z	X	Н
Output of A register	H	L
Output of C register	L	L

## C-PORT OUTPUT

INPUTS			
OEC	SELC	OUTPUT C	
H	X	Z	
L	H	Output of B register	
1.	1	Output of A register	

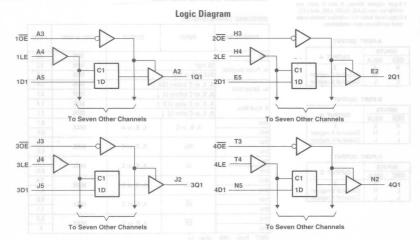
## RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABTH	UNIT
Icc	MAX	45	mA
Іон	MAX	-32	mA
IOL.	MAX	64	mA

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	АВТН
fmax			MIN	150
D. I I I	LE high		MIN	3.3
tw Pulse duration	CLK high or low		MIN	3.3
70	A, B, or C before CL	K ↑	MIN	2.4
tsu Setup time	A, B, or C before LE	MIN	2.1	
e Hald days	A, B, or C after CLK ↑		MIN	1.4
th Hold time	A, B, or C after LE ↓		MIN	2.1
tplh	A D C	C D A	MAY	6.1
tphl	A, B, or C	C, B, or A	MAX	6.6
tPLH	SEL	A, B, or C	MAX	6.5
tPHL	SEL	A, D, UI C	IVIAX	6.5
tPLH .	LE	A, B, or C	MAX	7.5
tphl .	LE	A, b, or c	IVIAX	6.9
tPLH	CLK	A D C	MAX	7.4
tPHL C	CLK	A, B, or C	IVIAX	6.7
tрzн	ŌĒ	A B as C	MAN	6.8
tPZL	1 06	A, B, or C	MAX	7.1
tphz	OF A B or C		MAN	6.2
tPLZ			MAX	6

UNIT fmax: MHz other: ns



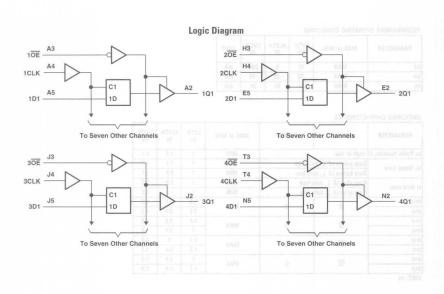
## **FUNCTION TABLE**

ľ		NPUTS		OUTPUT
	OE	LE	D	Q
	L	Н	H	Н
	L	H	L	L
	L	L	X	Qn
	L	V	Y	7

## BECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVTH 3V	ALVTH 3V	LVCH 3V	UNIT
Icc	MAX	10	5	0.02	mA
Юн	MAX	-32	-32	-24	mA
lou	MAX	64	64	24	mA

PARAMETER	alinput o ned	O m OUTPUT	MAX or MIN	LVTH 3V	ALVTH 3V	LVCH 3V
tw Pulse duration,	LE high or low	-8	MIN	3	1.5	3.3
tsu Setup time	Data before LE 1, da	ata high	MIN	1	1.4	1.7
tsu Setup time	Data before LE 1, data low  Data after LE 1, data high	MIN	1	0.9	1.7	
ts Uald time	high or low MIN Data before LE \( \), data high MIN Data before LE \( \), data low MIN Data after LE \( \), data high MIN	MIN	1	0.9	1.2	
is note time	Data after LE ↓, dat	a low	MIN	1	1.4	1.2
tPLH DI	S	0		3.8	3.1	4.2
tphl .		u	IVIAX	3.6	3.3	4.2
tplh	15	0	MAN	4.3	3.3	4.6
tphl.	LE	u	IVIAX	4	3.5	4.6
tРZH	OF HOLD	C commont	MAN	4.3	4	4.7
tPZL	- UE	ц	MAX	4.3	3.4	4.7
tPHZ	ŌĒ	0	LAXV.	5	4.9	5.9
tPLZ	OE OE	u u	MAX	4.7	4.5	5.9



#### FUNCTION TABLE (each flip-flop)

	INPUTS		OUTPUT
OE	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	HorL	X	Qn
H	X	X	Z

# BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

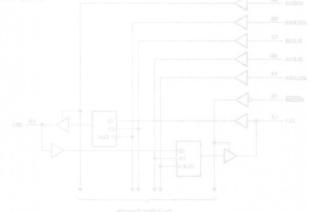
## RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVTH 3V	ALVTH 3V	LVCH 3V	ALVCH 3V	UNIT
Icc	MAX	10	5	0.02	0.04	mA
Іон	MAX	-32	-32	-24	-24	mA
lou	MAX	64	64	24	24	mA

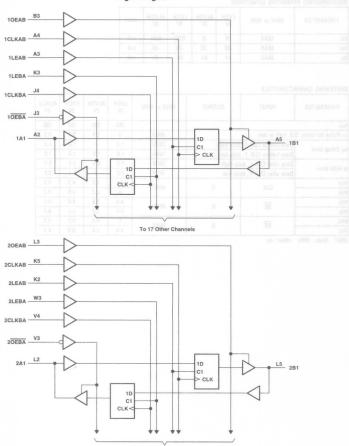
## SWITCHING CHARACTERISTICS

OTTITION OF							
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	ALVTH 3V	LVCH 3V	ALVCH 3V
fmax				160	250	150	150
tw Pulse duration, CLK high or low			MIN	3	1.5	3.3	3.3
t <sub>su</sub> Setup time	Data before CLK ↑, data high		MIN	1.8	1	1.9	1.9
	Data before CLK ↑, data low		MIN	1.8	1.5	1.9	1.9
	Data after CLK ↑, data high		MIN	0.8	0.5	1.1	0.5
th Hold time	Data after CLK ↑, da	ata low	MIN	0.8	1	1.1	0.5
tPLH .	CLK		MAY	4.5	3.2	4.5	4.2
tphl .	CLK	a	MAX	4	3.2	4.5	4.2
tpzH	ŌE		MAN	4.5	3.8	4.6	4.8
tPZL	UE	OE Q MAX		4.4	3.3	4.6	4.8
tPHZ	- Y	OE Q		5	4.6	5.5	4.3
tPLZ	UE	Q	MAX	4.6	4.2	5.5	4.3

UNIT fmax: MHz other: ns



## **Logic Diagram**



To 17 Other Channels

## **FUNCTION TABLE**†

INPUTS				OUTPUT	
OEAB	LEAB CLKA		Α	В	
input o	onditions	efore the were est	lablished,	steady-state provided that low	

SERIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUT

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABTH	ALVCH 3V	UNIT
lec	MAX	90	0.02	mA
Юн	MAX	-32	-24	mA
lou	MAX	64	24	mA

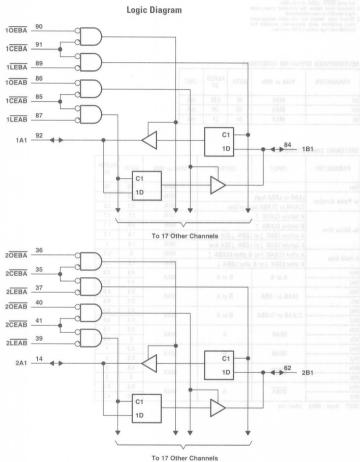
#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH	ALVCH 3V		
fmax		$-\langle -$	MIN	150	150		
tw Pulse duration	LEAB or LEBA high		MIN	3.3	3.3		
tw ruise duration	CLKAB or CLKBA high	or low	MIN	3.3	3.3		
	A before CLKAB ↑		MIN	3.5	1.7		
tsu Setup time	B before CLKBA ↑		MIN	3.5	1.7		
su Setup time	A before LEAB ↓ or LE	BA J CLK high	MIN	1.6	1.5		
	A before LEAB ↓ or LE	BA JCLK low	MIN	1.6	1		
th Hold time	A after CLKAB ↑ or B after CLKBA ↑		MIN	0	0.7		
th Hold time	A after LEAB ↓ or B at	fter LEBA ↓	MIN	1.6	1.4		
tplh	A or B	B or A	MAY	4.8	3.9		
tphl .	AOID	D OF A	MAX	5.4	3.9		
tPZH	LEAB or LEBA	B or A	MAX	5.3	4.6		
tPZL .	LEAD OF LEDA	D OF A	IVIAA	5.5	4.6		
tphz	CLKAB or CLKBA	B or A	MAX	5.3	4.9		
tPLZ	CLAB OF CLABA	D OF A	IVIAA	5.4	4.9		
tPZH	OEAB	В	MAX	5.6	4.6		
tPZL	UEAB	D	IVIAA	6	4.6		
tPHZ	OEAB	D	MAX	5.9	5		
tPLZ	UEAD	В	IVIAA	5.6	5		
tPZH -	OEBA	A	MAX	5.6	5		
tPZL	UEDA		IVIAA	6	5		
tPHZ	OEBA	A	MAX	5.9	4.2		
tPLZ	UEBA	A	IVIAA	5.6	4.2		

UNIT fmax: MHz other:ns

## **36-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS**





FUNCTION TABLE

	INP	OUTPUT		
CEAB	LEAB	OEAB	Α	Y
Н	X	X	X	Z
X	X	H	X	Z
L	Н	L	X	B <sub>0</sub> ‡
L	L	L	L	Ľ
L	L	L	H	H

† A-to-B data flow is shown: B-to-A flow conditions is the same that it uses CEBA, LEBA, and OEBA. † Outoput level before the indicated steady-state input conditions were established

## RECOMMENDED OPERATING CONDITIONS

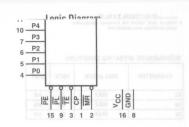
		1	1
PARAMETER	MAX or MIN	ABTH	UNIT
Icc	MAX	20	_mA
Іон	MAX	-32	mA
lo <sub>L</sub>	MAX	64	mA

#### SWITCHING CHARACTERISTICS

SWITCHING CHAI	TACTENISTICS					
PARAMETER	INPUT	DUTPUT	MAX or MIN	ABTH		
tw Pulse duration,	LEAB or LEBA low		MIN	3.3		
t Catana tima	Data before LEAB ↑	or LEBA ↑	MIN	2.1		
tsu Setup time	Data before CEAB ↑	Data before CEAB ↑ or CEBA ↑		1.7		
th Hold time	Data after LEAB ↑ or LEBA ↑		MIN	0.6		
th Hold time	Data after CEAB ↑ o	r CEBA ↑	MIN			
tPLH .	A or B	B or A	MAX	5.9		
tPHL .	A OF B	D OF A	IVIAA	5.7		
tplH	LE	A or B	MAN	7.5		
tphl .	LE	AOIB	MAX	6.6		
tPZH	CE		MAX	8		
tPZL	- UE	A or B	IVIAX	8.8		
tPHZ	CE	A D	MAN	7.1		
tPLZ	Ut	A or B	MAX	7.5		
tPZH	ŌĒ	A D	MAN	7.3		
tPZL	UE	A or B	MAX	8.1		
tPHZ	ŌĒ	4 0	2447	6.5		
tPLZ	UE	A or B	MAX	6.9		

TUNCTION TABLE

UNIT: ns



## **FUNCTION TABLE**

CO	CONTROL INPUTS		CONTROL INPUTS				
MR	PL	PE	TE	PRESET MODE	ACTION		
L	X	X	L	Synchronous	Inhibit Counter		
X	H	X	L		Cownt Down		
X	X	L	L		Preset On Next Positive Clock Transition		
H	L	L	L	Asynchronously	Preset Asychronously		
H	L	H	L		Clear to Maximum Count		

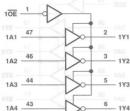
RECOMMENDED OPERATING CONDITIONS

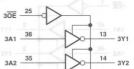
PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
lcc	MAX	0.16	0.16	mA
Іон	MAX	-4	-4	mA
lou	MAX	4	4	mA

PARAMETER	INPUT	ОИТРИТ	MAX or MIN	CD74 HC	CD74
tw		CP		50	53
		PL	MIN	38	63
		MR	1	38	53
tsu	P	to CP		30	36
	PE	to CP	MIN	22	30
	TE	to CP		45	60
th	Р	to CP	MIN	5	5
	TE	to CP		0	0
	PE	to CP		2	2
tPLH	CP CP	TC	MAX	90	90
tPHL .	CF	(Async Preset)	IVIAA	90	90
tplH .	CP TC MA		MAX	90	95
tphl.	GF.	(Sync Preset)	IVIAA	90	95
tPLH	TE	TC	MAX	60	75
tPHL	15	10	IVIAX	60	75
tPLH	PL	TC	MAX	83	102
tphl .	rL	10	IVIAA	83	102
tPLH	MR	TC	MAX	83	83
tPHL .	IVIT	16	IVIAX	83	83

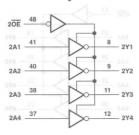
## 1622/10

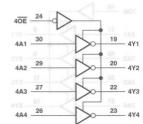
## **Logic Diagram**











## **FUNCTION TABLE**

INP	JTS	OUTPUT
OE	Α	Y
L	Н	L
L	L	H
H	X	Z

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVT 3V	LVTH 3V	UNIT
Icc	MAX	5	5	mA
Іон	MAX	-12	-12	mA
lou	MAX	12	12	mA



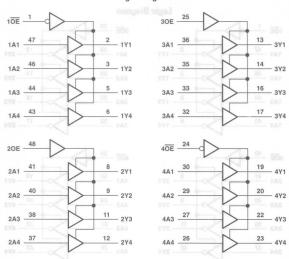
## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVT 3V	LVTH 3V
tPLH .	E # 1	V	MAN	4	4
tPHL .	A	т.	MAX	4	4
tPZH	ŌĒ	V	MANY	4.8	4.8
tPZL	UE	1	MAX	4.7	4.7
tPHZ	ŌĒ	V	MAX	4.7	4.7
tPLZ	UE	1	WAX	4.5	4.5

UNIT: ns

# 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS VINDA AREA TIAL AT THE VICE.

## Logic Diagram



## **FUNCTION TABLE**

INPU	INPUTS		
10E, 40E	1A, 4A	1Y, 4Y	
L	Н	Н	
L	L	L	
H	X	Z	

INPUT	OUTPUT	
20E, 30E	2A, 3A	2Y, 3Y
Н	Н	Н
H	L	L
L	X	Z

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVTH 3V	UNIT
lcc	MAX	5	mA
Іон	MAX	-12	mA
lou	MAX	12	mA

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V
tPLH		ν.	MAN	4.1
tPHL .	A	Y	MAX	4.1
tPZH	<u> </u>	v	1447	4.9
tPZL HTVL	OE or OE	scatal mass	MAX	4.8
tPHZ	OE or OE	v		5.3
tPLZ	UE OF UE	Y	MAX	4.9

# 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS TUD STATE & HTDW REVISED BARTTIR-AD

- SN74LVT162244A, LVTH162244: Output Ports Have Equivalent 22-Ω Series Resistors AMSSBITMATIME
- SN74ALVTH162244: Output Ports Have Equivalent 30-Ω Series Resistors no no9-A 284528 HTM JAPANA
- SN74LVC162244A: Output Ports Have Equivalent 26-Ω Series Resistors
- SN74LVCH162244A: Output Ports Have Equivalent 26-Ω Series Resistors
- SN74ALVCH162244: Output Ports Have Equivalent 26-Ω Series Resistors

## Logic Diagram 13 3Y1 14 3Y2 3A2 35 1A2 -16\_3Y3 3A3 33 1A3 17\_3Y4 3A4 32 1A4 1Y4 20E 2A1 41 19 4Y1 8 2Y1 20 4Y2 4A2 29 2A2 22\_ 4Y3 11 2Y3 23\_ 4Y4 12 2Y4 2A4 37

# FUNCTION TABLE (each 4-bit buffer)

INP	JTS	OUTPUT
ŌE	Α	Y
L	Н	Н
L	L	L
H	X	Z

#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVT 3V	LVTH 3V	ALVTH 3V	3V	LVCH 3V	ALVCH 3V	UNIT
Icc	MAX	30	5	5	5	0.02	0.02	0.04	mA
Іон	MAX	-12	-12	-12	-12	-12	-12	-12	mA
lou	MAX	12	12	12	12	12	12	12	mA

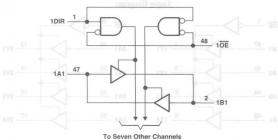
#### SWITCHING CHARACTERISTICS

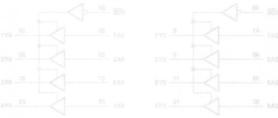
OTTIONING CHANAC	TEMOTIO									
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVT 3V	LVTH 3V	ALVTH 3V	3V LVC	TACH	ALVCH 3V
tPLH .		V	MAX	3.9	4	4	3.3	4.4	4.4	4.2
tPHL .	A	1		4.8	3.6	3.6	3.3	4.4	4.4	4.2
tPZH			1111	5.4	5.1	5.1	4.9	5.5	5.5	5.6
tPZL	0E	Y	MAX	5.1	4.5	4.5	3.3	5.5	5.5	5.6
tPHZ	ŌE		1449	4.6	5	5	4.9	6.3	6.3	5.5
tPLZ	ÜE	Y	MAX	4.5	5	5	4.3	6.3	6.3	5.5

UNIT: ns

- SIN/4EVGN10ZZ43: All Outputs have Equivalent 26-Ω Series Resistors IN amp9 augm0: AMASCR10VJATM2 @
  - SN74LVCH162244A: Output Ports Have Equivalent 26-Ω Series Resistors
  - SN74ALVCH162244: Dutput Ports Have Equivalent 26-Ω Series Resistors

## **Logic Diagram**





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RINCTION TABLE

SOUTHWIND AND DRINGTON

111-7910

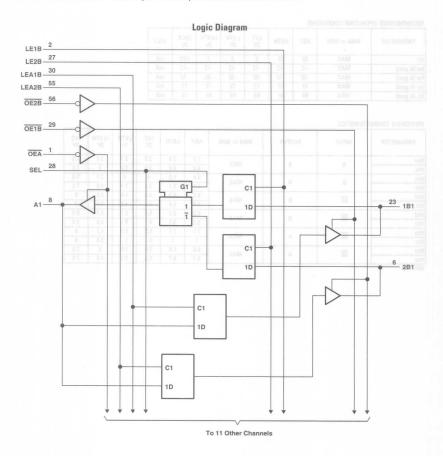
## RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ABTH	LVT 3V	LVTH 3V	ALVTH 3V	LVCR 3V	UNIT
Icc	MAX	32	32	5	5	5	0.02	mA
laн (A port)	MAX	-12	-12	-12	-12	-12	-12	mA
loн (B port)	MAX	-32	-32	-32	-32	-32	-12	mA
lot (A port)	MAX	12	12	12	12	12	12	mA
lot (B port)	MAX	64	64	64	64	64	12	mA

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ABTH	SV.	LVTH 3V	ALVTH 3V	3V
tPLH .	A		MAX	3.9	3.9	3.3	3.3	3.1	7.5
tPHL.	A	В	MAX	4.2	4.2	3.3	3.3	3	7.5
tPLH	В	А	MAN	4.6	4.6	4	4	3.7	7.5
tPHL .	В	A	MAX	5.1	5.1	3.4	3.4	3.4	7.5
tPZH	ŌE	В	AAAV	6.3	6.3	4.6	4.6	3.8	9
tPZL	UE	В	MAX	6.4	6.4	4.6	4.6	3.4	9
tPHZ	ŌĒ	В	MAX	6.3	6.3	5.2	5.2	4.7	7.5
tPLZ	UE	В	IVIAX	5.2	5.2	5.1	5.1	4.8	7.5
tPZH	ŌĒ		MAN	7.1	7.1	5.3	5.3	4.7	9
tPZL	UE	A	MAX	7	7	5.1	5.1	3.9	9
tPHZ	ŌE .		MAX	6.6	6.6	5.6	5.6	5	7.5
tPLZ	UE	A	MAX	5.7	5.7	5.5	5.5	4.9	7.5

## 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS

- lacktriangle SN74ABTH162260: B-Port Outputs Have Equivalent 25- $\Omega$  Series Resistors
- ullet SN74ALVCH162260: B-Port Outputs Have Equivalent 26- $\Omega$  Series Resistors



		_			-,			
	INPUTS OUTPUT							
1B	2B	SEL	LE1B	LE2B	OEA	A		
Н	X	Н	Н	X	L	H		
L	×	H	H	X	L	gratianis		
X	X	H	L	X	L	A <sub>0</sub>		
X	H	L	×	Н	L	H		
X	L	L	X	Н	L	L		
X	X	L	X	L	L	Ao		
X	X	X	X	X	H	Z		

A TO B (OEA = H)

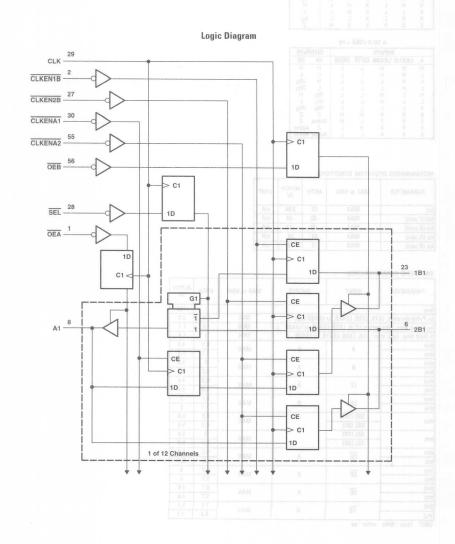
		INPUTS			OUT	PUTS
A	LEA1B	LEA2B	OE1B	OE2B	1B	2B
Н	Н	H	L	L	Н	H
L	H	H	L	L	L	L
Н	H	L	L	L	H	2B <sub>0</sub>
L	H	L	L	L	L	2B <sub>0</sub>
H	L	H	L	L	1B0	H
L	L	H	L	L	1B0	L
X	L.	L	L	L	1B0	2Bn
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABTH	ALVCH 3V	UNIT
Icc	MAX	63	0.04	mA
loн (A port)	MAX	-32	-24	mA
Iон (B port)	MAX	-32	-12	mA
IoL (A port)	MAX	64	24	mA
lot (B port)	MAX	12	12	mA

SWITCHING CHARA	CTERISTICS	- UI			_
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH	ALVCH 3V
fmax					150
tw Pulse duration, LE	1B, LE2B, LEA1B, o	r LEA2B high	MIN	3.3	3.3
tsu Setup time, data b	efore LE1B, LE2B,	MIN	1.5	1.1	
th Hold time, data aft	er LE1B, LE2B, LEA	MIN	1	1.5	
tplH .	A	MAX	6.1	4.9	
tphL .	A	В	IVIAA	7.1	4.9
tPLH	В	A	MAX	6	4.3
tPHL .	В	A	IVIAA	6.2	4.3
tPLH	LE		MAX	6.3	4.4
tphL .	LE	Agg	IVIAA	5.8	4.4
tPLH	LE	В	MAX	6.1	5
tphl.	LE	В	IVIAA	7.1	5
	SEL (1B)	- CE	MAX	5.6	5.6
tplH -	SEL (2B)	A	WAX	6.3	5.6
	SEL (1B)	A	MAX	5	5.6
tPHL -	SEL (2B)	Q1	MAX	6.2	5.6
tPZH	ŌĒ		MAX	6.3	5.4
tPZL	UE	A	MAX	6.5	5.4
tPZH	ŌE	В	MAX	6.3	6
tPZL	UE	В	IVIAX	8.2	6
tpHZ	ŌĒ		MAN	6.7	4.6
tPLZ	UE	A	MAX	5.2	4.6
tPHZ	ŌĒ	В	MAX	7.5	5.1
tpi 7	UE	В	MAX	6.2	5.1

UNIT fmax : MHz other : ns



FUNCTION TABLE OUTPUT ENABLE

19-979	NPUTS	3	OUTPUTS
CLK	OEA	OEB	A 1B, 2B
1	Н	Н	Z Z
+	H	L	Z Active
	L	H	Active Z
	L	L	Active Active

OUTPUTS
A 18 28

SW/AALVCHG18280: A-Port Outputs Have Equivalent 50-Ω Series Resist

## A-TO-B STORAGE (OEB = L)

	OUT	PUTS			
CLKENA1	CLKENA2	CLK	Α	1B	2B
Н	Н	X	X	1B <sub>0</sub> ‡	2B <sub>0</sub> ‡
L	X	1	L	L†	X
L	X	*	H	H†	X
X	L	7	L	X	L
X	L	1	H	X	H

†Two CLK edges are needed to propagate data. ‡ Output level before the indicated steady-state input conditions were established

## B-TO-A STORAGE (OEA = L)

	INPUTS					
CLKEN1B	CLKEN2B	CLK	SEL	1B	2B	A
Н	X	X	Н	X	X	An‡
×	H	X	L	X	X	An‡
L	×		H	H	X	Ľ
L	X		H	L	X	H
×	L	2	L	X	L	L
X	L		L	X	Н	H

Output level before the indicated steady-state input conditions were established.

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
Icc III	MAX	0.04	mA
loн (A port)	MAX	-24	mA
loн (B port)	MAX	-12	-mA
lot (A port)	MAX	24	mA
lot (B port)	MAX	12	mA

#### SWITCHING CHARACTERISTIC

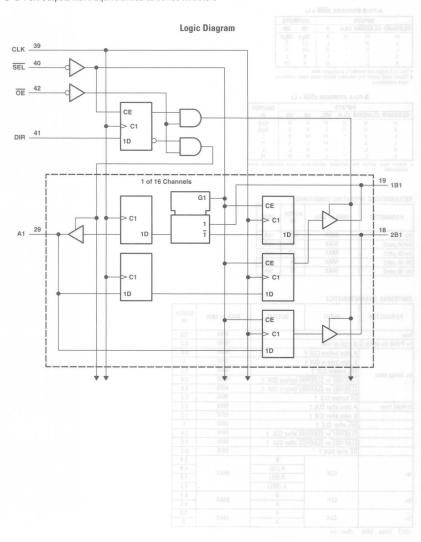
PARAMETER	INPUT	ОИТРИТ	MAX or MIN	ALVCH 3V
fmax		10 <	MIN	150
tw Pulse duration,	CLK high or low		MIN	3.3
	A data before CLK	MIN	3.4	
	B data before CLK		MIN	1
t <sub>su</sub> Setup time	SEL before CLK ↑	MIN	1.3	
	CLKENA1 or CLKEN	MIN	2.8	
	CLKENB1 or CLKEN	MIN	2.5	
	OE before CLK ↑	MIN	3.2	
th Hold time	A data after CLK ↑	MIN	0.2	
	B data after CLK ↑	MIN	1.3	
	SEL after CLK ↑	MIN	1	
	CLKENA1 or CLKEN	MIN	0.4	
	CLKENB1 or CLKEN	MIN	0.5	
	OE after CLK ↑		MIN	0.2
		В		5.4
tod	CLK	A (1B)	MAX	4.8
гра	GLK	A (2B)	IVIAA	4.8
		A (SEL)	1	5.8
ten	CLK	В	MAX	6.1
Len	ULK	A	IVIAA	5.1
İtdis	CLK	В	MAX	5.9
LOIS	GLK	A	IVIAX	5

UNIT fmax: MHz other:ns

TO BIT TO BE BIT HEGIOTERED DOO EXCHANGER WITH BITTE MACKO AND O

lacktriangle SN74ALVCHG162280: A-Port Outputs Have Equivalent 50- $\Omega$  Series Resistors

B-Port Outputs Have Equivalent 20-Ω Series Resistors



## **FUNCTION TABLE**

## A-TO-B STORAGE (OE = L, DIR = H)

	NPUTS		OUTI	PUTS
SEL	CLK	Α	1B	2B
Н	X	X	1B <sub>0</sub> †	2Bot
L		L	L‡	X
L		H	H±	X

## B-TO-A STORAGE (OE = L, DIR = L)

OUTPUT		INPUTS				
A	2B	1B	SEL	CLK		
L§	L	X	Н	1		
HŞ	H	X	H	1		
L	×	L	L	1		
H	X	H	L	1		

<sup>§</sup> Two CLK edges are needed to propagate the data. The data is loaded in the first register when SEL is low and propagates to the second register when SEL is high.

## C-TO-D STORAGE (OE = L)

INPUTS		OUTPUT		
SEL	CLK	С	1D	2D
Н	X	X	1Bot	2B <sub>0</sub> 1
L	1	L	L‡	L
L	1	H	H‡	H

<sup>†</sup> Output level before indicated steady-state input conditions were established ‡ Two CLK edges are needed to propagate the data.

## OUTPUT ENABLE

INPUTS		-	Г		
CLK	OE	DIR	A	1B, 2B	1D, 2D
1	Н	X	Z	Z	Z
1	L	H	Z	Active	Active
1	E.	1 L	Active	Z	Active

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCHG 3V	UNIT
Icc	MAX	0.04	mA
Ion (A to B)	MAX	8	mA
Ioн (В to A)	MAX	6	mA
IoL (A to B)	MAX	8	mA
lot (B to A)	MAX	6	mA

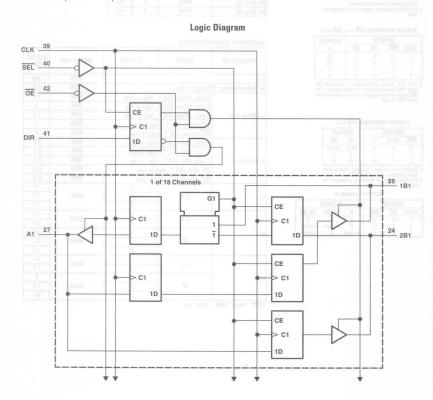
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCHG 3V
fmax			MIN	160
tw Pulse duration,	CLK high or low		MIN	2.3
	A data before CLK	1, high or low	MIN	1.4
	B data before CLK	1, high or low	MIN	2
tsu Setup time	C data before CLK	T, high or low	MIN	1.3
	DIR before CLK 1,	high or low	MIN	2
	SEL before CLK 1,	high or low	MIN	2
	A data after CLK T	, high or low	MIN	0.3
	B data after CLK T	, high or low	MIN	0.3
th Hold time	C data after CLK 1	, high or low	MIN	0.3
	DIR after CLK 1, hi	gh or low	MIN	0.3
	SEL after CLK 1, h	igh or low	MIN	0.3
		A		5
tpd	CLK	В	MAX	7.4
		D		7.2
	CLK	A	MAX	6.2
	ULK	В	IVIAA	9.4
ten	7	A		6
	0E	В	MAX	9.5
		D		7.9
	CLK	A	MAX	6.4
	CLK	В	IVIAA	7.8
ldis		A		5
	ŌE	В	MAX	7.6
		D	1	6.7

UNIT fmax: MHz other: ns

<sup>†</sup> Output level before indicated steady-state input conditions were established ‡ Two CLK edges are needed to propagate the data.

## 18-BIT TO 36-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

- ullet SN74ALVCHG162282: A-Port Outputs Have Equivalent 50- $\Omega$  Series Resistors
- B-Port Outputs Have Equivalent 20-Ω Series Resistors



Output level before indicated steady-state input conditions were established
 Two CLK edges are needed to propagate the data.

B-TO-A STORAGE (OE = L, DIR = L)

	INP	UTS		OUTPUT
CLK	SEL	1B	2B	Α
1	Н	X	L	L§
1	H	X	H	H§
1	L	L	X	L
1	100	H	X	H

§ Two CLK edges are needed to propagate the data. The data is loaded in the first register when SEL is low and proparates to the second register when SEL is high.

#### OUTPUT ENABLE

INPUTS			OUTPUTS	
CLK	OE	DIR	A	1B, 2B
Ť	Н	X	Z	Z
1	L	H	Z	Active
1	L	L	Active	Z

lot (A to B)	MAX	8	mA
IoL (B to A)	MAX	6	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCHG 3V
fmax		74,50	MIN	160
tw Pulse duration,	CLK high or low	A 20	MIN	2.3
	A data before CLK 1	b 31	MIN	1.5
tsu Setup time	B data before CLK 1	4	MIN	2
isa Setup time	DIR before CLK 1	7 70	MIN	2
9	SEL before CLK 1	120	MIN	2
	A data after CLK 1		MIN	0.3
th Hold time	B data after CLK 1		MIN	0.3
in Hold tillle	DIR after CLK 1		MIN	0.3
	SEL after CLK↑		MIN	0.3
tod	CLK	A	MAX	5
tpo.	CER	В	IVIAA	7.4
alamani Ph	CLK	A	MAX	6.3
ten	GEK	В	IVIAA	9.4
Len	ŌĒ	A	MAX	6
	ÜE.	В	IVIAA	9.5
	CLK	A	MAX	6.4
tdis	OLK	В	IVIAA	7.8
toria .	ŌĒ	A	MAX	5
	J.	В	1	7.6

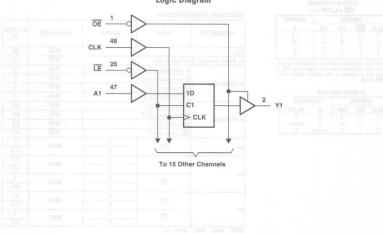
UNIT fmax : MHz other : ns

## 162334

## **16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS**

- ullet SN74ALVC162334: Output Ports Have Equivalent 26- $\Omega$  Series Resistors
- SN74ALVCH162334: Output Port Has Equivalent 26-Ω Series Resistors

## **Logic Diagram**



**FUNCTION TABLE** 

	INPUTS			OUTPUT
OE	LE	CLK	Α	Υ
Н	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	1	L	L
L	H	+	H	H
L	H	LorH	X	Yot

† Output level before the indicated steady-state input conditions were established

RECOMMENDED	OPERATING	CONDITIONS

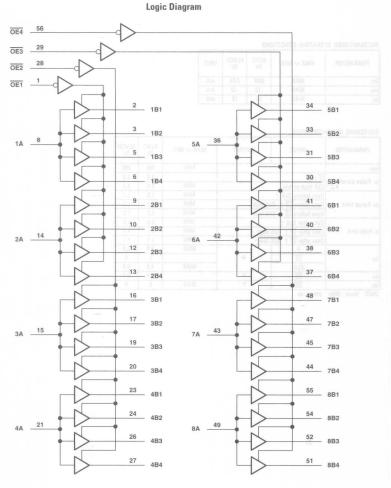
PARAMETER	MAX or MIN	ALVC 3V	ALVCH 3V	UNIT
Icc	MAX	0.04	0.04	mA
Іон	MAX	-12	-12	mA
lou	MAX	12	12	mA

## SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC 3V	ALVCH 3V	
fmax			MIN	150	150	
tw Pulse duration	LE low			3.3	3.3	
tw Pulse duration	CLK high or low		MIN	3.3	3.3	
	Data before CLK ↑		MIN	1.5	1.5	
tsu Setup time	Data before LE ↑ CI	K high	MIN	1.3	1.3	
	Data before LE ↑ CI	K low	MIN	1.2	1.2	
	Data after CLK ↑	100	MIN	0.9	0.9	
th Hold time	Data after LE ↑ CLK	high	MIN	1.1	1.1	
	Data after LE ↑ CLK	low	MIN	1.1	1.1	
15897	A A		MAX	3.9	3.9	
tpd	ĪĒ	Y		5	5	
	CLK		MAX	4.9	4.9	
ten	ŌĒ	Y		5.4	5.4	
tdis	ŌĒ	Υ	MAX	5	5	

UNIT fmax: MHz other: ns





## FUNCTION TABLE mangel@ sign.l

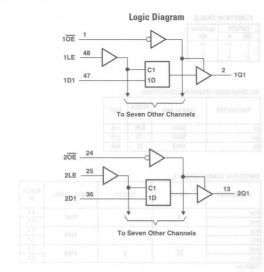
PARAMETER	MAX or MIN	ALVCH 3V	UNIT	
Icc	MAX	0.04	mA	
Іон	MAX	-12	mA	
lou	MAX	12	mA	

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
tPLH		-	MAX	4.4
tphl.	A	В	IVIAX	4.4
tpzH	25	D agva2 <sub>B</sub> T	MANY	5.7
tPZL	UE	В	MAX	5.7
tPHZ	ŌĒ	В	MAX	4.5
tPLZ	UE	D D	IVIAA	4.5

## 162373

## 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

 SN74LVTH162373: Output Ports Have Equivalent 22-Ω Series Resistors



#### FUNCTION TABLE (each 8-bit section)

1	INPUTS		OUTPUT
OE	LE	D	Q
L	Н	Н	Н
L	H	L	L
L	L	X	Qn
H	X	X	Z

## RECOMMENDED OPERATING CONDITIONS

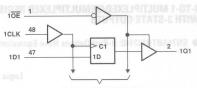
PARAMETER	MAX or MIN	LVTH 3V	UNIT
Icc	MAX	5	mA
Іон	MAX	-12	mA
lou	MAX	12	mA

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V
tw Pulse duration,	LE high or low		MIN	3
. Catua tima	Data before LE 1, d	lata high	MIN	1
tsu Setup time	Data before LE 1, d	lata low	MIN	1
e Hallaton	Data after LE 1, dat	ta high	MIN	1
th Hold time	Data after LE ↓, dat	ta low	MIN	1
tPLH	D	0	MAX	4.6
tPHL .		u	IVIAA	4
tplH	LE	0	MAX	5.1
tphL .	LE	u	IVIAX	4.6
tpzh	- OE	0	MANY	5.4
tPZL	T UE	u	MAX	4.9
tPHZ	- OE	0	BAAV	5.4
tPLZ	OE OE	u	MAX	5.1

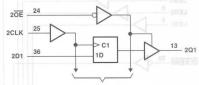
## **Logic Diagram**

## 3.3-V ABT 16-BIT EDGE-TRIGGERED **D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS**

- SN74LVTH162374: Output Ports Have Equivalent 22-Ω Series Resistors
- SN74ALVCH162374: Output Ports Have Equivalent 26-Ω Series Resistors



To Seven Other Channels



To Seven Other Channels

**FUNCTION TABLE** (each fllp-flop)

	INPUTS		OUTPUT
ŌE	CLK	D	Q
L	1	Н	H
L	1	L	30 L-
L	L	X	Qn
H	X	X	Z

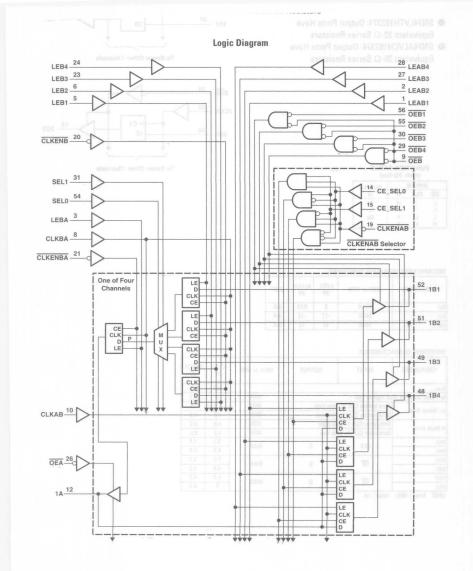
RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVTH 3V	ALVCH 3V	UNIT	
Icc	MAX	5	0.04	mA	
Іон	MAX	-12	-12	mA	
lou	MAX	12	12	mA	

## SWITCHING CHARACTERISTICS

UNIT fmax: MHz other: ns

	MAGTEMOTICO				-
PARAMETER	INPUT	ОИТРИТ	MAX or MIN	LVTH 3V	ALVCH 3V
fmax	4			160	150
tw Pulse duration	CLK high or low		MIN	3	3.3
	Data before CLK 1,	MIN	1.8	1.9	
tsu Setup time	Data before CLK 1,	data low	MIN	1.8	1.9
	Data after CLK 1, d	ata high	MIN	0.8	0.5
th Hold time	Data after CLK 1, d	ata low	MIN	0.8	0.5
tPLH	CLK	0		5.3	4.6
tPHL .	ULK NAME	u	MAX	4.9	4.6
tPZH	OF.			5.6	5.2
tPZL	OE Q		MAX	4.9	5.2
tPHZ			MAN	5.4	4.5
tPLZ	OE OLIS	Q	MAX	5	4.5



†n = 1, 2, 3, 4

#### B-TO-A STORAGE (after point P)

Р				S	INPUT														
Р	SEL0	SEL1	LEB4	LEB3	LEB2	LEB1	CLKBA	CLKENB											
B1	L	L	L	L	L	Н	X	X											
B2	H	L	L	L	H	L	X	X											
B3	L	H	L	H	L	L	X	X											
B4	H	H	H	L	L	L	X	X											
B1	L	L																	
B2	H	L	v		L														
B3	L	H	L	_		L	L	-	-	L	-	-	-	-	_	L	L	*	L
B4	H	H																	
B1 <sub>0</sub> † B2 <sub>0</sub> † B3 <sub>0</sub> † B4 <sub>0</sub> †	L	L																	
B201	H	L		1															
B301	L	H	L	L	L	L	L	L											
B401	H	H																	

B-TO-A STORAGE (after point P)

	INF	UTS			OUTPUT
CLKENBA	CLKBA	LEBA	OEA	В	A
X	X	X	H	X	X
X	X	H	L	L	L
×	X	H	L	H	H
H	X	L	L	X	Aot
L	*	L	L	L	L
L		L	L	H	H
L	L	L	L	X	Apt



PARAMETER	MAX or MIN	ABTH	UNIT
Icc	MAX	32	mA
lon (A port)	MAX	-32	mA
loн (B port)	MAX	-12	mA
lot (A port)	MAX	64	mA
lor (B port)	MAX	12	mA

# 18 10 XID

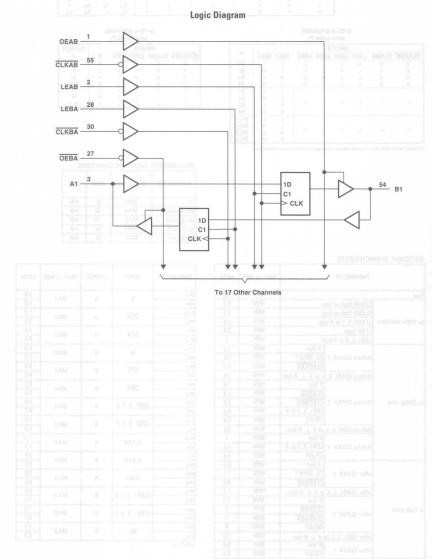
	PARAMETER		MAX or MIN	ABTH	
fmax			MIN	160	
	CLKAB high or lo	w	MIN	3.8	
	CLKBA high or lo	CLKBA high or low			
tw Pulse duration	LEAB1, 2, 3 or 4 h	igh	MIN	2.8	
	LEBA high		MIN	2.8	
	LEB1, 2, 3 or 4 hig	jh	MIN	3	
		A bus	MIN	2.5	
	Before CLKAB ↑	CE_SEL0/1	MIN	3.2	
		CLKENAB	MIN	3.2	
	Before LEAB1, 2,	Before LEAB1, 2, 3, or 4 ↓ A bus			
		B bus	MIN	3.8	
		CLKENB	MIN	2.3	
tsu Setup time	Before CLKBA ↑	CLKENBA	MIN	2.5	
		LEB1, 2, 3 or 4	MIN	4.3	
		SEL0/1	MIN	4.5	
	Before LEB1, 2, 3	MIN	3.2		
		B bus	MIN	4	
	Before CLKBA ↑	LEB1, 2, 3 or 4	MIN	4.4	
		SEL0/1	MIN	4.3	
		A bus	MIN	0.5	
	after CLKAB ↑	CE_SEL0/1	MIN	1.1	
		CLKENAB	MIN	0.5	
	after LEAB1, 2, 3,	or 4   A bus	MIN	1.2	
		B bus	MIN	1.3	
th Hold time	after CLKBA ↑	CLKENB	MIN	1	
	atter CERBA T	CLKENBA	MIN	1	
		SEL0/1	MIN	0	
	after LEB1, 2, 3, c	r 4 ↓ B bus	MIN	1.5	
	-G OLVDA A	B bus	MIN	0.4	
	after CLKBA ↑	SEL0/1	MIN	0.1	

		1		
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH
tPLH .	В	А	MAX	6.5
tPHL				6.5
tрzн	ŌĒĀ	А	MAX	5.6
tPZL				5.5
tPHZ	0EA	А	MAX	5.9
tPLZ				6.5
tPLH .	А	В	MAX	6.2
<b>TPHL</b>				6.5
tPZH	OEB	В	MAX	6.8
tPZL				6.3
tphz .	OEB	В	MAX	6.2
tPLZ				5.8
tPZH	OEB1, 2, 3, 4	В	MAX	- 6.6
tPZL				6.2
tPHZ	ŌEB1, 2, 3, 4	В	MAX	5.3
tPLZ				4.9
tPLH	CLKBA	А	MAX	7.4
tPHL				7.7
<b>TPLH</b>	CLKAB	В	MAX	6.5
TPHL				6.5
tPLH .	LEBA	А	MAX	5.8
<b>TPHL</b>				5.8
tPLH	LEAB1, 2, 3, 4	В	MAX	6.2
tPHL .				6.2
tPLH	LEBA1, 2, 3, 4	А	MAX	7.2
tPHL .				6.8
tplh	SEL	А	MAX	7.5
tPHL .				6.9

<sup>†</sup> Output level before the indicated steady-state input conditions were established

### 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

ullet SN74ABT162500: B-Port Outputs Have Equivalent 25- $\Omega$  Series Resistors



**FUNCTION TABLE** 

	INP	UTS		OUTPUT
OEAB	LEAB	CLKAB	Α	В
L	X	X	X	Z
Н	H	×	L	L
Н	H	X	H	H
Н	L	1	L	L S
Н	L	1	H	H
Н	L	H	X	B <sub>0</sub> ‡
H	L	L	X	Bo§

Cutput level before the indicated steady-state input conditions were established.
 Soutput level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

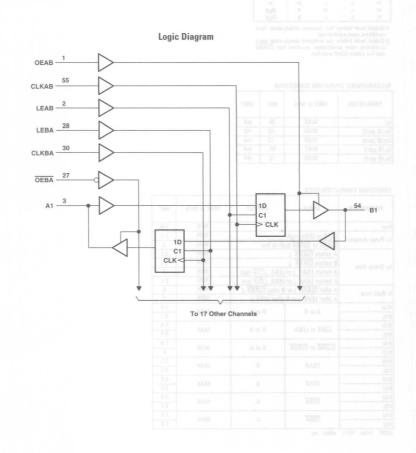
#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
Icc	MAX	36	mA
loн (A port)	MAX	-32	mA
loн (B port)	MAX	-12	mA
lot (A port)	MAX	64	mA
lor (B bort)	MAX	12	mA

SWITCHING CHAI	RACTERISTICS				
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	
fmax		7LID <	MIN	150	
tw Pulse duration	LEAB or LEBA high		MIN	2.5	
tw ruise duration	CLKAB or CLKBA high	or low	MIN	3	
	A before CLKAB ↓		MIN	3.3	
t. Catua tima	B before CLKBA ↓		MIN	3.3	
tsu Setup time	A before LEAB ↓ or LE	BA ↓ CLK high	MIN	1	
	A before LEAB 1 or LE	BA J CLK low	MIN	2.5	
th Hold time	A after CLKAB J or B	after CLKBA ↓	MIN	0	
th Hold time	A after CLKAB ↓ or B after CLKBA ↓  A after LEAB ↓ or B after LEBA ↓  A or B B or A		MIN	2	
tPLH .	A es D	STEETING OF BUILDING		4.8	
tPHL .	Aorb	B OF A	MAX	5.7	
tPZH	LEAB or LEBA	B or A	MAX	5.6	
tPZL	LEAD OF LEDA	D UI A	IVIAA	5.9	
tPHZ	CLKAB or CLKBA	B or A	MAX	5.9	
tPLZ	CLNAD OF CLNDA	D UI A	IVIAA	6	
tPZH	OFAB	В	MAX	5.3	
tPZL	UEAD	D	IVIAA	5.4	
tPHZ	OEAB	B	MAX	6.5	
tPLZ	UEAD	Ь	IVIAX	5.8	
tPZH	OEBA	A	MAX	5.3	
tPZL	ULDA	A	IVIAA	5.4	
tPHZ	- OEBA	A	MAX	6.5	
tPLZ	UEBA	A	IVIAX	5.8	

## 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SN74ABT162501: B-Port Outputs Have Equivalent 25-Ω Series Resistors



#### **FUNCTION TABLE**†

	INP	OUTPUT		
OEAB	LEAB	CLKAB	Α	Y
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	1	L	L
H	L	*	H	H
H	L	H	X	B <sub>0</sub> ‡
H	L	L	X	Bo§

H L X BOS

A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

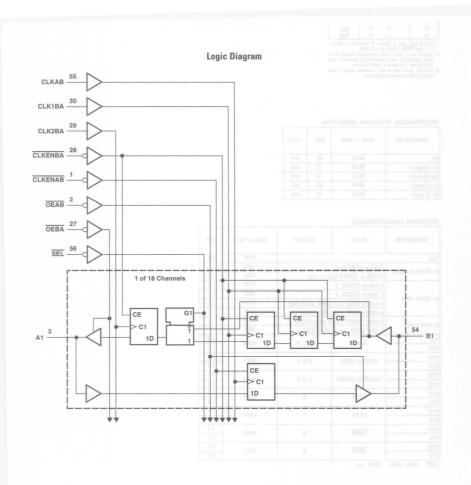
Output leveb before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAP went low

Output leveb before the indicated steady-state input conditions were established.

#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
Icc	MAX	36	mA
loн (A port)	MAX	-32	mA
Iон (B port)	MAX	-12	mA
lot (A port)	MAX	64	mA
lor (B port)	MAX	12	mA

SWITCHING CHAP	RACTERISTICS			
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
fmax			MIN	150
tw Pulse duration	LEAB or LEBA high		MIN	3
tw ruise duration	CLKAB or CLKBA high	or low	MIN	3.3
	A before CLKAB ↑		MIN	4.3
t. Catua tima	B before CLKBA ↑		MIN	4.3
tsu Setup time	A before LEAB ↓ or L	EBA J CLK high	MIN	2.5
	A before LEAB ↓ or L		MIN	1
th Hold time	A after CLKAB † or B	after CLKBA ↑	MIN	0
th Hold time	A after LEAB ↓ or B a			2
tPLH -			MAX	4.8
tPHL	A or B	B or A	IVIAX	5.7
tPZH	LEAB or LEBA	B or A	MAX	5.6
tPZL · · ·	LEAD OF LEBA	B OF A	IVIAX	5.9
tPHZ	CLKAB or CLKBA	B or A	MAX	5.5
tPLZ	CLKAB OF CLKBA	B OF A	WAA	5.3
tPZH	OEAB	В	MAX	5.3
tPZL	UEAB	В	IVIAA	5.4
tPHZ	OEAB	В	MAX	6.5
tPLZ	UEAD	В	WAX	5.8
tPZH	OEBA	Α	MAX	5.3
tPZL.	UEDA	A	WAA	5.4
tPHZ	- OEBA	А	MAX	6.5
tPLZ	UEBA	A	IVIAX	5.8



#### **FUNCTION TABLE**

A-TO-B STORAGE(OEAB=L)

	OUTPUT		
CLKNAB	OLKAB	Α	В
Н	X	X	B <sub>0</sub> †
L	*	L	L
L	†	H	H

† Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE (OFBA - I)

	INPUTS					
CLKENBA	CLK2BA	CLK1BA	SEL	В	A	
Н	X	X	X	X	Ant	
L	*	X	H	L	L	
L	+	X	H	H	Н	
L	1	+	L	L	L‡	
L.	1	+	L	Н	H‡	

were established
 Three CLK1BA edges and one CLK2BA edge are needed to propagate data from B to A when SEL is low.

RECOMMENDED OPERATING CONDITIONS



WITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
fmax			MIN	150
tw Pulse duration,	CLK high or low		MIN	3
	A data before CLKA	AB ↑	MIN	1.3
	B data before CLK2	BA ↑	MIN	1.7
	B data before CLK1	BA ↑	MIN	1.1
tsu Setup time	SEL before CLK2BA	1	MIN	3.3
	CLKENAB before C	LKAB ↑	MIN	1.6
	CLKENBA before C	LK1BA ↑	MIN	2.1
	CLKENBA before C	LK2BA ↑	MIN	2.2
	A data after CLKAB	1	MIN	0.9
	B data after CLK2B	data after CLK2BA ↑		0.6
	B data after CLK1BA ↑		MIN	1
th Hold time	SEL after CLK2BA ↑		MIN	0.1
	CLKENAB after CLK	KENAB after CLKAB ↑		0.3
	CLKENBA after CLI	K1BA ↑	MIN	0.1
	CLKENBA after CLF	K2BA ↑	MIN	0
Ind	CLKAB	В	MAX	4.7
rba .	CLK2BA	A	IVIAA	4.2
ten	OEBA	A	MAX	5.1
ten	OEAB	В	IVIAA	5.7
tdis	OEBA	А	MAX	4.9
tdis	OEAB	В	IVIAX	4.9

UNIT fmax: MHz other: ns

■ SN74LVTH162541: Output Ports Have Equivalent 22-Ω Series Resistors

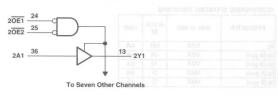
### 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

 $\bullet~$  SN74LVTH162541: Output Ports Have Equivalent 22- $\Omega$  Series Resistors

#### PUNCTION TABLE

A TO-P STORAGE(OEAR-L)

To Seven Other Channels



OUTPUT

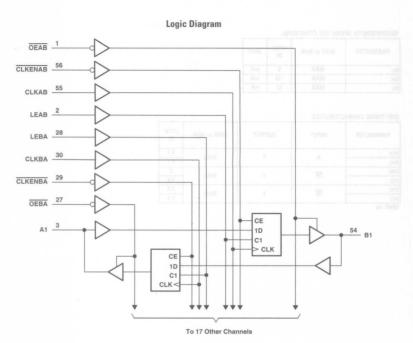
INPUTS

OE1 OE2 A

RECOMMENDED OF	PERATING CONDIT	21101					
PARAMETER	MAX or MIN	LVTH 3V	UNIT				
Icc	MAX	5	mA				
Іон	MAX	-12	mA				
lor	MAX	12	mA				
SWITCHING CHARA	ACTERISTICS	01	TPUT	MAX or MIN	LVTH 3V		
tPLH .		-		33,80	4.1		
tPHL .	A		Υ	MAX	4.1		
tPZH	ŌĒ		Υ	MAX	-5		
tPZL	UE		Y	MAX	4.8		
tphz	ŌĒ		Υ	MAX	5.9		
tPLZ	02			Wirth	5.4		
UNIT: ns							

- CNITABITADOS DE
- SN74ABT162601: B-Port Outputs Have Equivalent 25- $\Omega$  Series Resistors SN74ALVCH162601: B-Port Outputs Have Equivalent 26- $\Omega$  Series Resistors





FUNCTION TABLE

	INPUTS							
CLKENAB	OEAB	LEAB	CLKAB	Ā	OUTPUT			
X	Н	X	X	X	Z			
×	L	H	×	L	L			
×	L	Н	×	H	H			
Н	L	L	X	X	Bo‡			
Н	L	L	×	X	Bo‡			
L	L	L		L	L			
L	L	L		H	H			
L	L	- OL	L	X	Bo‡			
1	1.	1	H	Y	Bo8			

† A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA. † Output level before the indicated steady-state input conditions were established.

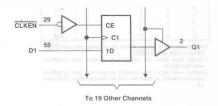
§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ALVCH 3V	UNIT
Icc	MAX	36	0.04	mA
Iон (A port)	MAX	-32	-24	mA
loн (B port)	MAX	-12	-12	mA
loL (A port)	MAX	64	24	mA
lot (B port)	MAX	12	12	mA

#### CHARTCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ALVCH 3V	
fmax			MIN	150	150	
	LEAB or LEBA high		MIN	2.5	3.3	
tw Pulse duration	CLKAB or CLKBA high o	MIN   15	3	3.3		
	Data before CLK ↑		MIN	4.3	2.1	
	A before LEAB ↓ or B be	efore LEBA J, CLK high	MIN	2.5	1.6	
tsu Setup time	A before LEAB 1 or B be	efore LEBA J, CLK low	MIN	1	1.1	
	CLKEN before ↑		MIN	2.7	1.7	
	Data after CLK ↑		MIN	0	0.8	
	A after LEAB ↓ or B afte	r LEBA 1. CLK high	MIN	0.5	1.4	
th Hold time	A after LEAB ↓ or B afte		MIN	0.5	1.7	
	CLKEN after ↑		MIN	0	0.6	
tPLH		1131	IA STREET, SON	4.8	4.5	
tPHL.	A	В	WAX	5.7	4.5	
tPLH		. 0	ALL DELINA	4	4.1	
tphl .	В	A	MAX	4.9	4.1	CLIC megh or law
tplh	1504	. 1		5	4.7	Date before O.K. 1
tPHL .	LEBA	A	MAX	5	4.7	CLAST Instant VISIO
tPLH	LEAB			5.6	5.1	1 XQ0 refts areQ
tphL .	LEAB	В	MAX	5.9	5.1	1 X I3 min V5XID
tPLH	CLKBA		MANY	5.3	5	
tPHL	CLKBA	A	IVIAX	5	5	9633
tplH	CLKAB	D	MAN	5.5	5.5	
tphL .	CLKAB	D	IVIAX	5.3	5.5	30 4
tPZH	- OEBA		MAN	5.1	5.2	
tPZL	UEBA	A	MAX	5.4	5.2	30 -
tPZH	OEAB		MAN	6.1	5.7	un tadio
tPZL	UEAB	В	MAX	5.7	5.7	
tphz .	DEBA		1447	6.2	4.4	
tPLZ	UEBA	A	WAX	5.4	4.4	
tphz	OEAB .	D	MANY	5.4	4.8	
TPLZ	UEAB	R	MAX	5.2	4.8	1



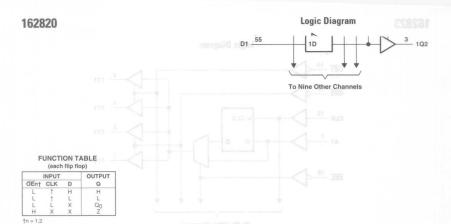
FUNCTION TABLE

		- (	each fl	ip-flop)	
		INP	UTS		OUTPUT
O	E CI	KEN	CLK	D	Q
L		Н	X	X	Q <sub>0</sub>
L		L	*	H	H
L		L	*	L	L
L		L	LorH	X	Qn
H		X	X	-X-	Z

	RECOMMENDED	OPERATING	CONDITIONS	
--	-------------	-----------	------------	--

NECOMMENDED OF	PERATING CUNDIT	101/15	
PARAMETER	MAX or MIN	ALVCH 3V	UNIT
lcc -	MAX	0.04	mA
Іон	MAX	-12	mA
lou	MAX	12	mA

SWITCHING CHARACTERISTICS								
	T	8.0	-	\$1746		1		
PARAMETER	INPUT	OUTPUT	8.5	MAX or MIN	ALVCH 3V	8		
			Til		30			
fmax		(3)	- 6	MIN	150	A		
tw Pulse duration	CLK high or low	12:01	. 2 .	MIN	3.3			
tsu Setup time	Data before CLK ↑	1,3	10	MIN	3.1	A		
isii Setup time	CLKEN before CLK ↑	1.2	2.	MIN	2.7			
th Hold time	Data after CLK ↑	150	0.0	MIN	0	18		
in noid time	CLKEN after CLK ↑	1.5	8.	MIN	0			
tPLH .	CLK	a	- 5	MAX	5.3	Α.		
TPHL	CER	u	8	IVIAA	5.3			
tPZH .	- OE	Q	935	MAX	5.8			
tPZL	OL.	ч	8.	IVIAA	5.8			
<b>TPHZ</b>	OE	0		MAX	5	70		
tPLZ	OL.	0	200	WIAA	5			
UNIT fmax: MHz	other : ns							



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT	
Icc	MAX	0.04	mA	
Іон	MAX	-12	mA	
lor	MAX	12	mA	
			1966	

#### SWITCHING CHARACTERISTICS

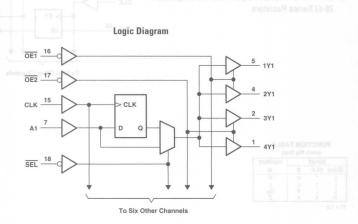
INPUT	OUTPUT	MAX or MIN	ALVCH 3V
		MIN	150
CLK high or low	THEIRIG	MIN	3.3
Data before CLK ↑		MIN	1.4
Data after CLK ↑		MIN	1
THE CLE	0	AAAV	5.4
CLK	u	IVIAX	5.4
MILL OF	0	MAN	5.6
UE	u	MAX	5.6
OF THE PERSON NAMED IN COLUMN TWO IS NOT THE PERSON NAMED IN COLUMN TO THE PERSON NAMED IN COLUM	0.000	MAN	5
UE	U AND E	WAX	5
	CLK high or low Data before CLK ↑	CLK high or low  Data before CLK ↑  Data after CLK ↑  CLK Q  OE Q	MIN   MIN   MIN

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty.
Production processing does not passessily include testing of all parameters. See wasky ti com/secllonic for the most current data sheats

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## 18-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS AND HOM 90.8-91.8 TIB-01 V-C.E

SN74ABT162823A: Output Ports Have Equivalent 25-Ω Series Resistors



**FUNCTION TABLE** 

		OUTPUT			
OE	CLR	CLENK	CLK	D	Q
L	L	X	X	X	L
L	H	L	+	H	Н
L	H	L	1	L	L
L	H	L	L	X	Qn
L	H	H	X	X	Qo
H	X	X	X	X	Z

RECOMMENDED OPERATING CONDITIONS

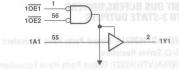
PARAMETER	MAX or MIN	ABT	UNIT
Icc	MAX	80	mA
Іон	MAX	-12	mA
lou	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
fmax	1000		MIN	150
tw Pulse duration	CLR low	D	MIN	3.3
tw Pulse duration	CLK high or low		MIN	3.3
	CLR inactive		MIN	1.6
tsu Setup time	Data before CLK ↑		MIN	2
	CLKEN low before	CLK ↑	MIN	2.8
th Hold time	Data after CLK ↑		MIN	1.2
th Hold time	CLKEN low after CL	K ↑	MIN	0.6
tPLH	CIV	0	MAN	7.5
tphl .	CLK	u	MAX	6.7
tPHL .	CLR	Q	MAX	7
tРZН	OF.			5.9
tPZL	- <u>OE</u> 0		MAX	7
tPHZ	- OF	0	MANY	6.6
tPLZ	T UE	u u	MAX	9

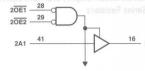
# 18-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

 SN74ABT162825: Output Ports Have Equivalent 25-Ω Series Resistors



Logic Diagram

To Eight Other Channels



To Eight Other Channels

FUNCTION TABLE

	INPUTS	OUTPUT	
OE1	OE2	Α	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	7

RECOMMENDED OPERATING CONDITIONS

necommence of	Elittinto oblitaliti	1	_
PARAMETER	MAX or MIN	ABT	UNIT
Icc	MAX	32	mA
Іон	MAX	-12	mA
lou	MAX	12	mA

SWITCHING CHARACTERISTICS

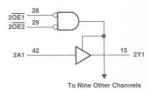
01211101100	HUTSALL STEE	101 TEA - 1613s	And Make
INPUT	OUTPUT	MAX or MIN	ABT
	8 E E E	MAY	3.9
A	1.7 0.0	IVIAX	4.7
<u> </u>		MAN	6.9
UE	1 Y 0-0	WAX	6.3
<u> </u>	V	5457	6.6
UE	Y	IVIAX	6.3
		INPUT	INPUT

UNIT: ns

- SN74ALVTH162827: Output Ports Have Equivalent 30-Ω Series Resistors
- SN74ALVCH162827: Output Ports Have Equivalent 26-Ω Series Resistors







## FUNCTION TABLE (each flip flop)

	INPUTS	OUTPUT	
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	7

†n = 1,2

#### RECOMMENDED OPERATING CONDITIONS

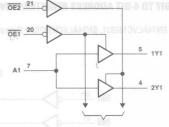
RECOMMENDED OF	PERATING CONDITI	ONS			
PARAMETER	MAX or MIN	ABT	ALVTH 3V	ALVCH 3V	UNIT
Icc	MAX	32	5.5	0.04	mA
Іон	MAX	-12	-12	-12	mA
lou	MAX	12	12	12	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ALVTH 3V	ALVCH 3V
tPLH	Α	Υ	MAN	3.9	3.9	3.8
tPHL .			MAX	4.7	3.7	3.8
tPZH .	ŌĒ		MAN	6.9	5.6	5.1
tPZL	UE	1	MAX	6.3	4.1	5.1
tPHZ	ŌĒ		MAX	6.6	6.3	4.7
PLZ	UE	1	MAX	6.3	5.1	4.7

### 1-BIT TO 2-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS

 SN74ALVCH162830, SN74ALVCHS162830: Output Ports Have Equivalent 26-Ω Series Resistors



Logic Diagram

To 17 Other Channels

## FUNCTION TABLE

INPUTS			OUT	PUTS
OE1	OE2	Α	1Yn	2Yn
L	H	H	H	Z
L	H	L	L	Z
H	L	H	Z	H
H	L	L	Z	L
L	L	H	H	Н
L	L	L	L	L
H	H	X	Z	Z

	H	H	H	Z			
	H	L	L	Z			
	L	H	Z	H			
	L	L	Z	L			
	L	H	Н	H			
	L	L	L	L			
	H	X	Z	Z			
_							

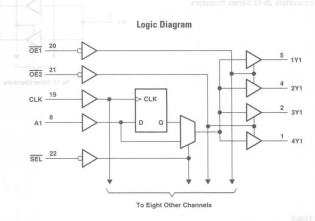
### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	ALVCHS 3V	UNIT
lcc	MAX	0.04	0.04	mA
Іон	MAX	-12	-12	mA
lou	- MAX	12	. 12	mA

SWITCHING CHARAC	TERISTICS		1 470 asie etc	P.P.	30-00-000
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V	ALVCHS 3V
tPLH .	A Y	MAX	3.5	3.5	
tPHL			IVIAA	3.5	3.5
tPZH	ŌĒ	Y	MAX	4.8	4.8
tPZL	UE			4.8	4.8
tPHZ	ŌĒ	V	MAN	5.2	5.2
tPLZ	UE	1	MAX 5.2		5.2
UNIT: ns					-

## 1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS 23 AGOA THE-S OT THE-I

SN74ALVC162831, SN74ALVCH162831: Output Ports Have Equivalent 26-Ω Series Resistors



**FUNCTION TABLE** 

	INP	UTS		OUTPUT
OE	SEL	CLK	Α	Υ
Н	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	+	L	L
L	L	1	H	H

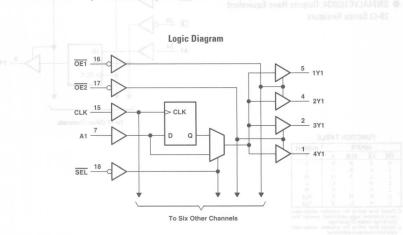
RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVC 3V	ALVCH 3V	UNIT
lcc	MAX	0.04	0.04	mA
Іон	MAX	-12	-12	mA
lor	MAX	12	12	mA

SWITCHING CHAR	ACTERISTICS				
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC 3V	ALVCH 3V
fmax			MIN	150	150
tw Pulse duration	CLK high or low		MIN	3.3	3.3
tsu Setup time	A data before CLK	1	MIN	1.6	1.6
th Hold time	A data after CLK ↑		MIN	1.1	1.1
tPLH		Y	****	4.3	4.3
tPHL .	A	ruggiun	MAX	4.3	4.3
tPLH	OLK	Y	MAN	4.7	4.7
tPHL .	CLK	Y	MAX	4.7	4.7
tPLH	SEL	V	MAN	4.8	4.8
tPHL 8 8 8 1	SEL	Y	MAX	4.8	4.8
tPZH E	ŌĒ	Y	21/	5.1	5.1
tPZL C	OE OE	Y	MAX	5.1	5.1
tPHZ 1	ŌĒ	Y	39	5.1	5.1
tPLZ	J UE	Y	MAX	5.1	5.1

# 1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS 2UG JA28-3VIMU TIB-81

SN74ALVCH162832: Output Ports Have Equivalent 26-Ω Series Resistors



**FUNCTION TABLE** 

	INP	UTS		OUTPUT
OE	SEL	CLK	Α	Y
Н	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	+	L	L
L	L		H	H

#### RECOMMENDED OPERATING CONDITIONS

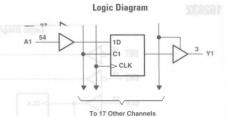
PARAMETER	MAX or MIN	ALVCH 3V	UNIT
Icc	MAX	0.04	mA
Іон	MAX	-12	mA
lor	MAX	12	mA

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
fmax			MIN	150
tw Pulse duration	CLK high or low		MIN	3.3
tsu Setup time	A data before CLK ↑		MIN	1.6
th Hold time	A data after CLK ↑		MIN	1.1
tPLH .	19118	V	MAN	4.3
tPHL PL	A	dold	MAX	4.3
tPLH	01.14	v	MAX	4.7
tPHL 10	CLK	,	MAX	4.7
tPLH .	SEL	V	MAX	4.8
tPHL PI	SEL	7	MAX	4.8
tPZH	ŌĒ	Υ	MAX	5.1
tPZL	UE	Y	IVIAX	5.1
tPHZ	ŌĒ	Y	MAX	5.1
tPLZ	UE	17	WAX	5.1



### 18-BIT LINIVERSAL RIIS DRIVED



#### **FUNCTION TABLE**

	INI		OUTPUT	
OE	LE	CLK	Α	Y
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	Н
L	H	*	L	L
L	H	*	H	H
L	H	H	X	Yot
L	Н	L	X	Y <sub>0</sub> ‡
+ Output	level I	before the	indicate	d steady-state

<sup>†</sup> Output level before the indicated steady-state input conditions were established, provided that CLK is high before LE goes high † Output level before the indicated steady-state input conditions were established

RECOMMENDED OPERATING CONDITIONS

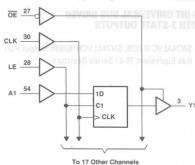
PARAMETER	MAX or MIN	ALVC 3V	UNIT
Icc	MAX	0.04	mA
Іон	MAX	-12	_mA
lou	MAX	12	mA

THE CHORD	Mill to 2.41/	TUSTUO	TURKE	83	SM
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC 3V	
fmax 0.5	Mild	MIN	150	ulb.	
tw Pulse duration	LE low		MIN	3.3	
tw Pulse duration	CLK high or low		MIN	3.3	200
5.0	Data before CLK ↑			1.7	
tsu Setup time	Data before LE ↑, CLK	high -	MIN	1.9	
	Data before LE ↑, CLK	MIN	1.5		
th Hold time	A data after CLK ↑	MIN	0.7		
	Data after LE ↑, CLK h	MIN	0.9		
	Data after LE ↑, CLK I	MIN	0.9		
tPLH I I	A				
tPHL LE	A	1.1	MAX	4.2	
tPLH	LE	Y	MAX	5.8	
tPHL I E	LC	17	IVIAA	5.8	
tPLH	CLK	٧	MAX	5.4	TOT
tphl.	CLK Y		IVIAA	5.4	7
tРZH	- OE Y		MAX	5.9	
tPZL	UE I		IVIAA	5.9	]
tPHZ	- OE	٧	MAX	5	1
tPLZ	UE	1	IVIAX	5	1

#### **Logic Diagram**

### 18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

 SN74ALVC162835, SN74ALVCH162835: Output Port Has Equivalent 26-Ω Series Resistors



#### FUNCTION TABLE

input conditions were established

INPUTS				OUTPUT
OE	LE	CLK	Α	Y
Н	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L		L	L
L	L		H	H
L	L	LorH	X	Yot

PARAMETER	MAX or MIN	ALVC 3V	ALVCH 3V	UNIT
Icc	MAX	0.04	0.04	mA
Іон	MAX	-12	-12	mA
lou	MAX	12	. 12	mA

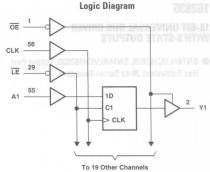
#### RECOMMENDED OPERATING CONDITIONS

#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC 3V	ALVCH 3V
fmax	1 50		MIN	150	150
e Dolos dosedes	LE low		MIN	3.3	3.3
tw Pulse duration	CLK high or low		MIN	3.3	3.3
	Data before CLK ↑	MIN	1.7	1.7	
tsu Setup time	Data before LE 1, C	MIN	1.5	1.5	
	Data before LE 1, C	MIN	1	1	
	A data after CLK ↑	MIN	0.7	0.7	
th Hold time	Data after LE 1, CLI	MIN	1.4	1.4	
	Data after LE 1, CLI	MIN	1.4	1.4	
tPLH	A Y		MAN	4.2	4.2
tPHL .	7 A	Y (	MAX	4.2	4.2
tPLH .	15	Y		5.1	5.1
tphl.	LE	Υ	MAX	5.1	5.1
tplH .	011/	Y	1444	5.4	5.4
tphl .	CLK	Y	MAX	5.4	5.4
tрzн	ŌĒ	Y		5.5	5.5
tPZL	T UE	Υ	MAX	5.5	5.5
tPHZ	ŌĒ	Y	MAN	4.5	4.5
tPLZ	- UE	Y	MAX	4.5	4.5

# 20-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

 SN74ALVC162836, SN74ALVCH162836: Output Port Has Equivalent 26-Ω Series Resistors



#### **FUNCTION TABLE**

	INF	OUTPUT		
OE	LE	CLK	Α	Y
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	1	L	L
L	H	1	H	H
L	H	LorH	X	Yot

† Output level before the indicated steady-state input conditions were established

#### RECOMMENDED OPERATING CONDITIONS

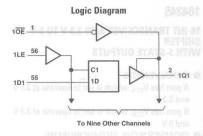
ENATING CONDIT	10143		
MAX or MIN	ALVC 3V	ALVCH 3V	UNIT
MAX	0.04	0.04	mA
MAX	-12	-12	mA
MAX	12	12	mA
	MAX or MIN  MAX  MAX	MAX 0.04 MAX -12	MAX or MIN

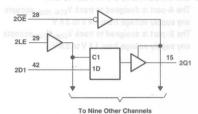
#### SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC 3V	ALVCH 3V
fmax			MIN	150	150
	LE low	1(3)	MIN	3.3	3.3
tw Pulse duration	CLK high or low	V	MIN	3.3	3.3
	Data before CLK ↑		MIN	1.5	1.5
tsu Setup time	Data before LE 1, C	LK high	MIN	1.3	1.3
	Data before LE 1, C		MIN	1.2	1.2
th Hold time	A data after CLK ↑		MIN	0.9	0.9
	Data after LE ↓, CLI	K high	MIN	1.1	1.1
	Data after LE 1, CLI		MIN	1.1	1.1
tPLH .	A	Y	CARAN	4	4
tPHL	Α Α	Y	MAX	4	4
tPLH .	- LE	Y I	MAN	5.1	5.1
tphl.	LE	Y	MAX	5.1	5.1
tPLH .	CLK	ν	MAX	5	5
tPHL .	ULK	1	IWAX	5	5
tPZH	ŌĒ	Y	MAX	5.5	5.5
tPZL	OE.	Y		5.5	5.5
tРНZ	ŌE	V 5	MAX	5.1	5.1
tPLZ	] UE	Y	IVIAX	5.1	5.1

#### 20-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

- SN74ABT162841: Output Ports Have Equivalent 25-Ω Series Resistors
- SN74ALVCH162841: Output Ports Have Equivalent 26-Ω Series Resistors





#### **FUNCTION TABLE** (each 10-bit latch)

- 1	NPUTS	6	OUTPUT
OE	LE	D	Q
L	H	H	Н
L	H	L	L
L	L	X	Qn
H	X	X	Z

#### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ALVCH 3V	UNIT
Icc	MAX	89	0.04	mA
Іон	MAX	-12	-12	mA
lou	MAX	12	12	mA

PARAMETER	MAX or MIN	ABT	ALVCH 3V	UNIT
Icc	MAX	89	0.04	mA
Іон	MAX	-12	-12	mA
lou	MAX	12	12	mA

#### SWITCHING CHARACTERISTICS

INPUT	OUTPUT	MAX or MIN	ABT	ALVCH 3V				
LE high or low	Am	MIN	4	3.3				
Data before LE ↓	Am	MIN	0.8	1.1.0				
Data after LE ↓	Am	MIN	1.8	1.1				
	- Am		5.2	4.3				
1 0	Au I	MAX	6	4.3				
	Am		5.4	4.7				
LE	u MAX		LE U MAX 5.8 4.7					
			5.7	5.3				
UE UE	Ε   Ω	UE U MAX		6.5	5.3			
			6.5	4.4				
OE OE	HUBBYA Q 85VA	MAX	7.1	4.4				
	LE high or low Data before LE ↓	LE high or low Data before LE 1 Data after LE 1  D Q AM  LE Q  OE Q	LE high or low         MIN           Data before LE ↓         MIN           Data after LE ↓         MIN           D         Q         MAX           LE         Q         MAX           —         Q         MAX	LE high or low MIN 4 Data before LE ↓ MIN 0.8 Data after LE ↓ MIN 1.8 D Q MAX 5.2 E Q MAX 5.4  - LE Q MAX 5.8 - OE Q MAX 6.5  DE Q MAX 6.5	LE high or low	LE high or low		

UNIT: ns

	Anna Anna	No really	A6 1 635 A	76 - 8007	AP - 1270-5

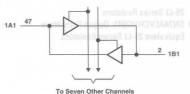
#### ● SN/4ALVU164245:

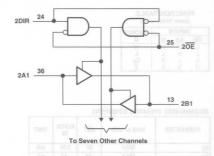
A port has  $V_{\text{CCA}}\text{, which is set to operate at 2.5 V}$  and 3.3 V

B port has  $V_{\text{CCB}}$ , which is set to operate at 3.3 V and 5 V

#### SN74AVCB164245, SN74AVCBH164245:

The A-port is designed to track V<sub>CCA</sub>, v<sub>CCA</sub> accepts any supply voltage from 1.4 V to 3.6 V The B-port is designed to track V<sub>CCB</sub>, V<sub>CCB</sub> accepts any supply voltage from 1.4 V to 3.6 V





#### FUNCTION TABLE (each 8-bit section)

INPUTS					
	DIR	OPERATION			
	L	B data to A bus			
	H	A data to B bus			
	X	Isolation			

#### RECOMMENDED OPERATING CONDITIONS

		1075018				
PARAMETER	MAX or MIN	ALVC	TEA	AVCB	AVCBH	UNIT
Icc (5V)	MAX	0.04	à.	- 1/1		mA
Icc (3V)	MAX	0.02	0.0	0.04	0.04	mA
Iон (5V)	MAX	-24	8.7	- 1/1		mA
Ior (5V)	MAX	24	5.2			mA
Iон (2.3V)	MAX	-12	35	-8	-8	mA
IoL (2.3V)	MAX	12	3.4	8	8	mA

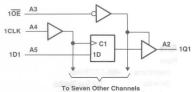
#### SWITCHING CHARACTERISTICS

			1.4	ALVC		AVCB	AVCBH	
PARAMETER	INPUT	OUTPUT	MAX or MIN	VCCB: 3V VCCA: 2.3V	VCCB: 5V VCCA: 3V	VCCB: 3V VCCA: 2.3V	VCCB: 3V VCCA: 2.3V	
tPLH	Δ.	В	MAX	7.6	5.8	3.4	3.4	
tphl .	Α	В	IVIAX	7.6	5.8	3.4	3.4	
tPLH .	В	А		MAX	7.6	5.8	3.7	3.7
tPHL .	В		IVIAA	7.6	5.8	3.7	3.7	
tPZL	ŌĒ		B MAX	11.5	8.9	5.1	5.1	
tPZH	UE	В		11.5	8.9	5.1	5.1	
tPZL	ŌĒ	Δ.	A MAN	12.3	9.1	4.2	4.2	
tPZH	UE	A	MAX	12.3	9.1	4.2	4.2	
tPLZ	ŌĒ	В	MAX	10.5	9.5	3.3	3.3	
tPHZ	UE	. Б		10.5	9.5	3.3	3.3	
tPLZ	OE A	<u> </u>	Α	MAX	9.3	8.6	3	3
tPHZ		IVIAA	9.3	8.6	3	3		

## 3.3-V ABT 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP Degan 2 technical enhanced enhanced and the second

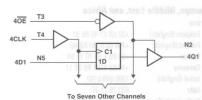
Output Ports Have Equivalent 22-Ω Series Resistors

#### **Logic Diagram**



20E H3
2CLK H4
2D1 E5 C1 E2 2Q1
To Seven Other Channels

3OE J3
3CLK
J4
3D1 J5
To Seven Other Channels



FUNCTION TABLE (each 8bit flip-flop)

INPUTS			OUTPUT
ŌĒ	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	HorL	X	Qn
Н	X	X	Z

RECOMMENDED OF	PERATING CONDITI	ONS	
PARAMETER	MAX or MIN	LVTH 3V	UNIT
lcc	MAX	10	mA
Іон	MAX	-12	mA
lou	MAX	12	mA

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V
fmax				160
tw Pulse duration,	CLK high or low	MIN	3	
	Data before CLK 1,	MIN	1.8	
tw Pulse duration, tsu Setup time th Hold time tPLH tPHL	Data before CLK T, data low		MIN	1.8
e Distriction	Data after CLK 1, d	ata high	MIN	0.8
th Hold time	Data after CLK 1, data low		MIN	0.8
fmax         to Pulse duration, CLK high or low           tw Setup time         Data before CLK ↑, Data before CLK ↑, Data after CLK ↑, d           b Hold time         Data after CLK ↑, d	0	MAN	5.3	
	CLK	u u	IVIAX	4.9
tpzh	Pulse duration, CLK high or low	MAY	5.6	
tPZL	UE UE	before CLK ↑, data low         MIN           after CLK ↑, data high         MIN           after CLK ↑, data high         MIN           CLK         MIN           CLK         Q           MAX           OE         Q           MAX	4.9	
tPHZ	OF.	ata before CLK T, data high ata before CLK T, data high ata before CLK T, data low AIIN ata after CLK T, data high MIN ata after CLK T, data high MIN CLK Q MAX  OE Q MAX	5.4	
tPLZ	- UE 0		MAX	5

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